SCL RESPOND Basket -2021

A	Area	VLSI Design (SCL)
A1	Sub Area	ASIC Design (SCL)
A1.1	**Design of Instrumentation Amplifier** A High-Precision Instrumentation Amplifier with large CMRR is required for the Sensor Signal conditioning applications. Instrumentation amplifier is a versatile device used for amplification of small differential mode signals while rejecting large common mode signal at the same time. In a typical signal conditioning chain, the output of the sensor goes to the instrumentation amplifier. The instrumentation amplifier amplifies the small output signal of the sensor and gives it to the ADC for digitization. **Target Specification:** • Supply Voltage: 3.3V • Temperature Range: -40 degC to 125 degC • Programmable Gain: 1 to 1000 • Low noise < 0.3µV p-p at 0.1 Hz to 10 Hz • Low non linearity < 20ppm (Gain = 1) • High CMRR (Common Mode Rejection Ratio) > 90dB (Gain=1) • Low offset voltage < 100µV • 3 dB Bandwidth: 1MHz (at Gain = 1) The design of the proposed Instrumentation Amplifier is to be carried out in SCL 180 nm process.	
A1.2	**Design of 14 bit 500 MSPS DAC in SCL's 180nm Technology** Digital to Analog Converter (DAC) is a device that transforms digital data into an analog signal. The digital data may be produced from a microprocessor, Application Specific Integrated Circuit (ASIC), or Field Programmable Gate Array (FPGA), but ultimately the data requires the conversion to an analog signal in order to interact with the real world. This DAC should cater test and Measurement, Imaging and high-Precision, high-Speed data acquisition applications with these features in Junction temperature range -40 °C to +125 °C **Target Specifications:** • Resolution 14 bits	

	• Speed 500 MSPS • FSR Current 2 mA-20 mA • SFDR >74 dBFS at 70 Msps • DNL < ±0.5LSB • INL < ±2LSB • Gain Error < ±2 % of FSR • Output Compliance range -0.5 to +1 V @ Full Scale Current = 20 mA • Offset Error < ±0.01 % of FSR @ Mid Code • Power Dissipation < 600 mW • Power supply 1.8/3.3 V • Technology SCL 180 nm
A1.3	**Design of 8-Bit 1GSPS Flash ADC** The flash analog-to-digital converter (ADC) architecture is the most popular topology for video processing, telecommunications, digital imaging etc. designs because its gives highest speed. This design of ADC should cater imaging as well as communication applications with these features in Junction temperature range -40 °C to +125 °C **Target Specifications:** SNDR >46 dBFS at 1000 Msps SFDR >60 dBc at 1000 Msps DNL <±0.5LSB INL <±0.5LSB No missing Code Gain Error<±0.5LSB Offset Error<±0.5LSB Output data format in LVDS or CMOS **Deliverables:** i. Design Details along with all schematics and layout ii. GDSII file of Design iii. Test results and evaluation board
A1.4	**Design of Radiation Hardened Dual port SRAM – Different Cuts** DPRAM Cuts of following variations are needed which can be used as Embedded Solution or Stand-alone Memory Chip Voltage Levels – 1.8 V / 3.3 V Access Time - < 5 ns

	Address Bit Range – 4 Bits to 14 Bits Data Bit Range – 4 bits to 72 Bits Radiation Tolerance – TID >300 Krad (Si), SEL > 80 MeV-cm2/mg, SEU > 50 MeV-cm2/mg
A1.5	**Design of High Speed CMOS Standard Cell Library in 180nm SCL process** Standard cell library contains a collection of components that are standardized at the logic or functional level, and consists of cells or macro – cells based on the unique layout. The importance of standard cell library design methodology is growing with very-large-scale integration (VLSI) technology advancement due to its usage in VLSI EDA flows. In high performance standard cell library, the main objective is to increase performance of logic cells that satisfies the given specifications. The benefit of high performance cell library is used in processors, high computational IC's etc. designs where density will be neglected to meet the performance. **The Standard Cell library should include the following criteria :** 1. Static CMOS Library 2. PVT variation : not more than 20% 3. D flipflops in the library should be working upto 2GHz clock frequency 4. Library should have Multibit D FlipFlops : 2bits, 4 bits, 8bits 5. Tracks –> 9 or 12(any one for complete library) 6. Multiple drive strength of the cells 7. Multiple inputs and various cell combination 8. Supply Voltage 1.8V 9. Temperature range -40°c to 125°c 10. Views and files required in the library: **Deliverables:** • cdl – cdl netlist for LVS with VDD and VSS defined as local and cdl netlist for LVS with VDD and VSS defined as global. • doc – datasheets

	• gds – gds for all cells • lef – lef abstract • liberty – 27 corners timing information (PVT combinations) in both CCS and NLDM (CCS-P, CCS-N to be 4ncluded). • spc – spice netlist for all cells • spc_simple – spice netlist for all cells without parasitics. • verilog – verilog model for all cells.
A1.6	**Design of DSP Processor in 180nm SCL process** A digital signal processor (DSP) is a specialized microprocessor chip, with its architecture optimized for the operational needs of digital signal processing. They are widely used in audio signal processing, telecommunications, digital image processing, radar, sonar and speech recognition systems, etc. The goal of a DSP is to measure, filter or compress continuous real-world analog signals. Most general-purpose microprocessors can also execute digital signal processing algorithms successfully, but may not be able to keep up with such processing continuously in real-time. Also, dedicated DSPs usually have better power efficiency, are more suitable in portable devices because of power consumption constraints. DSPs often use special memory architectures that are able to fetch multiple data or instructions at the same time. DSPs often also implement data compression technology. DSPs are designed to execute complex math in parallel, which is common in many signal processing applications. By having hardware and an instruction set architecture (ISA) optimally designed for the FFT, the FFT is executed with higher performance in shorter time—and at lower energy. Power is directly proportional to the clock frequency and voltage squared. To run the clock at a higher frequency requires a higher voltage, which leads to an exponential increase in power draw. Hence, it is desirable if DSP is able to run at low clock frequencies while delivering high performance through hardware multi-threading, and by maximizing work per clock cycle.
A1.7	**Design and development of Power Analysis Attack Tolerant Cryptographic Processor for Security Critical Space Applications** This topic is targeted for design and development of Cryptographic processor which is power analysis attack (side channel) tolerant. It is relevant for our

	futuristic cryptographic development activities & as additional hardware security mechanism that may be an integrated feature of attack prone ASICs to be used in space applications.	
B	**Area**	**Process Technology (SCL)**
B1	**Sub Area**	**CMOS Process (SCL)**
B1.1	**Technology Development of High Power RF LDMOS Device** SCL has initiated in-house development of high Power RF LDMOS devices. In this work development of two different RF LDMOS devices for 650MHz (~500Watt) and 325MHz (1kWatt) operations has been initially targeted. In this regard SCL requires support for following topics: 1. Device Design for state of the art and reliable, rugged High voltage (~50V) RFLDMOS. 2. Process & Implant conditions (must be supported with TCAD simulated results). 3. Test chip for RF LDMOS process integration 4. RF characterization and Reliability analysis of developed devices.	
B1.2	**Modelling of High Voltage (10-20, 40-60V) N /P LDMOS devices developed at SCL in 180nm CMOS baseline process technology** A Simple concise statement about the investigation/theme and the expected deliverables in around 250 words Process development work at SCL is in progress for the process integration of LDMOS (VDS: 10-20, 40-60V; VGS: 3.3-5V) devices (n and PMOS) in standard 180nm baseline process. Once the devices are enabled, SPICE device models are required for the above LDMOS devices for circuit design implementation. The developed models should be accurately predicting both DC and AC performance of the devices over a range of voltage, temperatures (-55 to 125C) and frequencies. **Deliverables:** i. Device characterization (DC-IV, CV, RF) as required for Model parameter extraction. ii. Industry standard LDMOS Device Models (Scalable /Binned) iii. Model QA report complying IEEE/CMC model validation tests and accuracy.	

B2	**Sub Area**	**CCD Process (SCL)**
B2.1	**Modelling of buried channel MOSFET:** The existing CCD process development at SCL is based on buried channel technology to cater the need of high Charge Transfer Efficiency with high SNR. The output stage of CCD comprises of multiple stage source follower amplifier connected with sense node to produce voltage equivalent of collected charge with greater sensitivity. To design CCD output amplifier, modelling of n-buried channel MOSFET is required using SPICE.	
C	**Area**	**Compound Semiconductor Technology (SCL)**
C.1	**Development of compound semiconductors based THz detectors for space applications** THz detectors are at the heart of THz astronomy. With the advent of III-Nitride (III-N) based devices, once can exploit its unique 2 Dimensional Electron Gas (2DEG) properties to realize broadband THz detectors. By designing appropriate antenna coupling with III-N based High Electron Mobility Transistor, the sensitivity and speed can be improved. The present project calls for the design and development of III-N based THz detectors in the potentially ranging from 0.3 – 0.9 THz. The scope of the project includes • Identifying appropriate antenna architecture to be coupled with III-N HEMT device for desired frequency range • Co-development of circuit level and system level design for THz detector • Development and calibration of circuit and system level models • Demonstration of prototype	
C.2	**Epitaxial growth of InP on Si for millimetre wave communication applications** InP offers a clear performance advantage over conventional CMOS devices in terms of high frequency performance. However, the use of native InP substrates is usually of smaller size than commercial Si wafers, thereby limiting the number of devices realized on a single wafer. Additionally, the costs of InP substrates are much higher than Si substrates. On the other hand, epitaxial growth of InP layers on Si substrates offer an alternative route to integrate InP devices with well-established Si technology. In this aspect,	

	this project calls for development of epitaxial growth of InP epitaxial layers on Si targeting mm wave applications. The scope of the project includes • Understanding the fundamentals of InP growth on Si substrates • Use of different nucleation techniques and methods such as aspect ratio trapping to reduce defects in the grown InP layers • Using the understanding to realize the growth of device grade InP epitaxial layers on Si substrates.	
D	**Area**	**MEMS Design & Process Technology (SCL)**
D.1	**Design/Development/Testing of Silicon Nanowire based biosensor (BioFET) for clinical diagnostics in space** Includes simulation of the response of a Si-nw BioFET sensor both as fabricated and when exposed to analyte.Identification, development, testing etc of bio-markers/analytes alone, compatible for use in BioFETs, can also be considered. **Deliverables:** • Detailed documents on design, simulation, test etc. • Simulation Code/model.	
E	**Area**	**IC Package Design & Development (SCL)**
E.1	**Optimisation of electrical design in HTCC package with mutidrop lines** In case of multichip substrate design having mutidrop connections, it becomes paramount to optimize the floor plan to meet assembly & fabrication constraints while getting optimum electrical performances. Parametric studies for varying dielectric thicknesses, trace widths, metallization thicknesses, via sizes, pin outlines CQFP or PGA etc. **Target Specification:** Design multi die package having processor, memory, digital ASIC, analog ASIC, MEMS sensor, Signal conditioner IC, power die etc. • Power Distribution Network Impedance <= 0.2ohm • Speed of operation 200MHz or better	

	Deliverables: Design philosophy and layout and proof of concept through fabrication & testing.
E.2	**Design and Development of deposition type MultiChip Module using silicon** One of the promising multi die substrates are Deposition type (MCM-D) on semiconductor material. Design and realisation of this substrate on Silicon for ICs like Processors, ASIC and Analog ICs to be taken up with promising electrical performances of complete module. **Target Specification:** Design multi die package having processor, memory, ASIC, transceiver and power die on silicon substrate. • Design must follow 180 nm SCL Fab Design guidelines. • Power Distribution Network Impedance <= 0.5ohm. • operation frequency 100MHz or better **Deliverables:** Design & layout for substrate; Design validation through siliconisation using SCL fab & Testing.
E.3	**Development of multi layer IC package using 3-D printing advanced technologies** Custom development of multilayer substrate having buried power planes and vias using Additive technologies is an open area to meet the design evaluation requirements. In addition to high packaging efficiency the substrates to meet specifications as per performance specifications of MIL 38535 and test conditions of MIL883 for hermetic space grade reliability & applications. **Deliverables:** Technology know-how transfer including design and fabrication. 100 to 120 pin QFP package delivery for technology evaluation.