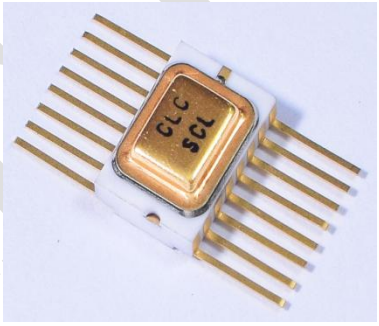
SCL CLOCK DRIVER

EF1105-0

DATA SHEET



Version 1.0, March 2019

Semi–Conductor Laboratory

Department of Space, Government of India

FEATURES:

- High voltage 0.35 um AMS CMOS Process
- Intersil EL7457 pin to pin compatible
- Four channels input
- Input level shifters
- $8V \geq VL \geq -5V$
- $0V \leq VH \leq 15V$
- 16ns t_R/t_F at 1000pF C_{LOAD}
- 5 MHz operating frequency
- 2ns rise and fall time match
- 3ns prop delay match
- Wide output voltage range
- Low power dissipation (<5W at 5MHz with output load of 1000pf on each output)
- 0.6A peak drive
- Low on-resistance
- Input level shifters
- TTL/CMOS input-compatible
- Hermetic sealed 16 pin Lead Flat package (SOP)
- Radiation Hardened (TID) up to 140Krad(Si)
- Single event latch (SEL) immune up to 50 MeV-cm^2/mg
- Temperature range of -55°C to +125°C
- TTL/CMOS input-compatible
- **θj_c: 7.12 °C/Watt**

PRODUCT DESCRIPTION:

The EF1105-0 is a high speed non-inverting, quad CMOS driver designed on High voltage 0.35 um AMS CMOS Process (H35B4D3). It is capable of running at clock rates up to 5 MHz and features 0.6A typical peak drive capability and a nominal low on-resistance. The EF1105-0 is ideal for driving highly capacitive loads, such as storage and vertical clocks in CCD applications. It is also well suited to ATE pin driving, level-shifting, and clock-driving applications. Each output can be switched to either the high (VH) or low (VL) supply pins, depending on the related input pin. The inputs are compatible with both 3V and 5V CMOS and TTL logic. The output enable (OE) pin can be used to put the outputs into a high-impedance state. This is especially useful in CCD applications, where the driver should be disabled during power down. The driver has fast rise and fall times, which are typically matched to within 2ns (for C_{Load}=1nF). The ceramic flat pack (16 Lead) is taken for packaging.

DEVICE SUMMARY:

Table-1: Device Summary

Reference	Package	Pins	Lead Finish	Description
EF1105-0	Ceramic Flat pack	16	Gold	Engineering

BLOCK LEVEL DIAGRAM:

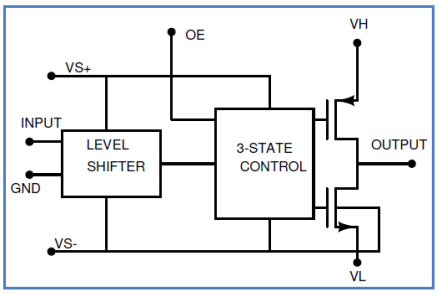


Figure-1: Block Level Diagram

PIN CONFIGURATION:

Table-2: Pin Configuration 16 Pin Lead Package

Pin No	Signal Name	Pin Type	Pin Description	Remarks
1	INA	AI	Input channel A	
2	OE	DI	Output enable	Active High
3	INB	AI	Input channel B	
4	VL	AP	Low voltage pin	
5	GND	GND	Input logic ground	
6	NC			
7	INC	AI	Input channel C	
8	IND	AI	Input channel D	
9	Vs-	AP	Negative supply voltage	
10	OUTD	AO	Output channel D (Load 1nF)	
11	OUTC	AO	Output channel C (Load 1nF)	
12	VH	AP	High voltage input pin	
13	NC			
14	OUTB	AO	Output channel B (Load 1nF)	
15	OUTA	AO	Output channel A (Load 1nF)	
16	Vs+	AP	Positive supply voltage	

- Pin Type DI = Digital Input, AO = Analog Output, AP = Analog Power, AGND = Analog Ground
- De-coupling capacitors of 10uF and 0.1uF in parallel are recommend on Analog Power pins w.r.t ground pin

DEVICE PIN DIAGRAM:

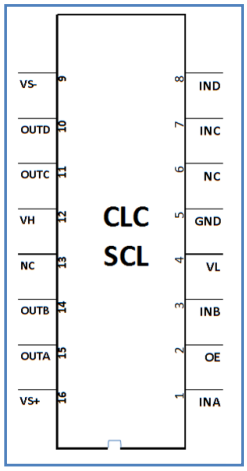


Figure-2: Device Pin Diagram 16 Pin Lead Package

Table-3: Pin Configuration 16 Pin DIP (CoB) Package

Pin Number	Pin Description	Remarks
1	Input B	-
2	VL	Both short on CoB
3	VL	
4	Ground	-
5	Input C	-
6	Input D	-
7	VS-	Short with Ground on CoB
8	Output D	-
9	Output C	-
10	VH	Both short on CoB
11	VH	
12	Output B	-
13	Output A	-
14	VS+	Short with VH on CoB
15	Input A	-
16	Output Enable	Pulled up to VS+ through 10kΩ on the CoB

Note:
De-coupling capacitor of 1µF between VH and ground (C16) connected on the CoB
De-coupling capacitor of 1µF between VL and ground (C15) connected on the CoB

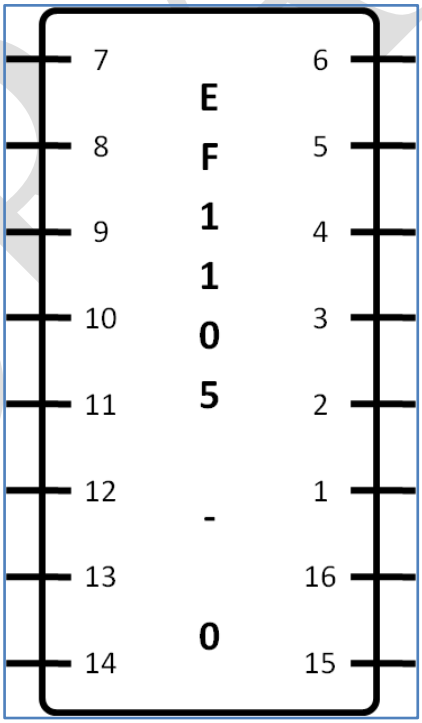


Figure-3: Device Pin Diagram 16 Pin DIP (CoB) Package

RECOMMENDED OPERATING CONDITIONS:

Table-4: Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vs+ to Vs-	Supply Voltage (Vs+ to Vs-)	5	12	15	V
Vs- to GND	Substrate Voltage (Vs- to GND)	-5	0	0	V
V_H	VH Voltage	Vs- + 2.5	Vs+	Vs+	V
V_L	VL Voltage	Vs-	0	Vs+	V
V_H to V_L	VH to VL Voltage	0	-	15	V
V_L to Vs-	VL to Vs- Voltage	0	-	8	V
V_{IH}	Logic"1" Input Voltage	2.0	3.3	5	V
V_{IL}	Logic"0" Input Voltage	0	0	0.8	V
T_A	Temperature range	-55	25	+125	ºC

ABSOLUTE MAXIMUM RATINGS (1):

Over operating free-air temperature range (unless otherwise noted),

Table-5: Absolute Maximum Rating

PARAMETER	UNIT
Supply Voltage range **(Vs+ to Vs-)**	18 V
Input Voltage range **(V_H,V_L)**	Vs- –0.3 V, Vs_+ +0.3 V
T_{stg} , Storage temperature range	–65°C to 150°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DC ELECTRICAL SPECIFICATIONS:

Test condition: Vs+ = V_H = 5V, V_L = Vs– = GND = 0V, T_A = 25ºC, unless otherwise specified

Table-6: DC Electrical Characteristics

Symbol	Parameter	Test Conditions	Pin	Min.	Typ.	Max.	Unit
INPUT							
I_{IH}	Logic "1" Input Current	V_{IH}=5V	INA, INB, INC, IND		0.1	10	uA
I_{IL}	Logic "0" Input Current	V_{IL}=0V			0.1	10	uA
OUTPUT							
V_{OH}	Output Voltage High		OUTA, OUTB, OUTC, OUTD	4.5	5.03	5.5	V
V_{OL}	Output Voltage Low			–0.2	0.44	0.5	V
POWER SUPPLY							
I_{DD} (static)	I_{DDL} (Inputs at Low)	0V at all Inputs	Vs+		4.24	10	mA
			Vs–	-5	-1.32		
			V_H		0.04	2	
			V_L	-2	-0.04		
	I_{DDH} (Inputs at High)	3.3V at all Inputs	Vs+		3.95	10	mA

Symbol	Parameter	Test Conditions	Pin	Min.	Typ.	Max.	Unit
			Vs–	-5	-1.15		
			V_H		0.05	2	
			V_L	-2	-0.04		
I_{DD} (Dynamic)	I_{DD}, dynamic	0 to 3.3V square wave input with frequency of 5MHz , 50% duty cycle	Vs+		9	12	mA
			Vs–	-10	-6		
			V_H		90	150	
			V_L	-150	-96		

AC ELECTRICAL SPECIFICATIONS:

Test condition: Vs+ = V_H = 5V, V_L = Vs– = GND = 0V, T_A = 25ºC, unless otherwise specified

Table-7: AC Electrical Characteristics

Symbol	Parameter	Test Conditions	Typical	Units
T_R	Output rise time (10% to 90%)	0 to 3.3V square wave input with frequency of 5MHz , 50% duty cycle, C_L=1000pF	21.9	ns
T_F	Output fall time (90% to 10%)		20.7	ns
$t_{RF\Delta}$	t_R, t_F Mismatch		1.2	ns
t_{D+}	Turn-Off Delay Time		38	ns
t_{D-}	Turn-On Delay Time		41	ns
t_{DD}	t_{D-1} - t_{D-2} Mismatch		3	ns
t_{ENABLE}	Enable Delay Time		39	ns
$t_{DISABLE}$	Disable Delay Time		78	ns

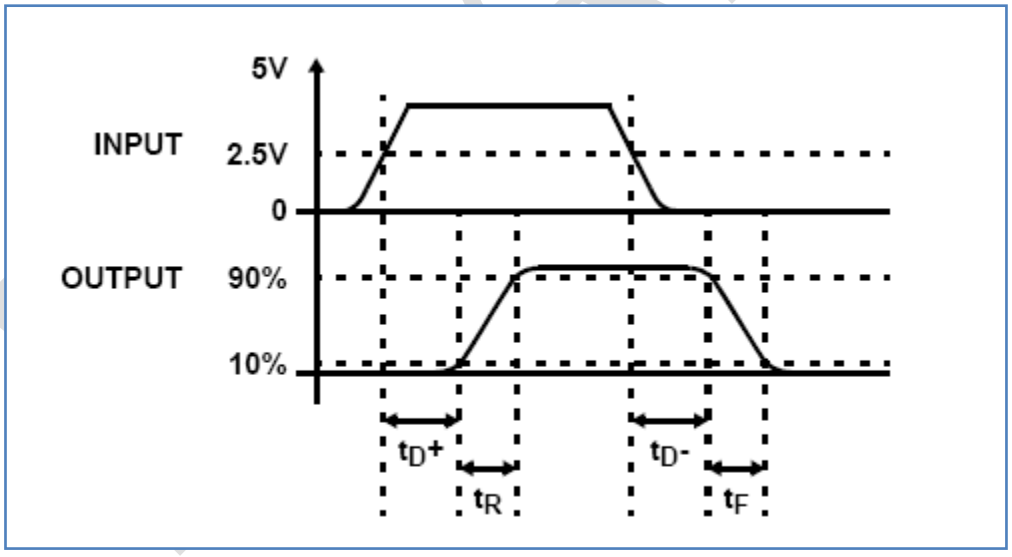


Figure-4: Timing Diagram

DC ELECTRICAL SPECIFICATIONS:

Test condition: Vs+ = V_H = 15V, V_L = Vs– = GND = 0V, T_A = 25ºC, unless otherwise specified

Table-8: DC Electrical Characteristics

Symbol	Parameter	Test Conditions	Pin	Min.	Typ.	Max.	Unit
INPUT							
I_{IH}	Logic "1" Input Current	V_{IH}=5V	INA, INB, INC, IND		0.1	10	uA
I_{IL}	Logic "0" Input Current	V_{IL}=0V			0.1	10	uA
OUTPUT							
V_{OH}	Output Voltage High		OUTA, OUTB, OUTC, OUTD	13.4	14.22	15.6	V
V_{OL}	Output Voltage Low			–0.2	0.44	0.5	V
POWER SUPPLY							
I_{DD} (static)	I_{DDL} (Inputs at Low)	0V at all Inputs	Vs+		20.51	25	mA
			Vs–	-5	-1.36		
			V_H		0.64	2	
			V_L	-2	-0.06		
	I_{DDH} (Inputs at High)	3.3V at all Inputs	Vs+		20.62	25	mA
			Vs–	-5	-1.36		
			V_H		0.74	2	
			V_L	-2	-0.05		
I_{DD} (Dynamic)	I_{DD}, dynamic	0 to 3.3V square wave input with frequency of 5MHz , 50% duty cycle	Vs+		40	50	mA
			Vs–	-30	-19		
			V_H		250	400	
			V_L	-400	-275		

AC ELECTRICAL SPECIFICATIONS:

Test condition: Vs+ = V_H = 15V, V_L = Vs– = GND = 0V, T_A = 25ºC, unless otherwise specified

Table-9: AC Electrical Characteristics

Symbol	Parameter	Test Conditions	Typical	Units
T_R	Output rise time (10% to 90%)	0 to 3.3V square wave input with frequency of 5MHz , 50% duty cycle, C_L=1000pF	16.7	ns
T_F	Output fall time (90% to 10%)		16.2	ns
$t_{RF\Delta}$	t_R, t_F Mismatch		0.5	ns
t_{D+}	Turn-Off Delay Time		21	ns
t_{D-}	Turn-On Delay Time		23	ns
t_{DD}	t_{D-1} - t_{D-2} Mismatch		02	ns
t_{ENABLE}	Enable Delay Time		20	ns
$t_{DISABLE}$	Disable Delay Time		39	ns

DC ELECTRICAL SPECIFICATIONS:

Test condition: Vs+ = V_H = 5V, V_L = Vs– = -5V, GND = 0V, T_A = 25ºC, unless otherwise specified

Table-10: DC Electrical Characteristics

Symbol	Parameter	Test Conditions	Pin	Min.	Typ.	Max.	Unit
INPUT							
I_{IH}	Logic "1" Input Current	V_{IH}=5V	INA, INB, INC, IND		0.1	10	uA
I_{IL}	Logic "0" Input Current	V_{IL}=0V			0.1	10	uA
OUTPUT							
V_{OH}	Output Voltage High		OUTA, OUTB, OUTC, OUTD	4.5	5.1	5.5	V
V_{OL}	Output Voltage Low			–5.5	-4.8	-4.5	V
POWER SUPPLY							
I_{DD} (static)	I_{DDL} (Inputs at Low)	0V at all Inputs	Vs+		4.75	10	mA
			Vs–	-10	-4.73		
			V_H		0.05	2	
			V_L	-5	-3.39		
	I_{DDH} (Inputs at High)	3.3V at all Inputs	Vs+		4.42	10	mA
			Vs–	-10	-5.04		
			V_H		0.05	2	
			V_L	-5	-3.40		
I_{DD} (Dynamic)	I_{DD}, dynamic	0 to 3.3V square wave input with frequency of 5MHz , 50% duty cycle	Vs+		15	20	mA
			Vs–	-250	-189		
			V_H		183	250	
			V_L	-20	-16		

AC ELECTRICAL SPECIFICATIONS:

Test condition: Vs+ = V_H = 5V, V_L = Vs– = -5V, GND = 0V, T_A = 25ºC, unless otherwise specified

Table-11: AC Electrical Characteristics

Symbol	Parameter	Test Conditions	Typical	Units
T_R	Output rise time (10% to 90%)	0 to 3.3V square wave input with frequency of 5MHz , 50% duty cycle, C_L=1000pF	18.7	ns
T_F	Output fall time (90% to 10%)		17.9	ns
$t_{RF\Delta}$	t_R, t_F Mismatch		0.8	ns
t_{D+}	Turn-Off Delay Time		29	ns
t_{D-}	Turn-On Delay Time		32	ns
t_{DD}	t_{D-1} - t_{D-2} Mismatch		3	ns
t_{ENABLE}	Enable Delay Time		29	ns
$t_{DISABLE}$	Disable Delay Time		51	ns

TYPICAL PERFORMANCE CURVES:

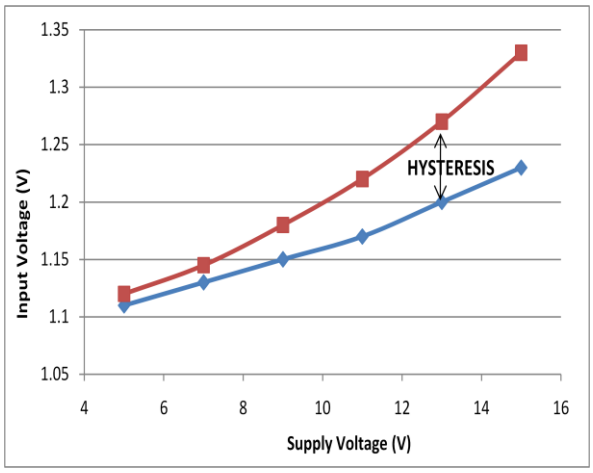


Figure-5: Switch Threshold vs Supply Voltage

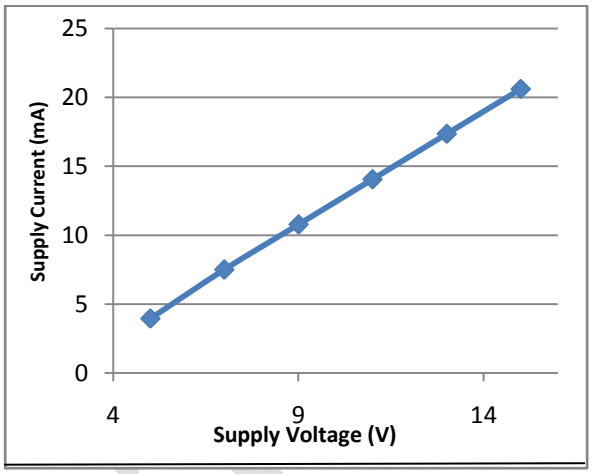


Figure-6: Vs+ Static Supply Current vs Supply Voltage

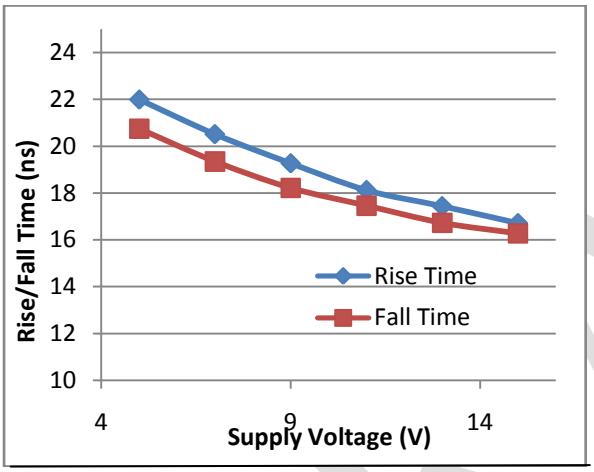


Figure-7: Rise/Fall Time vs Supply Voltage

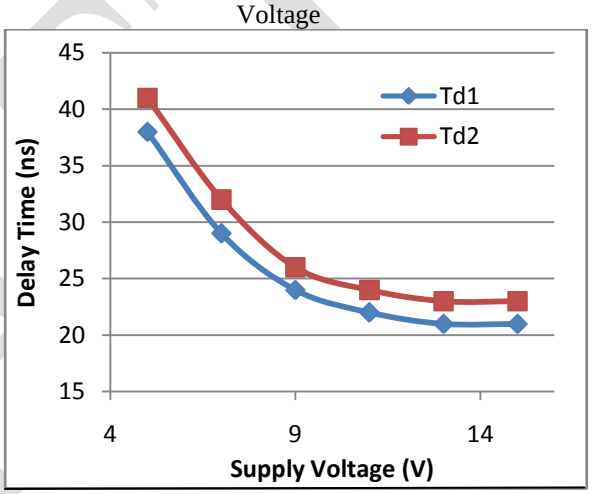


Figure-8: Propagation Delay vs Supply Voltage

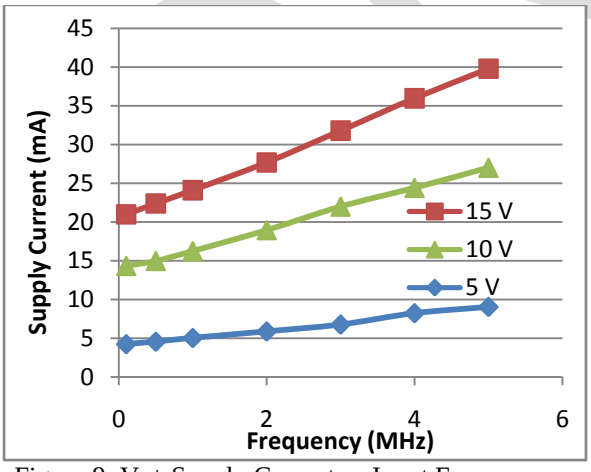


Figure-9: Vs+ Supply Current vs Input Frequency

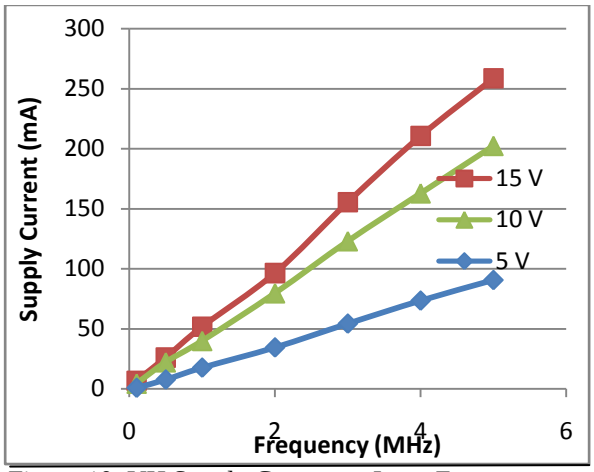


Figure-10: VH Supply Current vs Input Frequency

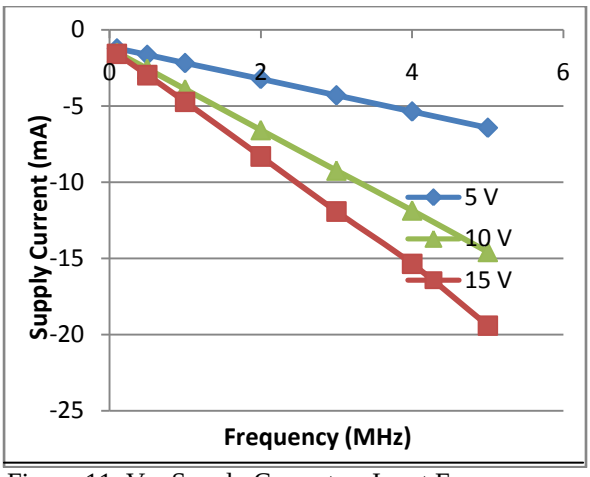


Figure-11: Vs- Supply Current vs Input Frequency

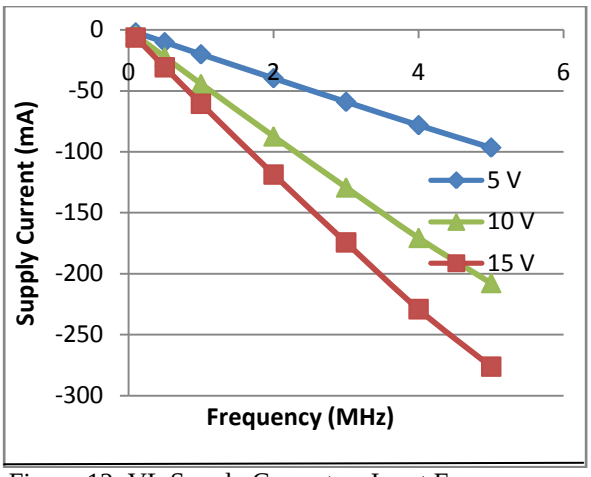


Figure-12: VL Supply Current vs Input Frequency

APPLICATIONS INFORMATION:

Product Description

The SCL clock driver is a high performance 5 MHz high speed quad driver. Each channel of the SCL clock driver consists of a single P-channel high side driver and a single N-channel low side driver. These low on resistance devices will pull the output (OUT_X) to either the high or low voltage, on V_H and V_L respectively, depending on the input logic signal (IN_X). It should be noted that there is only one set of high and low voltage pins.

A common output enable (OE) pin is available on the SCL clock driver. This pin, when pulled low will put all outputs in to the high impedance state.

The SCL clock driver is available in Hermetic sealed 16 pin Lead Flat package (SOP). The relevant package should be chosen depending on the calculated power dissipation.

Supply Voltage Range and Input Compatibility

The SCL clock driver is designed for operation on supplies from 5V to 15V. The table 4 shows the specifications for the relationship between the V_{S+}, V_{S-}, V_H, V_L, and GND pins. The SCL clock driver does not contain a true analog switch and therefore V_L should always be less than V_H.

All input pins are compatible with both 3V and 5V CMOS signals. With a positive supply (V_{S+}) of 5V, the SCL clock driver is also compatible with TTL inputs.

Power Supply Bypassing

When using the SCL clock driver, it is very important to use adequate power supply bypassing. The high switching currents developed by the SCL clock driver necessitate the use of a bypass capacitor on both the positive and negative supplies. It is recommended that a 4.7μF tantalum capacitor be used in parallel with a 0.1μF low-inductance ceramic capacitor. These should be placed as close to the supply pins as possible. It is also recommended that the V_H and V_L pins have some level of bypassing, especially if the SCL clock driver is driving highly capacitive loads.

Power Dissipation Calculation

When switching at high speeds, or driving heavy loads, the SCL clock driver drive capability is limited by the rise in die temperature brought about by internal power dissipation. For reliable operation die temperature must be kept below T_{JMAX} (125°C). It is necessary to calculate the power dissipation for a given application prior to selecting package type.

Power dissipation may be calculated:

$$PD = (V_S \times I_S) + \sum_{1}^{4} (C_{INT} \times V_S^2 \times f) + (C_L \times V_{OUT}^2 \times f)$$

where:

V_S is the total power supply to the SCL clock driver (from V_{S+} to V_{S-})
V_{OUT} is the swing on the output (V_H - V_L)
C_L is the load capacitance
C_{INT} is the internal load capacitance (80pF max)
I_S is the quiescent supply current (3mA max)
f is frequency

Having obtained the application's power dissipation, the maximum junction temperature can be calculated:

$$T_{JMAX} = T_{MAX} + \Theta_{JA} \times PD$$

Where:

T_{JMAX} is the maximum junction temperature (125°C)
T_{MAX} is the maximum ambient operating temperature
P_D is the power dissipation calculated above
θ_{JA} is the thermal resistance, junction to ambient, of the application (package + PCB combination).

APPLICATION DIAGRAM:

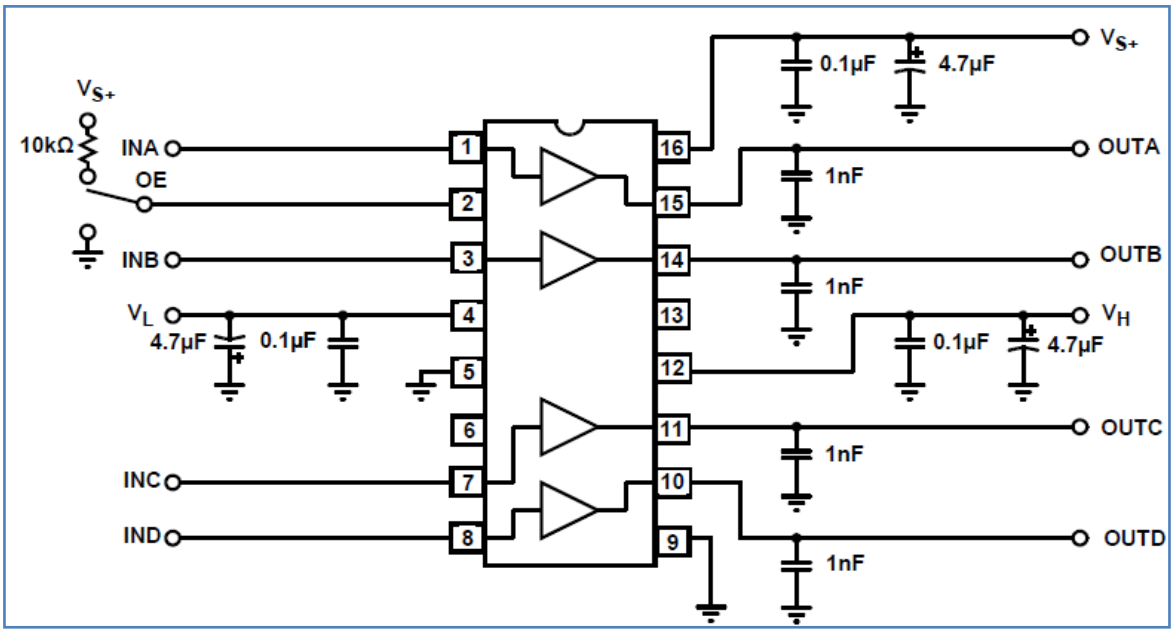


Figure-13: Application Diagram

PACKAGE DRAWING (CERAMIC-LEAD-FLATPACK):

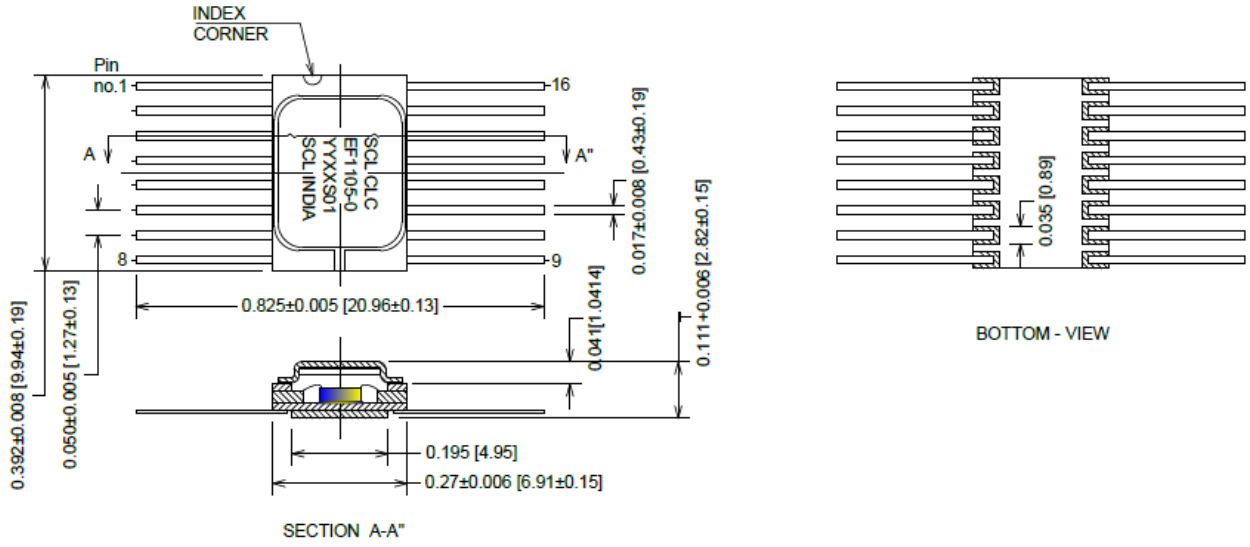


Figure-14: Package Device Drawing

NOTE: All linear dimensions are in inches (mm.)