SC1235-0T2

PRELIMINARY DATASHEET

August 2022

Voltage Supervisory Circuit (RADIATION HARDENED)

FEATURES:

- **Radiation Hardness**
- **High Dose rate ……150krad(Si)**
- **SEL/SEU/SET…….70MeV.cm^2/mg**
- **Analog Supply Voltage is 3.3V**
- **Precision Supply Voltage Monitor**
- **3.1 V Threshold**
- **178ms (typical) Reset Pulse Width**
- **Independent watchdog timer with 1.6s(typical) timeout**
- **Precision threshold detector**
- **0.61V threshold**
- **Operating Temperature: -55ºC to +125ºC.**
- **Low Power Dissipation.**
- **Packaged in 8-Pin CFP package.**
- **SCL 0.18µ CMOS technology.**

DESCRIPTION:

SC1235-0T2 is a radiation hardened 3.3V Supervisory circuits that reduce the complexity required to monitor supply voltages in microprocessor systems. These devices significantly improve accuracy and reliability relative to discrete solutions. This device has following key functions

• A reset output during power-up, power down and brownout conditions

• An independent watchdog output that goes low if the watchdog input has not been triggered within 1.6Sec (typical).

• A precision threshold voltage detector for monitoring a power supply other than V_{DD}.

• An active-low, manual-reset input.

APPLICATIONS:

- **Supervisor for µ-processors, µ-controllers, FPGAs and DSPs.**
- **Critical Power Supply monitoring**
- **Reliable replacement of discrete solutions**

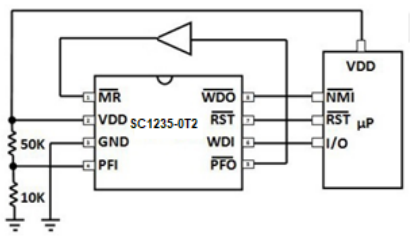
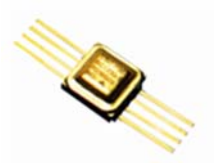


Figure 1: Application Circuit



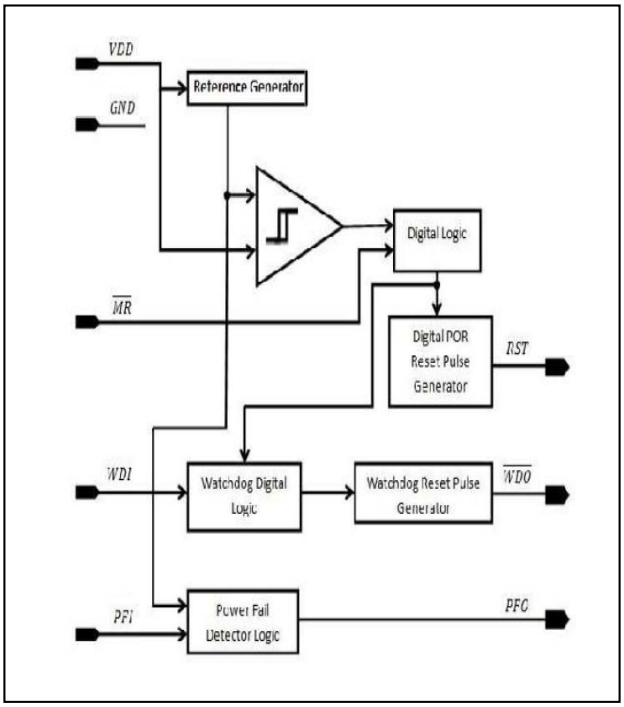


Figure 2: Block Diagram

PIN CONFIGURATION:

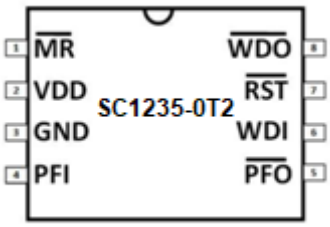


Figure 3: Pin Diagram

PIN DESCRIPTIONS:

PIN NO.	NAME	TYPE	DESCRIPTION
1	MR	Input	Manual Reset, MR is an active-low, Debounced , TTL/CMOS compatible input that can be used to trigger a reset pulse
2	VDD	Input	Power Supply, VDD is a supply voltage input that provides power to all internal circuitry. This input is also monitored and used to trigger a reset pulse.
3	GND	Input	Ground, GND is a supply voltage return for all internal circuitry. This return establishes the reference level for voltage detection and should be connected to signal ground.
4	PFI	Input	Power fail Input, PFI is an input to a threshold detector which can be used to monitor another supply voltage level. The threshold of the detector (VPFI) is 0.61V
5	PFO	Output	Power Fail Output, PFO is an active low, Push-Pull Output of a threshold detector that indicated the voltage at the PFI pin is less than VPFI.
6	WDI	Input	Watchdog Input, WDI is a tri-state input that monitors microprocessor activity.
7	RST	Output	Reset, RST is an active-low. As V_{DD} rises, RST stays low. When V_{DD} rises above a 3.1V reset threshold, an internal time releases RST after 178ms. RST pulses low whenever V_{DD} goes below the reset threshold.
8	WDO	Output	Watchdog Output, WDO is an active-low , push pull output that goes low if the microprocessor does not toggle WDI within 1.6s and WDI is not tri-stated WDO is usually connected to the non-mask able interrupt input of a microprocessor.

Table1: Pin Description

TIMING SPECIFICATIONS:

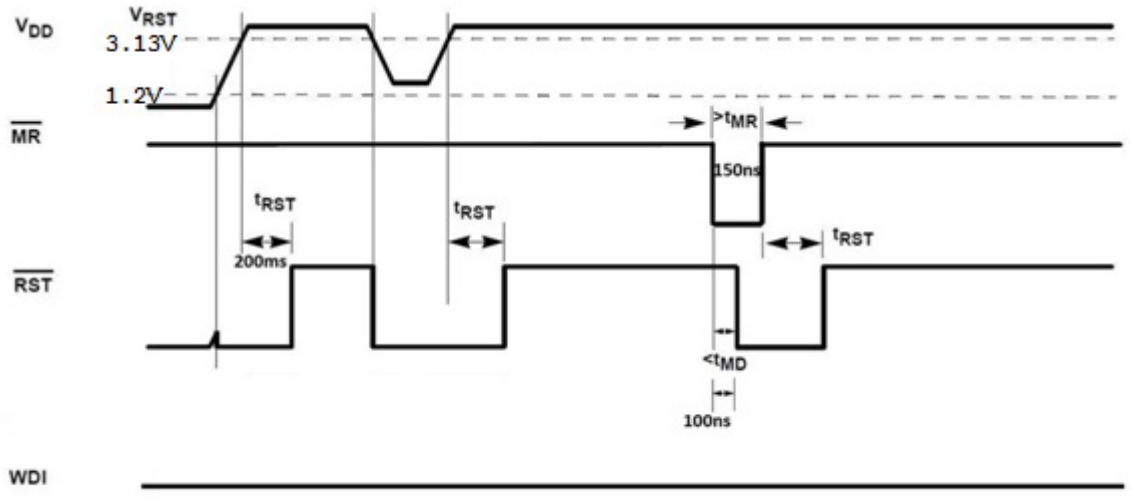


Figure4: RST, MR timing diagram

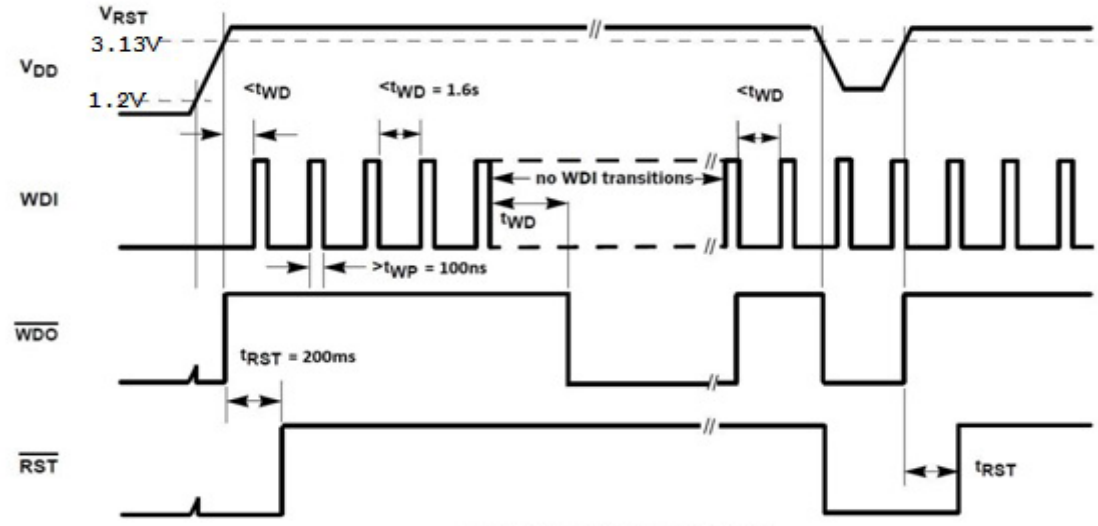


Figure5: Watchdog timing diagram

ELECTRICAL CHARACTERISTICS

All Specifications VDD= +3.3V, Temp. = 25ºC, unless otherwise specified.

PARAMETER	SYMBOL	TESTS CONDITIONS	SC1235-0T2			UNITS
			MIN	TYP	MAX	
POWER SUPPLY						
Supply Voltage	VDD		3.00	3.3	3.6	V
Supply Current	IDD	Static	450	500	750	µA
RESET						
Reset Threshold Voltage, Rising	V_{RST}, Rising		3.08	3.10	3.12	V
Reset Threshold Voltage, Falling	V_{RST}, Falling		3.04	3.05	3.08	V
Reset Threshold Voltage, Hysteresis	V_{RST}, Hyst		30	50	70	mV
Reset Pulse Width	t_{RST}		165	178	215	ms
Reset Output Voltage	V_{OUT}	I_{SOURCE} = 500µA	3.0	3.2	3.3	mV
		I_{SINK} = 1.2 mA		70	150	mV
WATCHDOG TIMER						
Watchdog Time-out period	t_{WD}		1.3	1.61	1.67	S
Watchdog Input Current	I_{WDI}		-5		5	µA
Watchdog output Voltage	V_{WDO}	I_{SOURCE} = 500µA	3.0	3.28	3.3	V
	V_{WDO}	I_{SINK} = 1.2mA		70	150	mV
MANUAL RESET						
Manual Reset pulse width	t_{MR}	MR =0V	50	150		ns
Manual Reset to Reset output delay	t_{MD}			5	100	ns
Manual Reset Pull-Up Current	I_{MR}		-10		10	nA
Reset output	V_{RST}	MR =V_{DD}	3.26	3.278	3.29	V
	V_{RST}	MR = 0V		50	100	mV
THRESHOLD DETECTOR						
Power fail input threshold voltage	V_{PFI}		0.60	0.61	0.62	V
Power fail input threshold current	I_{PFI}		2	3.5	5	nA
Power fail output voltage	V_{PFO}	I_{SOURCE} = 500µA	3.0	3.27	3.3	V
		I_{SINK} = 1.2mA		50	100	mV
PFI Rising Threshold to PFO Delay	t_{RPFI}			7	20	µs
PFI Falling Threshold to PFO Delay	t_{FPFI}			7	40	µs
PFI Input Current	I_{PFI}		-1		1	µA
TEMPERATURE RANGE						
Operating			-55		125	ºC
TOTAL IONIZE DOSE		Upto 150KRad		Pass		
SINGLE EVENT EFFECT						
Single Event Latch up		Upto 70 LET (MeV-cm^2/mg)		Pass		
Single Event Transient		Upto 70 LET (MeV-cm^2/mg)		Pass		

TYPICAL PERFORMANCE CURVES

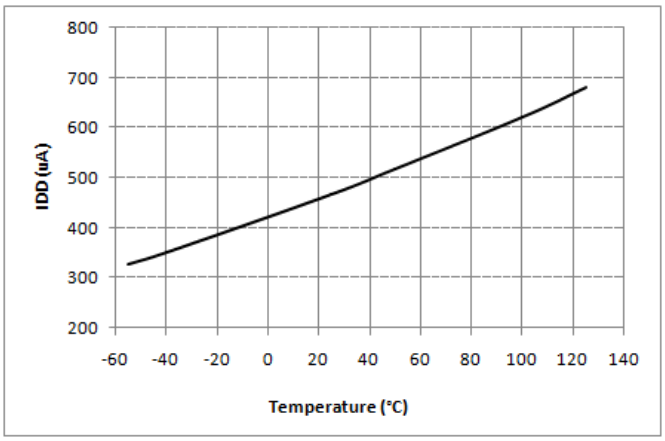


Figure 6: I_{DD} versus Temperature

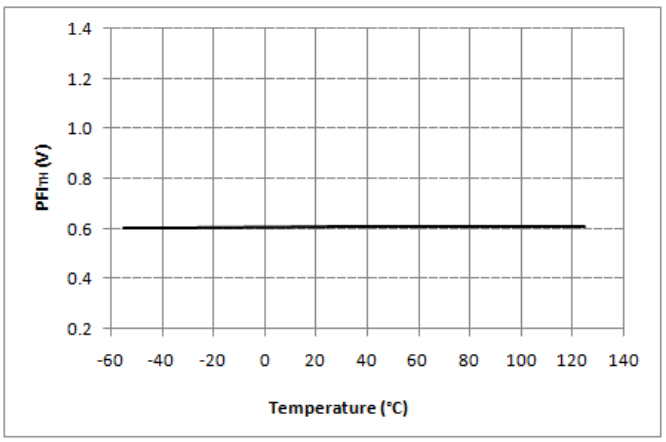


Figure 7: V_{PFI} versus Temperature

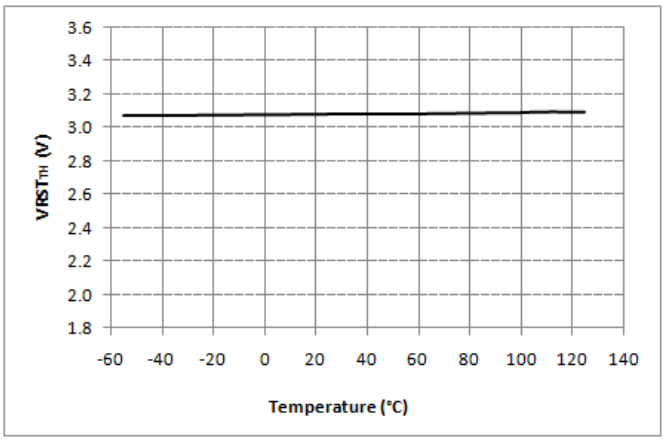


Figure 8: V_{RST} versus Temperature

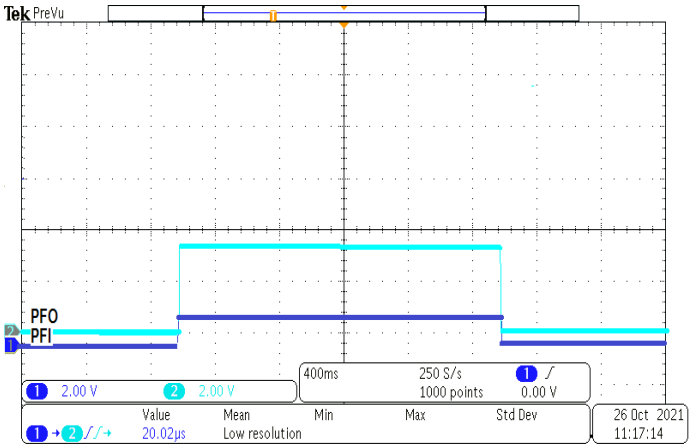


Figure 9: PFI to PFO Response

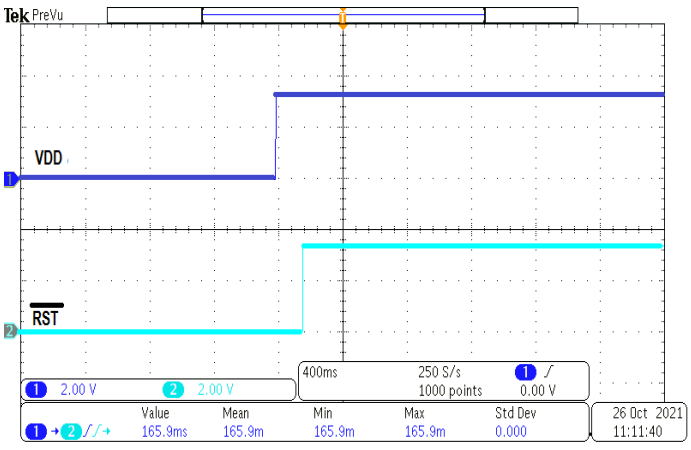


Figure 10: VDD to RST Assertion

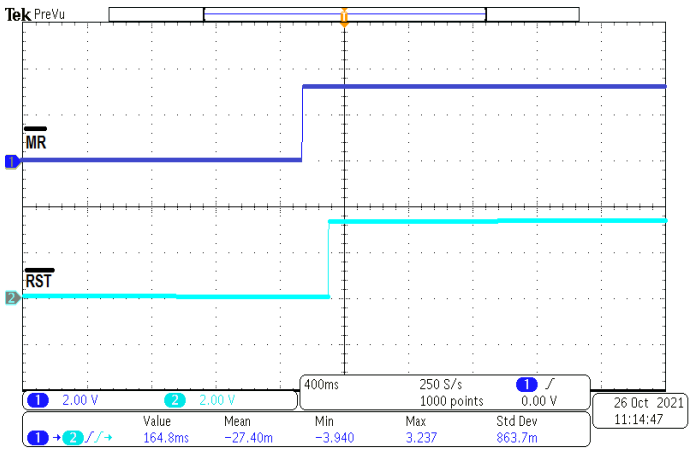


Figure 11: MR to RST Assertion

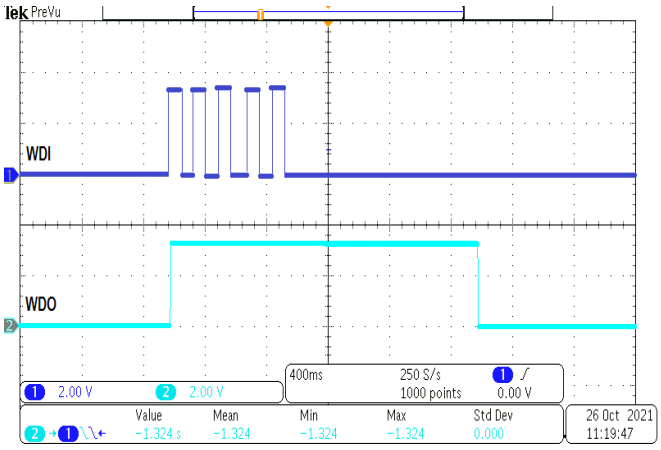


Figure 12: WDI to WDO Response

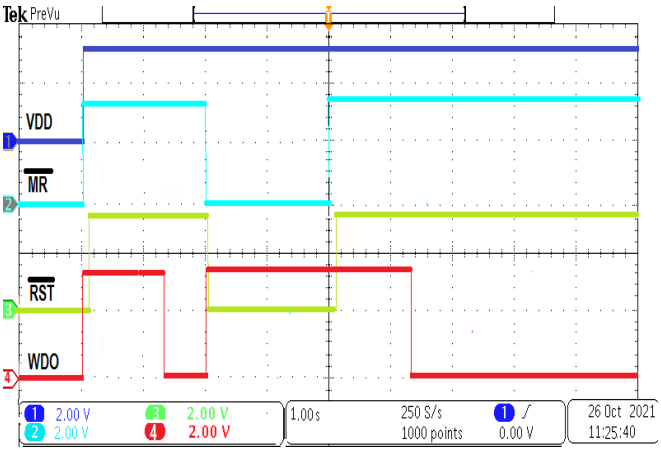
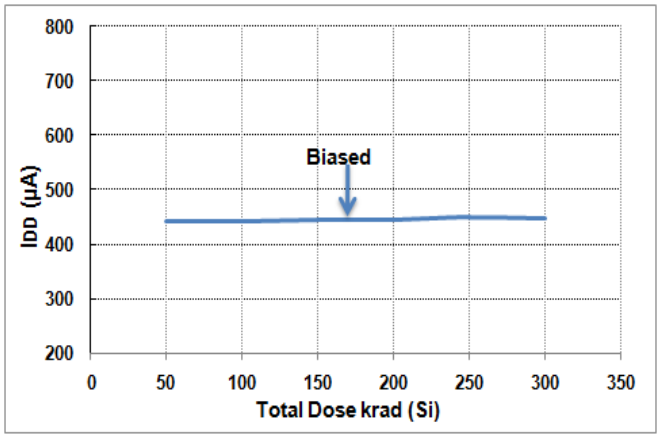
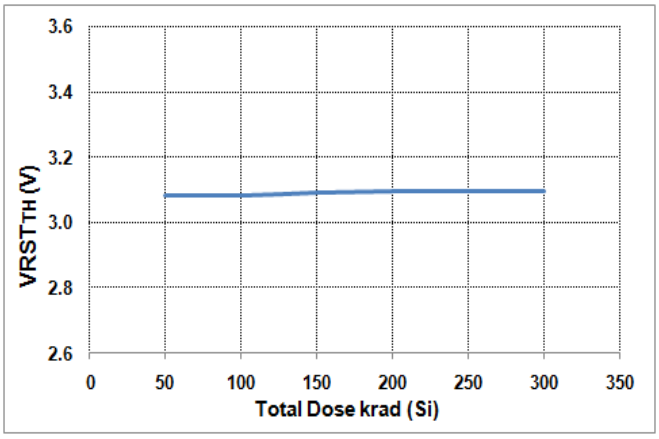


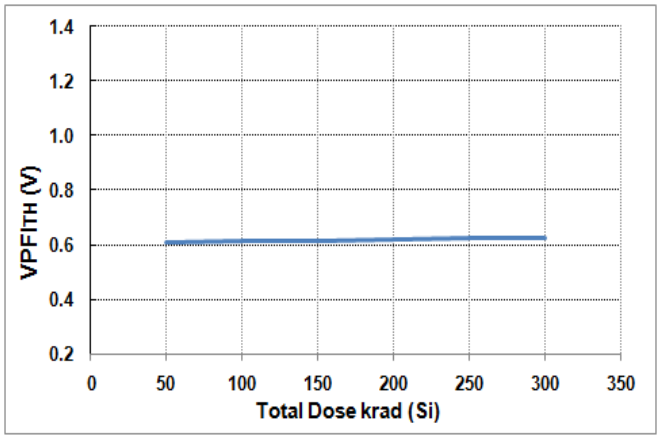
Figure 13: Start-Up to Reset, Manual Reset and WDO Function

POST RADIATION CHARACTERISTICS

unless otherwise specified, VDD = 3.3V, TA = +25°C. This data is typical mean test data post radiation exposure at a rate of 190 rad (Si)/s.







DIGITAL CHARACTERISTICS

DVDDO= 3.0 V to 3.6V

PARAMETER	TESTS CONDITIONS	SC1235-0T2			UNITS
		MIN	TYP	MAX	
Logic Family			CMOS		
Logic Level: V_{IH}		2		VDD	V
V_{IL}		GND		0.8	V
V_{OH}	I_{OH}=8mA	3.0			V
V_{OL}	I_{OL}=8mA	GND		0.4	V

ABSOLUTE MAXIMUM RATING

PARAMETER	SC1235-0T2		UNITS
	MIN	MAX	
VDD to GND	-0.3	4.3	V
Digital Input Voltage to GND	-0.3	VDD+0.3	V
Digital Output Current		8	mA
Maximum Ambient Temperature		125	°C

THERMAL INFORMATION

PARAMETER	SC1235-0T2		UNITS
	MIN	MAX	
Theta jc		13.96	°C/W
Storage Temperature	-65	150	°C
Junction Temperature		175	°C

OVERVIEW

The SC1235-0T2 provides the functions needed for monitoring critical voltages in high reliability applications such as microprocessor systems. Functions of these supervisors include power-on reset control, supply voltage supervisions, power-fail detection, manual-reset assertion, and a watchdog timer. The integration of these functions along with their high threshold accuracy, low power consumption, and radiation tolerance make these devices ideal for critical supply monitoring.

RESET OUTPUT

Reset control has long been a critical aspect of embedded control design. Microprocessors require a reset signal during power-up to ensure that the system environment is stable before initialization.

The reset signal provides several benefits:

- It prevents the system micro-processor from starting to operate with insufficient voltage.
- It prevents the processor from operating before stabilization of the oscillator.
- It ensures that the monitored device is held out of operation until internal registers are initialized.
- It allows time for an FPGA to perform its self-configuration before initialization of the circuit.

When VDD rises above the reset threshold (V_{RST}), an internal timer releases RST after 178 ms (typical). RST pulses low whenever VDD degrades to below VRST. If a brownout condition occurs in the middle of a previously initiated reset pulse, the pulse is lengthened 178 ms (typical).

POWER FAILURE MONITOR

Besides monitoring VDD for reset control, these devices have a Power Failure Monitor feature that supervises an additional critical voltage on the Power-Fail Input (PFI) pin. For example, the PFI pin could be used to provide an early power-fail warning, overvoltage detection, or monitor a power supply other than VDD. PFO goes low whenever PFI is less than V_{PFI}. The threshold detector can be adjusted using an external resistor divider network to provide custom voltage monitoring for voltages greater than V_{PFI}, according to Equation 1.

$$\mathrm{VIN} = \mathrm{VPFI} * \frac{\mathrm{R1+R2}}{R2} \qquad \text{..... (Eq.1)}$$

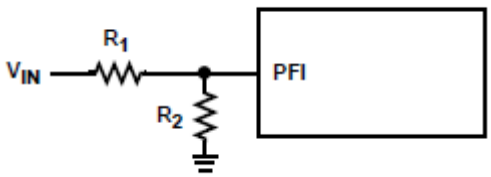


Figure 6: Custom VTH with Resistor Divider circuit on PFI

Note: Hysteresis for the comparator used for Power Failure detector can be modified externally by adding positive feedback to the circuit.

MANUAL RESET

The manual reset input (MR) allows designers to add manual system reset capability using a push button switch. The MR input is an active low de-bounced input which asserts reset if the

MR pin is pulled low to less than V_{IL} for at least 50ns.

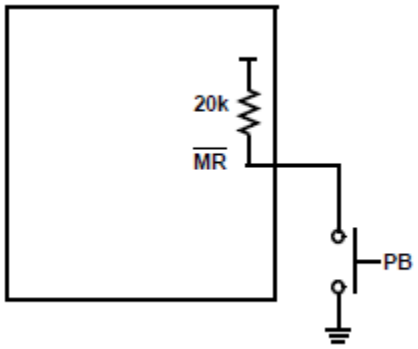


Figure 7: Connecting Push Button to MR

After MR is released, the reset output remains asserted for tRST and then released. An internal pull-up resistor is placed between MR Pin and VDD pin to limit current when MR pin is pulled low.

WATCHDOG TIMER

The watchdog time circuit checks for coherent program execution by monitoring the WDI pin. If the processor does not toggle the watchdog input within t_{WD}, WDO will go low. Whenever there is a low-voltage V_{DD} condition, WDO goes low. Unlike the reset outputs, however, WDO goes high as soon as V_{DD} rises above its voltage trip point .With WDI open or connected to a tri-stated high impedance input, the watchdog timer is disabled and only pulls low when $V_{DD} < V_{RST}$.

APPLICATION:

Special considerations:

Using decoupling capacitor between power supply rails will prevent unwanted glitches, droops in supply voltage and noise due to switching which can cause unwanted resets. If the PFI input transition is less than the delay, the PFO pin will not change its states.

Overvoltage Sensing Application:

This device can be used to sense over voltage. Values of R1 and R2 to be select such that V_{PFI} remains less than 0.61V during normal supply (V_{DD}=3.3V).

Select R1 =50kΩ and V_{PFI} =0.55V, R2 can be calculated from Equation 2.

$$VPFI = VDD(\frac{R2}{R1+R2}) \ldots\ldots\ldots\ldots \text{(Eq.2)}$$

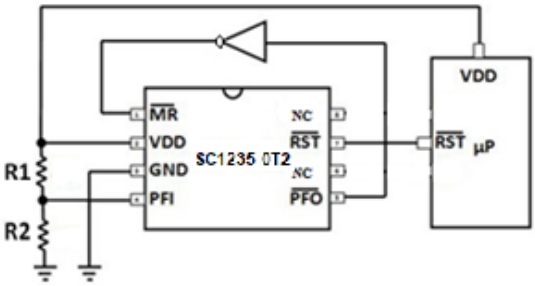


Figure8: Over Voltage Sensing Application

In normal supply (V_{DD}), PFO output will remain low and MR will be high. When V_{PFI} reach ≥0.61V, PFO will go high which reset µP thru MR. The over voltage sensing point can be calculated as follows

$$VDD\ OVER = VPFI(\frac{R1 + R2}{R2})$$

With VPFI =0.61V, R1 =50KΩ and R2 =10KΩ, the over voltage sensing point is 3.66V.

Adding Hysteresis to PFI Comparator:

The PFI comparator has no built-in hysteresis. The user can add hysteresis by connecting a resistor between PFO and PFI pin as shown

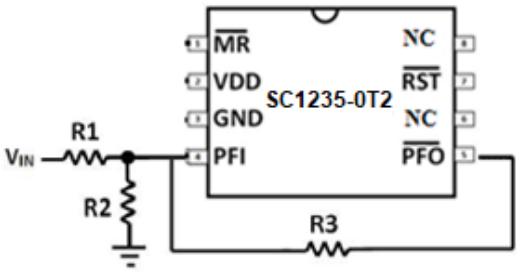


Figure9: Positive Feedback for Hysteresis

The Value of R3 can be calculated as follows.

I_{R3}= V_{PFI}/R_3, When PF is Low ……Eq.3

I_{R3}= (V_{DD}-V_{PFI})/R_3, When PFO is high…Eq.4

The feedback current needs to be very small so it does not induce oscillations; 200nA is ok. Now two values of R_3 can be calculated with V_{DD}= 3.3V and V_{PFI}=0.61V from Eq.1 and Eq.2

R3 =3.05MΩ or 13.45MΩ

Select the lowest value i.e. R3 =3.05MΩ.

With V_{HB} =100mV selected, R1 can be calculated as follows

$$R_1 = R_3\ (\frac{VHB}{VDD}) = 92k\Omega \ldots \text{Eq.5}$$

Then next step is select the rising trip voltage (V_{TR}) such that:

$V_{TR} > V_{PDI} (1+\frac{VHB}{VDD})$ Eq.6

The rising threshold voltage (V_{TR}) is selected at 2.0V and R2 is calculated by Eq. 6,

$R2 = 1/ [(\frac{VTR}{VPFIXR1})-(\frac{1}{R1})-(\frac{1}{R3})]$ …Eq.7

By solving Eq.6, R_2 yield 40.9kΩ.

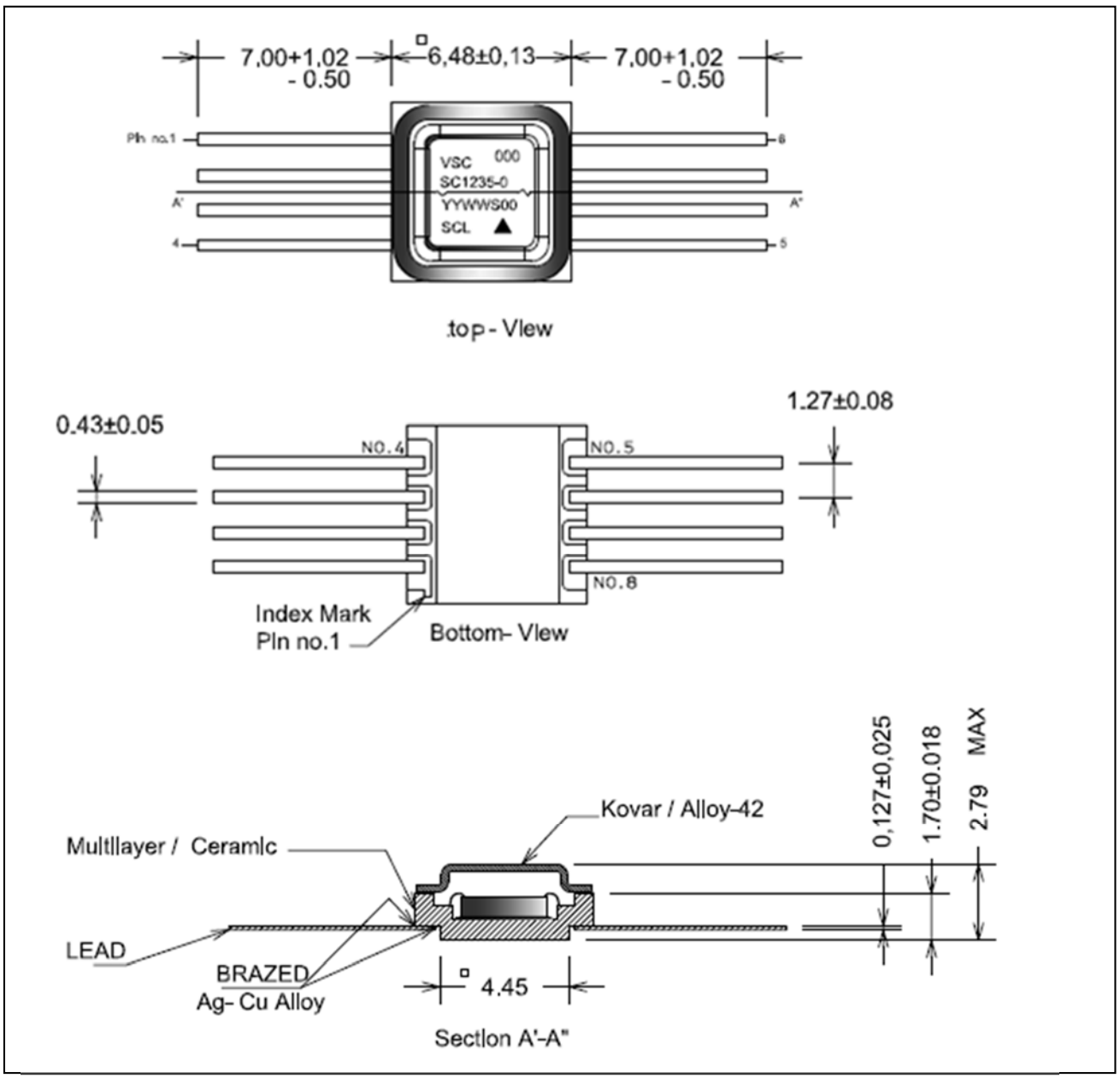
The Falling threshold voltage, V_{TF} Can be calculated as follows

$V_{TF} = V_{TR} – (\frac{R1 \times VDD}{R3}) = 1.9V$…Eq.8

So 100mV hysteresis is achieved.

PACKAGE INFORMATION

8-PIN CFP



NOTES: All linear dimensions are in millimetres.

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