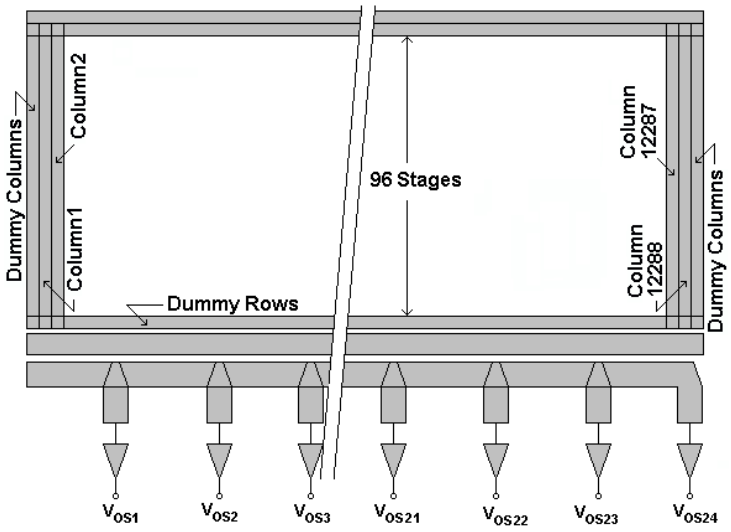
12288 PIXELS VISIBLE CCD TDI IMAGER (PRELIMINARY)

- **8µm × 8µm pixel size**
- **8µm pixel pitch**
- **Maximum 96 integration stages**
- **Variable number of integration stages**
- **Twenty-four outputs for fast readout**
- **Cascading feature for reduced number of outputs**

Device Description:

The SC3928 is a high resolution, high data rate, 12288 pixels visible TDI linear imager. Each pixel consists of 96 stages of CCD (photo-gate) sensors for charge integration. There are twenty-four readout shift registers for high data rate.



The parallel shift registers are of 4-phase N-buried channel type, serving the multiple purposes of photo-detection, charge integration and charge transfer. For a particular rate of transfer in the parallel shift register, the integration can be varied using 2, 8 or 32 stages instead of all the 96. This is done by applying appropriate clock signals to the corresponding pins.

The read-out shift registers, like the parallel shift registers, are of 4-phase N-buried channel type. The signal from 512 photo-sensitive elements associated with each read-out shift register is read out of each of the twenty-four outputs. At each output channel, the signals corresponding to 10 dummy pixels arrive first, followed by those from the photo-sensitive pixels. Signal charge from multiple (2, 4, 8 or 24) read-out shift registers may be read out through a single output by employing the cascading feature, which is done by applying appropriate clock signals. This reduces the number of outputs. The output signals may be processed to reconstruct the image.

Each output section comprises a floating diffusion charge detection node, a reset transistor and a two-stage N-buried channel source follower amplifier.

Pin Descriptions:

The device pins may be grouped according to their functions.

Parallel shift register:

The parallel shift register has been divided into four sections as per the requirements of stage selection. Each section has independent transport clock inputs of four phases each and all but the last have a stage selection clock input to allow operation as a transport or as a blocking gate. The charge from the unselected stages are dumped in a gated drain. Finally, at the interface between the parallel and the serial shift registers is the parallel to serial transfer clock.

Transport clocks (Φ_{VXY} : where X denotes the phase and Y denotes the segment)
Stage Selection Clocks (Φ_{SSX} : where X denotes the segment)
Stage Selection Gate (V_{SSG})
Stage Selection Drain (V_{SSD})
Parallel Shift Register Terminal Clock (Φ_{V4T})
Parallel to Serial Transfer Clock (Φ_{VH})

Serial shift register:

There are twenty-four serial read-out shift registers. These have been divided into two sections, with transport clocks of four phases for both. The cascading feature requires two more clocks, the cascade clock and the tap clock. There are four pins of each.

Transport clocks (Φ_{HXY} : where X denotes the phase and Y denotes the section)
Cascade clocks (Φ_{HCX}: where X is the serial letter for identifying the shift registers being cascaded)
Tap clocks (Φ_{HTX}: where X is the serial letter based on function of the pin)

Output section and peripherals:

There is a single output gate pin. There are four pins each of the reset gate and the reset drain. Based on the requirement of cascading the amplifier drain pins (bias pins corresponding to unused outputs need not be powered) have been divided into eight groups. There are twenty-four output pins and amplifier source bias pins. Finally, there are the substrate pins and a pin for powering heat dissipation elements on-chip.

Output gate (V_{GS})
Reset gate (Φ_{RX}: where X is A, B, C or D)
Reset drain (V_{DRX}: where X is A, B, C or D)
Amplifier drain bias (V_{DDX}: where X may be from A to H)
Device output (V_{OSX}: where X is a number between 1 and 24)
Amplifier source biases (V_{SX}: where X is a number between 1 and 24)
Heat dissipation bias (V_{HD})
Substrate bias (V_{SS})

Table 1: Pin descriptions (sorted by pin function).

a) PARALLEL SHIFT REGISTER

1. Transport Clocks					
Stage	**Phase 1**	**Phase 2**	**Phase 3**	**Phase 4**	**Stage Sel.**
96-34	Φ_{V1D} [D16]	Φ_{V2D} [C13]	Φ_{V3D} [D18]	Φ_{V4D} [D10]	-
33				-	Φ_{SC} [D08]
32-10	Φ_{V1C} [D15]	Φ_{V2C} [C12]	Φ_{V3C} [C18]	Φ_{V4C} [C10]	-
9				-	Φ_{SB} [D07]
8-4	Φ_{V1B} [D14]	Φ_{V2B} [D12]	Φ_{V3B} [C17]	Φ_{V4B} [C09]	-
3				-	Φ_{SA} [C07]
2-1	Φ_{V1A} [C14]	Φ_{V2A} [D11]	Φ_{V3A} [C16]	Φ_{V4A} [D09]	-
2. Stage Selection Gate					V_{SSG} [D05]
3. Stage Selection Drain					V_{SSD} [C05]
4. Parallel Shift Register Terminal Clock					Φ_{V4T} [C06]
5. Parallel to Serial Transfer Clock					Φ_{VH} [D04]

b) SERIAL SHIFT REGISTER

Pins	**Readout register number**																							
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
Φ_{H1A} [B04]	■	■	■	■	■	■	■	■	■	■	■	■												
Φ_{H2A} [B03]	■	■	■	■	■	■	■	■	■	■	■	■												
Φ_{H3A} [A03]	■	■	■	■	■	■	■	■	■	■	■	■												
Φ_{H4A} [B02]	■	■	■	■	■	■	■	■	■	■	■	■												
Φ_{H1B} [B33]													■	■	■	■	■	■	■	■	■	■	■	■
Φ_{H2B} [B34]													■	■	■	■	■	■	■	■	■	■	■	■
Φ_{H3B} [A34]													■	■	■	■	■	■	■	■	■	■	■	■
Φ_{H4B} [B35]													■	■	■	■	■	■	■	■	■	■	■	■
Φ_{HTA} [D01], Φ_{HCA} [D36]	■		■		■		■		■		■		■		■		■		■		■		■	
Φ_{HTB} [D02], Φ_{HCB} [D35]		■				■				■				■				■				■		
Φ_{HTC} [D03], Φ_{HCC} [D34]				■								■								■				
Φ_{HTD} [C03], Φ_{HCD} [C34]								■								■								

c) OUTPUT SECTION AND PERIPHERALS

Pins	Readout register number																							
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
Φ_{RA} [A01],V_{DRA} [C01]																								
Φ_{RB} [B01],V_{DRB} [C02]																								
Φ_{RC} [A36],V_{DRC}[C36]																								
Φ_{RD} [B36],V_{DRD} [C35]																								
V_{DDA} [A04]																								
V_{DDB} [A05]																								
V_{DDC} [A06]																								
V_{DDD} [B06]																								
V_{DDE} [A33]																								
V_{DDF} [A32]																								
V_{DDG} [A31]																								
V_{DDH} [B31]																								
V_{OS01} to V_{OS24}	A07	A08	A09	A10	A11	A12	A13	A14	A15	A16	A17	A18	A19	A20	A21	A22	A23	A24	A25	A26	A27	A28	A29	A30
V_{S01} to V_{S24}	B07	B08	B09	B10	B11	B12	B13	B14	B15	B16	B17	B18	B19	B20	B21	B22	B23	B24	B25	B26	B27	B28	B29	B30
V_{HD} [B05]																								
V_{SS} [A02], [A35], [C08], [C11], [C15], [D06], [D13] & [D17]																								

The following pins are not connected: A0, A37, B0, B32, B37, C0, C19 – C32, C37, D0, D19 – D33 and D37.

Table 2: Pin Descriptions (sorted by pin number)

Pin No.	Pin symb.
A01	Φ_{RA}
A02	V_{SS}
A03	Φ_{H3A}
A04	V_{DDA}
A05	V_{DDB}
A06	V_{DDC}
A07	V_{OS1}
A08	V_{OS2}
A09	V_{OS3}
A10	V_{OS4}
A11	V_{OS5}
A12	V_{OS6}
A13	V_{OS7}
A14	V_{OS8}
A15	V_{OS9}
A16	V_{OS10}
A17	V_{OS11}
A18	V_{OS12}
A19	V_{OS13}
A20	V_{OS14}
A21	V_{OS15}
A22	V_{OS16}
A23	V_{OS17}
A24	V_{OS18}
A25	V_{OS19}
A26	V_{OS20}
A27	V_{OS21}
A28	V_{OS22}
A29	V_{OS23}
A30	V_{OS24}
A31	V_{DDG}
A32	V_{DDF}
A33	V_{DDE}
A34	Φ_{H3B}
A35	V_{SS}
A36	Φ_{RC}

Pin No.	Pin symb.
B01	Φ_{RB}
B02	Φ_{H4A}
B03	Φ_{H2A}
B04	Φ_{H1A}
B05	V_{HD}
B06	V_{DDD}
B07	V_{S1}
B08	V_{S2}
B09	V_{S3}
B10	V_{S4}
B11	V_{S5}
B12	V_{S6}
B13	V_{S7}
B14	V_{S8}
B15	V_{S9}
B16	V_{S10}
B17	V_{S11}
B18	V_{S12}
B19	V_{S13}
B20	V_{S14}
B21	V_{S15}
B22	V_{S16}
B23	V_{S17}
B24	V_{S18}
B25	V_{S19}
B26	V_{S20}
B27	V_{S21}
B28	V_{S22}
B29	V_{S23}
B30	V_{S24}
B31	V_{DDH}
B32	–
B33	Φ_{H1B}
B34	Φ_{H2B}
B35	Φ_{H4B}
B36	Φ_{RD}

Pin No.	Pin symb.
C01	V_{DRA}
C02	V_{DRB}
C03	Φ_{HTD}
C04	V_{GS}
C05	V_{SSD}
C06	Φ_{V4T}
C07	Φ_{SA}
C08	V_{SS}
C09	Φ_{V4B}
C10	Φ_{V4C}
C11	V_{SS}
C12	Φ_{V2C}
C13	Φ_{V2D}
C14	Φ_{V1A}
C15	V_{SS}
C16	Φ_{V3A}
C17	Φ_{V3B}
C18	Φ_{V3C}
C19	-
C20	-
C21	-
C22	-
C23	-
C24	-
C25	-
C26	-
C27	-
C28	-
C29	-
C30	-
C31	-
C32	-
C33	V_{SS}
C34	Φ_{HCD}
C35	V_{DRD}
C36	V_{DRC}

Pin No.	Pin symb.
D01	Φ_{HTA}
D02	Φ_{HTB}
D03	Φ_{HTC}
D04	Φ_{VH}
D05	V_{SSG}
D06	V_{SS}
D07	Φ_{SB}
D08	Φ_{SC}
D09	Φ_{V4A}
D10	Φ_{V4D}
D11	Φ_{V2A}
D12	Φ_{V2B}
D13	V_{SS}
D14	Φ_{V1B}
D15	Φ_{V1C}
D16	Φ_{V1D}
D17	V_{SS}
D18	Φ_{V3D}
D19	-
D20	-
D21	-
D22	-
D23	-
D24	-
D25	-
D26	-
D27	-
D28	-
D29	-
D30	-
D31	-
D32	-
D33	-
D34	Φ_{HCC}
D35	Φ_{HCB}
D36	Φ_{HCA}

The following pins are not connected: A0, A37, B0, B32, B37, C0, C19 – C32, C37, D0, D19 – D33 and D37.

DC Characteristics:

Table 3 : DC Operating Characteristics :

Parameters	Symbol	Value			Units
		Min	Typical	Max	
Stage selection gate DC bias	V_{SSG}	0.5	1	2	V
Stage selection drain	V_{SSD}	13	13.5	14	V
Output gate DC bias	V_{GS}	0.5	1	2	V
Reset drain DC bias	V_{DR}	13	13.5	14	V
Output amplifier drain supply	V_{DD}	15	18	19	V
Output amplifier source supply	V_S	0	0	0	V
Substrate bias	V_{SS}	0	0	0	V

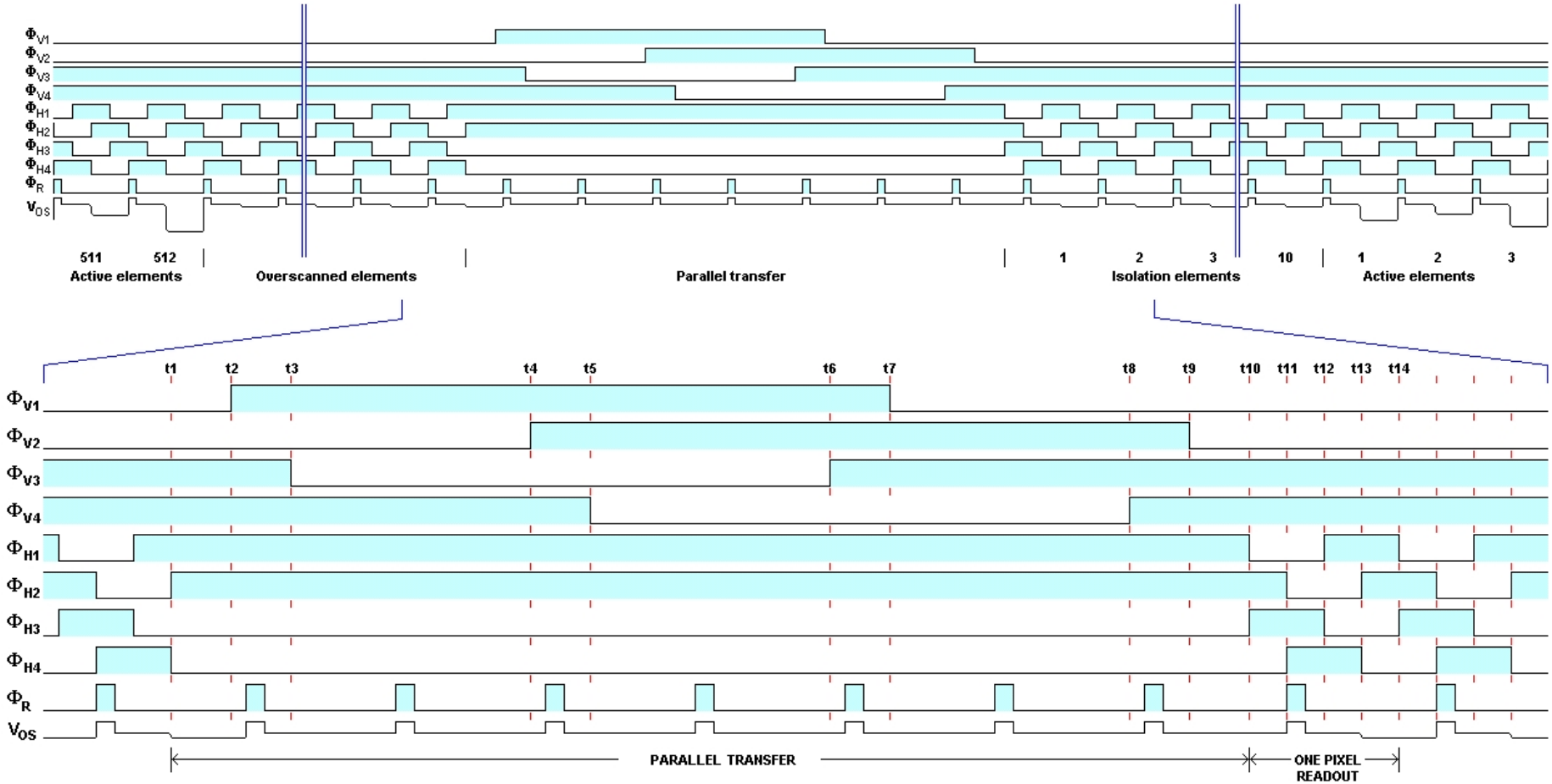
Clock characteristics:

Figure 2 shows the timing relationships of the different clock inputs to the device. The timing details are enumerated in table 4 and the clock characteristics in table 5. Different modes of operation of the device require the routing of the different clock inputs shown in figure 2 to different pins. The routing for different stage selection modes are shown in table 6, and those for the cascading modes are shown in table 7.

Table 4 : Timing Characteristics (referred to in figure 2):

Parameter	Value		Unit	Remarks
	Typical	Min.		
T_i	100	33	µ sec	Integration time
$t_{10} - t_9$, $t_2 - t_1$	400		n sec	Horizontal to vertical transfer time gap
$t_3 - t_2$, $t_5 - t_4$, $t_7 - t_6$ & $t_9 - t_8$	400		n sec	VSR clock overlap period
$t_4 - t_3$, $t_6 - t_5$ & $t_8 - t_7$	1.6		µ sec	VSR adjacent phase offset
$t_{14} - t_{10}$	150	50	n sec	Readout register clock period
$t_{11} - t_{10}$, $t_{12} - t_{11}$, $t_{13} - t_{12}$, $t_{14} - t_{13}$	$t_r / 4$		µ sec	HSR clock overlap period
$t_{\Phi r}$	$t_r / 4$		n sec	Reset clock on time

Timing Relationships (INDICATIVE – TO BE MODIFIED):



This figure shows the interrelationships between the different phases of clocks. The routing of the above signals to the different pins is shown in tables 6 & 7.

Figure 2 : Clock and output signals for normal device operation

Table 5 : Clock Characteristics:

Parameters	Symbol	Level	Value		Unit
			Min	Max	
Parallel SR clocks[1] (four phases: X=1,2,3,4)	ϕ_{VX}	HIGH	10	13	V
		LOW	0.4	1	V
Stage selection clocks[2] (eight pins: X=1to8)	ϕ_{SSGX}	HIGH	10	13	V
		LOW	0.4	1	V
Parallel to Serial S.R. Clock	ϕ_{VH}	HIGH	10	13	V
		LOW	0.4	1	V
Serial SR Clocks (four phases: X=1,2,3,4)	ϕ_{HX}	HIGH	10	13	V
		LOW	0.4	1	V
Reset clocks	ϕ_{R}	HIGH	10	13	V
		LOW	0.4	1	V
Parallel shift register transport and stage selection clocks	$C\Phi_{V1I,V3I}$		4.4		nF
	$C\Phi_{V2I,V4I}$		3.5		nF
	$C\Phi_{V1G,V3G}$		3.3		nF
	$C\Phi_{V2G,V4G}$		2.6		nF
	$C\Phi_{V1H,V3H}$		2.2		nF
	$C\Phi_{V2H,V4H}$		1.7		nF
	$C\Phi_{V1A,V3A,}$ $C\Phi_{V1E,V3E,}$ $C\Phi_{V1F,V3F}$		820		pF
	$C\Phi_{V2A,V2E,}$ $C\Phi_{V2F,V4A}$		650		pF
	$C\Phi_{V1C,V3C,}$ $C\Phi_{V1D,V3D,}$ $C\Phi_{V4E,V4F}$		540		pF
	$C\Phi_{V2C,V2D}$		430		pF
	$C\Phi_{V4C,V4D}$		320		pF
	$C\Phi_{V1B,V3B}$		270		pF
	$C\Phi_{V2B}$		220		pF
	$C\Phi_{V4B,SS(A\ to\ H)}$		110		pF
Parallel to Serial S.R. Clock	$C\Phi_{VH}$		200		pF
Serial SR Clocks (four phases: X=1,2,3,4)	$C\Phi_{HX}$		200		pF
Reset clocks	$C\Phi_{R}$		25		pF

Table 6: Clock connections for different stage selection options. The clock phase for each pin corresponding to each stage selection option is shown. Un-shaded cells denote gates clocked normally, cells in gray denote gates clocked for reverse transfer cells and 'L' denotes gates held at low potential to act as a barrier.

VSR Section	Pin	Stage Selection option			
		96	32	8	2
33-96	Φ_{V1D}	1	1	1	1
	Φ_{V2D}	2	4	4	4
	Φ_{V3D}	3	3	3	3
	Φ_{V4D}	4	2	2	2
	Φ_{SSC}	4	L	2	2
9-32	Φ_{V1C}	1	1	1	1
	Φ_{V2C}	2	2	4	4
	Φ_{V3C}	3	3	3	3
	Φ_{V4C}	4	4	2	2
	Φ_{SSB}	4	4	L	2
3-8	Φ_{V1B}	1	1	1	1
	Φ_{V2B}	2	2	2	4
	Φ_{V3B}	3	3	3	3
	Φ_{V4B}	4	4	4	2
	Φ_{SSA}	4	4	4	L
1-2	Φ_{V1A}	1	1	1	1
	Φ_{V2A}	2	2	2	2
	Φ_{V3A}	3	3	3	3
	Φ_{V4A}	4	4	4	4
	Φ_{V4T}	4	4	4	4
	Φ_{VH}	1	1	1	1

Table 7: Clocking requirements for different cascading options. The clock phase for each pin corresponding to each cascading option is shown. 'L' signifies that a low potential value is applied to the pin, for it to act as a barrier. For each cascading option, only the VDD pins marked 'ON' need to be powered.

Pins	Number of outputs				
	24	12	6	3	1
$\Phi_{H1A\ \&\ B}$	1	1	1	1	1
$\Phi_{H2A\ \&\ B}$	2	2	2	2	2
$\Phi_{H3A\ \&\ B}$	3	3	3	3	3
$\Phi_{H4A\ \&\ B}$	4	4	4	4	4
Φ_{HTA}	4	L	L	L	L
Φ_{HCA}	L	4	4	4	4
Φ_{HTB}	4	4	L	L	L
Φ_{HCB}	L	L	4	4	4
Φ_{HTC}	4	4	4	L	L
Φ_{HCC}	L	L	L	4	4
Φ_{HTD}	4	4	4	4	L
Φ_{HCD}	L	L	L	L	4
V_{DDA}	ON	OFF	OFF	OFF	OFF
V_{DDB}	ON	ON	OFF	OFF	OFF
V_{DDC}	ON	OFF	OFF	OFF	OFF
V_{DDD}	ON	ON	ON	OFF	OFF
V_{DDE}	ON	OFF	OFF	OFF	OFF
V_{DDF}	ON	ON	ON	ON	ON
V_{DDG}	ON	ON	OFF	OFF	OFF
V_{DDH}	ON	OFF	OFF	OFF	OFF

All the pins not mentioned in the above two tables will be continuously powered as defined in Table 3.

Table 8 : Static and Dynamic Electrical Characteristics :

Symbol	Description	Values	Unit
P_{DC}	Static power dissipation	2.9	W
P_{AC}	Dynamic power dissipation	4.8	W
Z_{OUT}	Output impedance	250	Ω
DC_{OUT}	Output DC level	11	V
I_G	Gate leakage current	1	nA

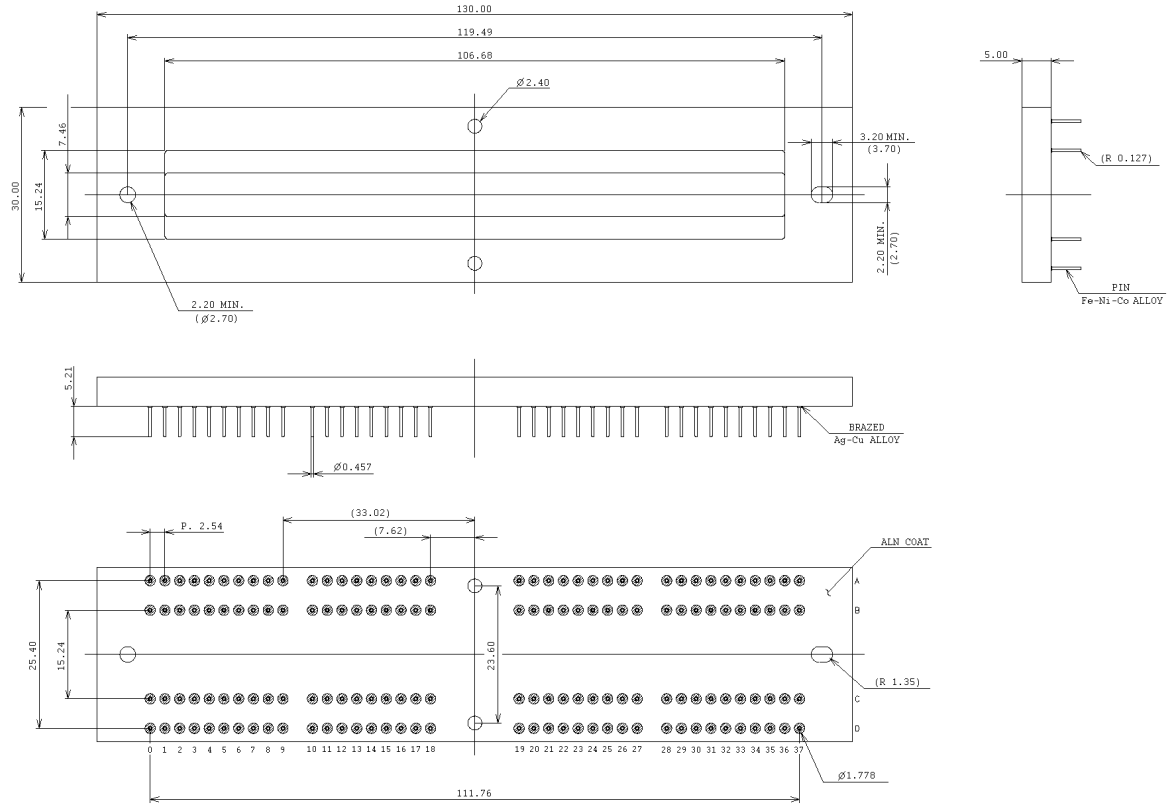
Table 9 : Electro-optical Characteristics :

The parameters are valid for Integration Time, Ti = 0.1 msec

Parameter	Value	Unit	Remarks
Linearity (gamma)	0.015	-	For signal range 1e3e$^-$ to 2e5e$^-$.
Conversion gain	>4	μV/e$^-$	
Charge Handling Capacity	>2.5e5	e$^-$	
Dark current signal -Mean -Peak	 <500 <1000	 e$^-$/msecs e$^-$/msecs	Measured at 25±0.1°C
Noise in darkness	<50	e$^-$ rms	Measured at 25±0.1°C
Signal to RMS Noise Ratio	>250	-	Measured at 25±0.1°C
PS to readout register crosstalk	<1	%	
Spectral response variation among pixels a. within a device b. among devices	 <3 <10	 % %	
Quantum efficiency B1 band B2 band B3 band B4 band	 >0.1 >0.2 >0.2 >0.15	 - - - -	 B1 (400-450nm) B2 (520-590nm) B3 (620-680nm) B4 (770-860nm)
Response non-uniformity -Max high spatial freq. Non-uniformity -Max. N.U. excl. spikes & dips. -Max. allowable no. of spikes & dips -Max. N.U. incl. spikes & dips. -Max. signal amplitude of any pixel with respect to that of adjacent.	 4 ±3 10 ±7 5	 % % % - %	
CTF at λ=500nm at λ=850nm	 >0.7 >0.3	 - -	
Horizontal charge transfer efficiency	>0.999995	-	
Vertical charge transfer efficiency	>0.99999	-	

Package Drawing :

The device package is of ceramic PGA type.



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