FRAME TRANSFER-CCD DEVICE FOR HySIS MISSION (SD31130)

DATA SHEET

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SFSD/EOSG/SEDA
SPACE APPLICATIONS CENTRE

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PRODUCT DESCRIPTION:

HySIS device is a Frame transfer CCD. The Image Region consists of an array of 1000 x 60 for sensing of the image and collection of the photo-generated charge. Image region is split in two parts, which is subsequently readout through four Readout Shift Registers; two shift register is at top of the image region and other two shift register is at bottom of the image region. Image region and storage is separated by 8 dark isolation rows and 3 unshielded rows. Each readout shift register is terminated in an Output Section. The electrical points in the device are accessed through Device Pads.

The schematic of the device, shown in the Fig. 1 comprises of the blocks which are described below.

BLOCK DIAGRAM:

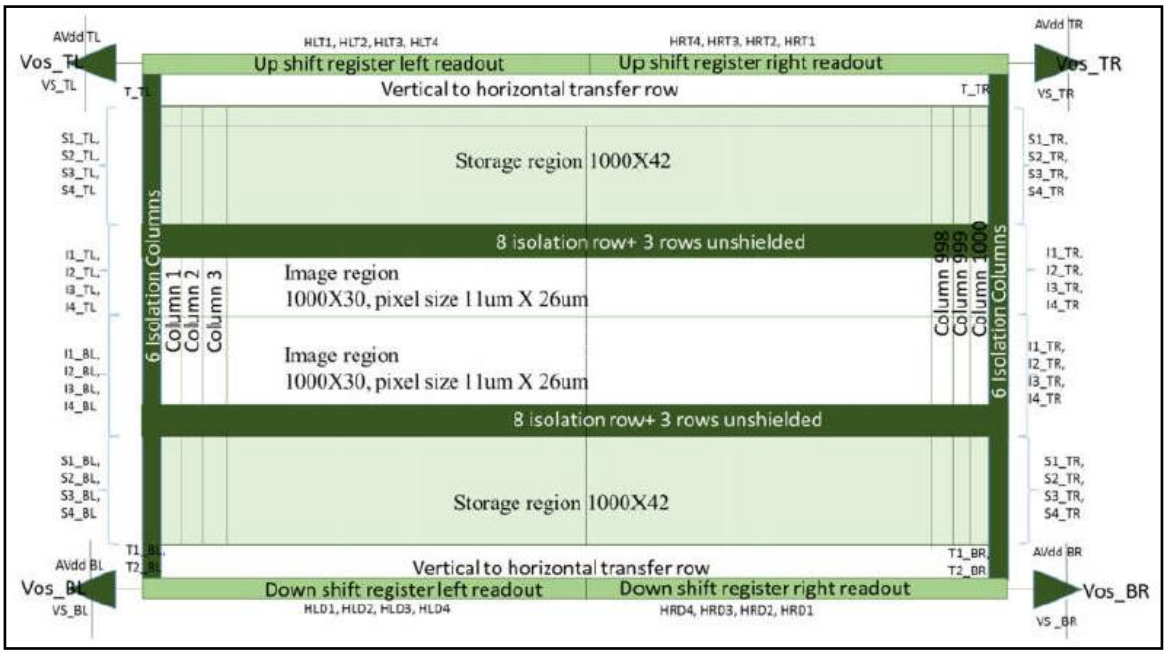

Figure-1: Device Block Diagram

IMAGE REGION

The image region of the device consists of an array of 1000 columns, 6 isolation columns on both side of image region and 60 photosensitive rows. The signals from the isolation columns are read out as dark reference. Pixels of each column are of 4-phase N-buried channel type, serving the multiple purposes of photo-detection, charge integration and charge transfer. Image region is split in two parts, top thirty rows are readout from top horizontal shift register and bottom thirty rows are readout from bottom horizontal shift register

STORAGE REGION

The storage region of the device is an array of shift register elements identical to the image region, covered by the second metal layer to prevent photo-generation. Photo-generated charge packets are transferred to the storage region for subsequent row-by-row readout. To reduce the

effect of cross-talk, there are 3 unshielded rows followed by 8 dark isolation rows between the image and storage regions. Three unshielded rows are kept so that image region should not get affected by shadow of shield metal. Between the storage region and the readout shift register, is an independently clocked vertical to horizontal transfer gate.

READOUT SHIFT REGISTERS

The readout comprises 4 readout shift registers. Each shift register read 500 active pixels and 6 isolation pixels. There are 3 extra pixels and 6 isolation elements that are read out before the active elements. The readout shift registers are of 4-phase N-buried channel type.

OUTPUT SECTION

The output section comprises a floating diffusion charge detection node, a reset transistor and a two-stage N-buried channel source follower amplifier.

Characteristics	Details
Number of photosensitive elements	1000 × 60
Pixel Pitch	11µm
Pixel Size	11µm × 26µm
Dark Isolation rows	8 (between the Image and storage region)
Dark Isolation columns	6 (both side)
Number of serial readout shift registers and video outputs	4
Number of elements per read-out register (all are read) Active elements Pre-scan isolation elements	 500 6
Vertical transfer	4 phase (N buried channel)
Horizontal shift register transfer	4-Phase N buried channel
Charge detection node	Floating diffusion type
Output amplifier	2-stage buried channel source follower type

Table 1: Device Characteristics

DEVICE DESIGN SPECIFICATIONS

pixel size: 11um X 26 um; Pixel format: 1000 columns X 60 rows; 4 output port

S.No	EO parameters	Value
1	Full well capacity	≥500 ke
2	Read Noise	<100 e
3	Conversion gain	~ 4uV/e
4	HCTI (50% of saturation)	<0.2%
5	VCTI(50% of saturation)	<0.1%
6	QE (%) 500nm 700nm 900nm	 >20 >40 >20

Table 2: Device Design Specification

PIN DESCRIPTION:

Pad No.	Pin No.	SCL Name	SAC Name	Type	Description
1	1	VOS_TL	Output_TL	Bias	Output Port
2	2	VS_TL	AVSS_TL	Bias	Amplifier VSS (ground)
3	3	VSS	VSS2	Bias	Substrate Contact (Guard Ring)
4	4	FH4T	CRLAST_TL	CLK	Last Horizontal Shift Register
5	5	FH4_TL	HCCD_P1_TL	CLK	HCCD_Phase 1 clock for charge transfer
6	6	FH3_TL	HCCD_P2_TL	CLK	HCCD_Phase 2 clock for charge transfer
7	8	FH2_TL	HCCD_P3_TL	CLK	HCCD_Phase 3 clock for charge transfer
8	9	FH1_TL	HCCD_P4_TL	CLK	HCCD_Phase 4 clock for charge transfer
9	7,10,13	VPD	VDD1	Bias	VDD Contact (Guard Ring)
10	7,10,13	VPD	VDD2	Bias	VDD Contact (Guard Ring)
11	7,10,13	VPD	VDD3	Bias	VDD Contact (Guard Ring)
12	11,12	VSS	VSS3	Bias	Substrate Contact (Guard Ring)
13	11,12	VSS	VSS4	Bias	Substrate Contact (Guard Ring)
14	11,12	VSS	VSS5	Bias	Substrate Contact (Guard Ring)
15	11,12	VSS	VSS6	Bias	Substrate Contact (Guard Ring)
16	11,12	VSS	VSS7	Bias	Substrate Contact (Guard Ring)
17	11,12	VSS	VSS8	Bias	Substrate Contact (Guard Ring)
18	11,12	VSS	VSS9	Bias	Substrate Contact (Guard Ring)
19	7,10,13	VPD	VDD4	BIAS	VDD Contact (Guard Ring)
20	7,10,13	VPD	VDD5	BIAS	VDD Contact (Guard Ring)
21	7,10,13	VPD	VDD6	BIAS	VDD Contact (Guard Ring)
22	14	FH1_TR	HCCD_P4_TR	CLK	HCCD_Phase 4 clock for charge transfer
23	15	FH2_TR	HCCD_P3_TR	CLK	HCCD_Phase 3 clock for charge transfer
24	16	FH3_TR	HCCD_P2_TR	CLK	HCCD_Phase 2 clock for charge transfer
25	17	FH4_TR	HCCD_P1_TR	CLK	HCCD_Phase 1 clock for charge transfer
26	18	FH4T	CRLAST_TR	CLK	Last Horizontal Shift Register
27	19	VSS	VSS12	BIAS	Substrate Contact (Guard Ring)
28	20	VS_TR	AVSS_TR	Bias	Amplifier VSS (ground)
29	21	VOS_TR	Output_TR	Bias	Output Port
30	22	VDD_TR	AVDD_TR	Bias	Amplifier VDD
31	23	VRD_TR	RST_Drain_TR	Bias	Reset Drain
32	24	VSS	VSS11	BIAS	Substrate Contact (Guard Ring)
33	25	FR_TR	RST_Clk_TR	CLK	Reset Clock
34	26	VOG_TR	VSET_TR	Bias	Set Gate Bias
35	27	FVH_TR	TG_TR	CLK	Vertical To Horizontal Charge Transfer Gate
36	28	FVS1_TR	STU_P1_TR	CLK	Storage Upper Frame Phase1 Clock
37	29	FVS2_TR	STU_P2_TR	CLK	Storage Upper Frame Phase2 Clock
38	30	FVS3_TR	STU_P3_TR	CLK	Storage Upper Frame Phase3 Clock
39	31	FVS4_TR	STU_P4_TR	CLK	Storage Upper Frame Phase4 Clock
40	32	FVI1_TR	AFU_P1_TR	CLK	Active Upper Frame Phase1 Clock

Pad No.	Pin No.	SCL Name	SAC Name	Type	Description
41	33	FVI2_TR	AFU_P2_TR	CLK	Active Upper Frame Phase2 Clock
42	34	FVI3_TR	AFU_P3_TR	CLK	Active Upper Frame Phase3 Clock
43	35	FVI4_TR	AFU_P4_TR	CLK	Active Upper Frame Phase4 Clock
44	36	FVI1_BR	AFL_P1_BR	CLK	Active Lower Frame Phase1 Clock
45	37	FVI2_BR	AFL_P2_BR	CLK	Active Lower Frame Phase2 Clock
46	38	FVI3_BR	AFL_P3_BR	CLK	Active Lower Frame Phase3 Clock
47	39	FVI4_BR	AFL_P4_BR	CLK	Active Lower Frame Phase4 Clock
-	40	-	-	-	-
48	41	FVS1_BR	STL_P1_BR	CLK	Storage Lower Frame Phase1 Clock
49	42	FVS2_BR	STL_P2_BR	CLK	Storage Lower Frame Phase2 Clock
50	43	FVS3_BR	STL_P3_BR	CLK	Storage Lower Frame Phase3 Clock
51	44	FVS4_BR	STL_P4_BR	CLK	Storage Lower Frame Phase4 Clock
52	45	FVH_BR1	TG_BR1	CLK	Vertical To Horizontal Charge Transfer Gate
53	46	FVH_BR2	TG_BR2	CLK	Vertical To Horizontal Charge Transfer Gate
54	47	VOG_BR	VSET_BR	Bias	Set Gate Bias
55	48	FR_BR	RST_CLK_BR	CLK	Reset_Clock
56	49	VSS	VSS12	BIAS	Substrate Contact (Guard Ring)
57	50	VRD_BR	RST_Drain_BR	Bias	Reset_Drain
58	51	VDD_BR	AVDD_BR	Bias	Amplifier VDD
59	52	VOS_BR	Output_BR	Bias	Output Port
60	53	VS_BR	AVSS_BR	Bias	Amplifier VSS (ground)
61	54	VSS	VSS13	BIAS	Substrate Contact (Guard Ring)
62	55	FH4T	CRLAST_BR	CLK	Last Horizontal Shift Register
63	56	FH4_BR	HCCD_P1_BR	CLK	HCCD_Phase 1 clock for charge transfer
64	57	FH3_BR	HCCD_P2_BR	CLK	HCCD_Phase 2 clock for charge transfer
65	59	FH2_BR	HCCD_P3_BR	CLK	HCCD_Phase 3 clock for charge transfer
66	60	FH1_BR	HCCD_P4_BR	CLK	HCCD_Phase 4 clock for charge transfer
67	58,61,64	VPD	VDD7	Bias	VDD Contact (Guard Ring)
68	58,61,64	VPD	VDD8	Bias	VDD Contact (Guard Ring)
69	58,61,64	VPD	VDD9	Bias	VDD Contact (Guard Ring)
70	62,63	VSS	VSS14	Bias	Substrate Contact (Guard Ring)
71	62,63	VSS	VSS15	Bias	Substrate Contact (Guard Ring)
72	62,63	VSS	VSS16	Bias	Substrate Contact (Guard Ring)
73	62,63	VSS	VSS17	Bias	Substrate Contact (Guard Ring)
74	62,63	VSS	VSS18	Bias	Substrate Contact (Guard Ring)
75	62,63	VSS	VSS19	Bias	Substrate Contact (Guard Ring)
76	62,63	VSS	VSS20	Bias	Substrate Contact (Guard Ring)
77	58,61,64	VPD	VDD10	Bias	VDD Contact (Guard Ring)
78	58,61,64	VPD	VDD11	Bias	VDD Contact (Guard Ring)
79	58,61,64	VPD	VDD12	Bias	VDD Contact (Guard Ring)
80	65	FH1_BL	HCCD_P4_BL	CLK	HCCD_Phase 4 clock for charge transfer
81	66	FH2_BL	HCCD_P3_BL	CLK	HCCD_Phase 3 clock for charge transfer

Pad No.	Pin No.	SCL Name	SAC Name	Type	Description
82	67	FH3_BL	HCCD_P2_BL	CLK	HCCD_Phase 2 clock for charge transfer
83	68	FH4_BL	HCCD_P1_BL	CLK	HCCD_Phase 1 clock for charge transfer
84	69	FH4T	CRLAST_BL	CLK	Last Horizontal Shift Register
85	70	VSS	VSS21	BIAS	Substrate Contact (Guard Ring)
86	71	VPD	AVSS_BL	Bias	Amplifier VSS (ground)
87	72	VOS_BL	Output_BL	Bias	Output Port
88	73	VDD_BL	AVDD_BL	Bias	Amplifier VDD
89	74	VRD_BL	RST_Drain_BL	Bias	Reset Drain
90	75	VSS	VSS22	BIAS	Substrate Contact (Guard Ring)
91	76	FR_BL	RST_Clk_BL	CLK	Reset Clock
92	77	VOG_BL	VSET_BL	Bias	Set Gate Bias
93	78	FVH_BL2	TG_BL2	CLK	Vertical To Horizontal Charge Transfer Gate
94	79	FVH_BL1	TG_BL1	CLK	Vertical To Horizontal Charge Transfer Gate
95	80	FVS4_BL	STL_P4_BL	CLK	Storage Lower Frame Phase4 Clock
96	81	FVS3_BL	STL_P3_BL	CLK	Storage Lower Frame Phase3 Clock
97	82	FVS2_BL	STL_P2_BL	CLK	Storage Lower Frame Phase2 Clock
98	83	FVS1_BL	STL_P1_BL	CLK	Storage Lower Frame Phase1 Clock
-	84	-	-	-	-
99	85	FVI4_BL	AFL_P4_BL	CLK	Active Lower Frame Phase4 Clock
100	86	FVI3_BL	AFL_P3_BL	CLK	Active Lower Frame Phase3 Clock
101	87	FVI2_BL	AFL_P2_BL	CLK	Active Lower Frame Phase2 Clock
102	88	FVI1_BL	AFL_P1_BL	CLK	Active Lower Frame Phase1 Clock
103	89	FVI4_TL	AFU_P4_TL	CLK	Active Upper Frame Phase4 Clock
104	90	FVI3_TL	AFU_P3_TL	CLK	Active Upper Frame Phase3 Clock
105	91	FVI2_TL	AFU_P2_TL	CLK	Active Upper Frame Phase2 Clock
106	92	FVI1_TL	AFU_P1_TL	CLK	Active Upper Frame Phase1 Clock
107	93	FVS4_TL	STU_P4_TL	CLK	Storage Upper Frame Phase4 Clock
108	94	FVS3_TL	STU_P3_TL	CLK	Storage Upper Frame Phase3 Clock
109	95	FVS2_TL	STU_P2_TL	CLK	Storage Upper Frame Phase2 Clock
110	96	FVS1_TL	STU_P1_TL	CLK	Storage Upper Frame Phase1 Clock
111	97	FVH_TL	TG_TL	CLK	Vertical To Horizontal Charge Transfer Gate
112	98	VOG_TL	VSET_TL	Bias	Set Gate Bias
113	99	FR_TL	RST_CLK_TL	CLK	Reset_Clock
114	100	VSS	VSS1	BIAS	Substrate Contact (Guard Ring)
115	101	VRD_TL	RST_Drain_TL	BIAS	Reset_Drain
116	102	VDD_TL	AVDD_TL	Bias	Amplifier VDD

Table 3: Pin Details

DC OPERATING CONDITION

The following are the tentative DC and AC device operating conditions based on COB packaged detector. These will be fine-tuned after the prototype devices are fabricated and characterized.

AC Operating Condition:
All Clocks: 12±0.5V (High level); 0.5V (Low level)

DC Operating Condition:

Name	Description	Min value (V)	Typical value (V)	Max value (V)
AVDD_TR, AVDD_TL, AVDD_BR, AVDD_BL	Amplifier VDD	17.75	18	18.5
VDDX	VDD contact (guard ring)	13.5	14	14.5
VSSX	Substrate Contact (Guard Ring)		0	
AVSS_TR, AVSS_TL, AVSS_BR, AVSS_BL	Amplifier VSS (ground)		0	
RST_Drain_TR, RST_Drain_TL, RST_Drain_BR, RST_Drain_BL	Reset Drain	15.5	16	16.5
VSET_TR, VSET_TL, VSET_BR, VSET_BL	Set Gate Bias	1	1.2	1.4

Table 4: DC operating conditions

CLOCK TIMING DETAILS

The following figures depict the tentative timing relationships between the clock signals for normal device operation. The grey shaded regions represent multiple clock periods too numerous to be resolved in the figure.

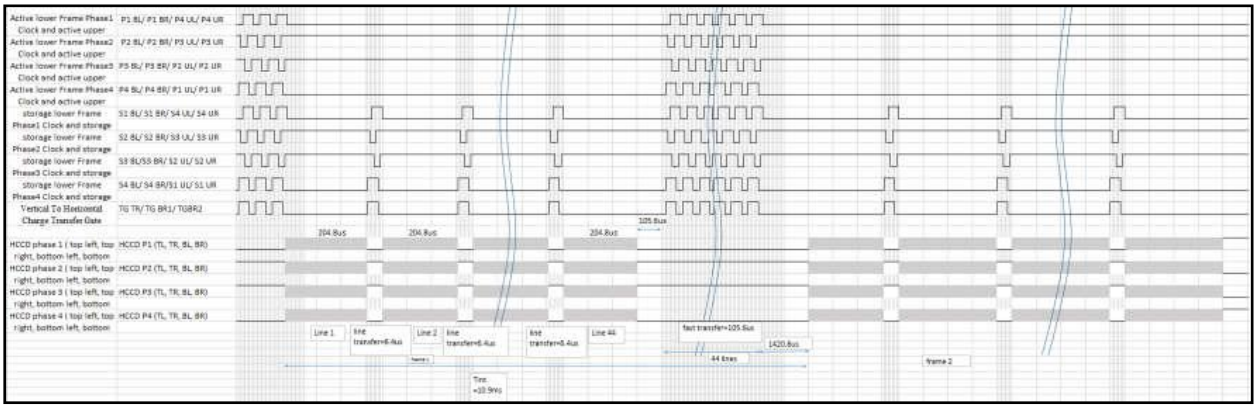

Figure-2: Overall timing diagram

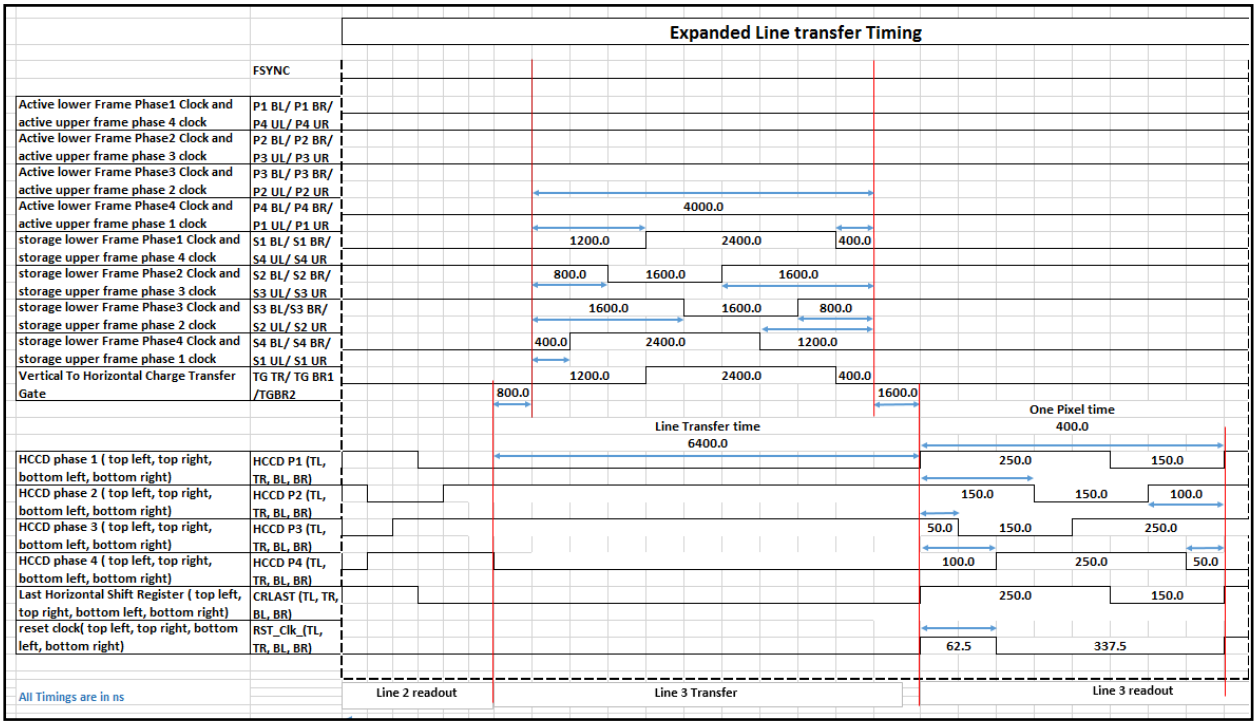

Figure-3: Line transfer timing and horizontal transfer timing

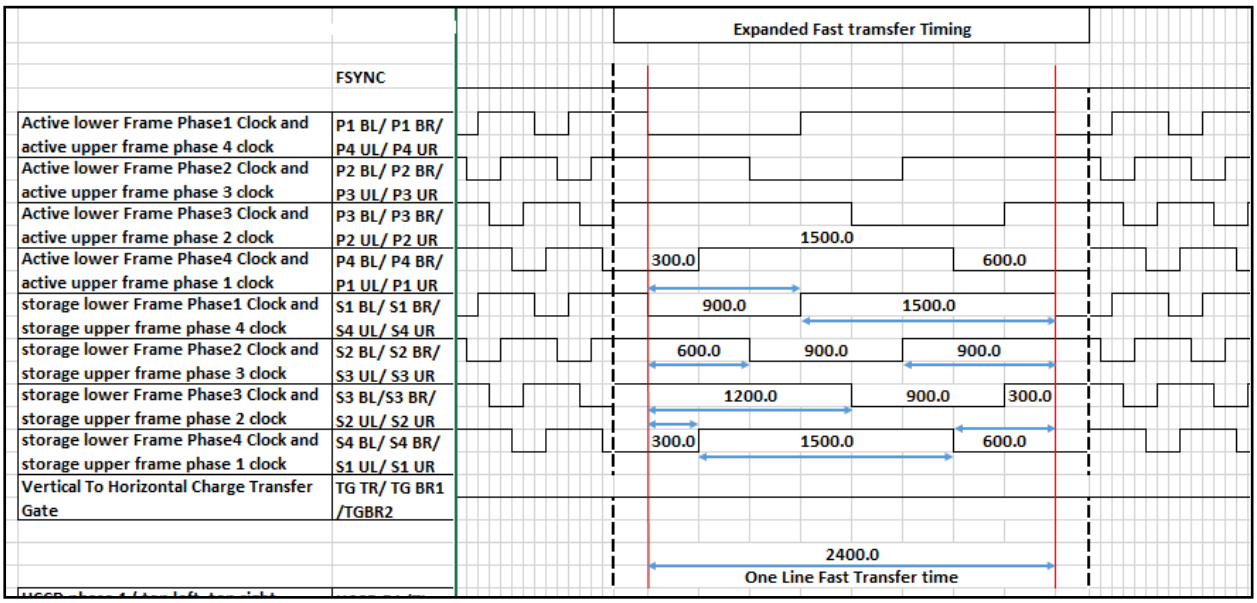

Figure-4: Fast transfer timing

Note: (All timings are in ns)

The relationships between the clocks may need to be tuned after the prototype devices are obtained. Based on the device architecture and the operational requirements, the serial register readout rate is determined.

- Frame rate: 91Hz
- Vertical to horizontal transfer time: 105.6us
- Horizontal readout rate: 2.5MHz

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