FRAME TRANSFER CCD IMAGER

4K X 48 - OCM3

(SD3101-0)

DATASHEET

Version 1.0, Aug 2017

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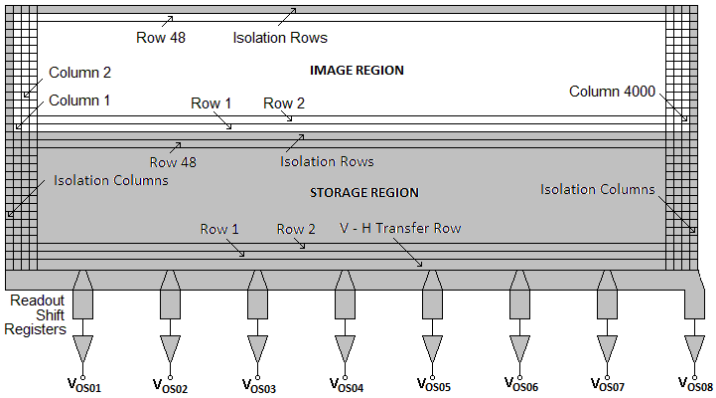
FEATURES

- **10µm × 10µm pixel size**
- **10µm pixel pitch**
- **4000 columns × 48 rows Image and Storage regions**
- **Eight output ports with cascading feature for reduced number of outputs**

Device Description:



The SD3101-0 is a Frame Transfer imager with 10µm square pixels with 4000 × 48 element Image and Storage regions. There are eight outputs with cascading feature whereby fewer outputs may be employed for readout by cascading signal from one shift register to the next, bypassing an output. The imager is designed for off-chip TDI mode and employs metal straps across the image region for feeding clock signals. This affects photo response uniformity in frame transfer imaging snap-shot mode.

The parallel shift registers are of 4-phase N-buried channel type, serving the multiple purposes of photo-detection, charge integration and charge transfer. The read-out shift registers, like the parallel shift registers, are of 4-phase N-buried channel type. The signal from 500 photo-sensitive elements associated with each read-out shift register is read out of the corresponding output. Signal charge from multiple (2, 4 or 8) read-out shift registers may be read out through a single output by employing the cascading feature, which is done by applying appropriate clock signals. This reduces the number of outputs. For the case of cascading of 2 shift registers to one output, all the unused outputs may be powered off.

Each output section comprises a floating diffusion charge detection node, a reset transistor and a two-stage N-buried channel source follower amplifier.

Device Characteristics:

The following table summarizes the main characteristics of the device.

Table 1. Device Characteristics

Characteristics	Details
Number of photosensitive elements	4000 × 48
Pixel Pitch	10µm
Pixel Size	10µm × 10µm
Isolation rows	8 (between the Image and Storage regions)
Isolation columns	8 (At each end of array)
Number of serial readout shift registers and video outputs	8
Number of elements per read-out register (all read out) Active elements Pre-scan isolation elements	 500 8
Cascading option	Cascading of 2, 4 or 8 outputs (giving 1000, 2000 or 4000 elements per output respectively)
Shift register type - Parallel - Serial	 4-Phase N buried channel 4-Phase N buried channel
Charge detection node	Floating diffusion type
Output amplifier	2-stage buried channel source follower type

Pin Descriptions:

The following table lists the device pins grouped according to their functions.

Table 2. Pin Descriptions

Pin	Pin description	Pin No.
VOFG	Overflow gate bias	38
VOFD	Overflow drain bias	57
ΦI1	Image zone shift register transport clocks (Phase 1)	40
ΦI2	Image zone shift register transport clocks (Phase 2)	41
ΦI3	Image zone shift register transport clocks (Phase 3)	43
ΦI4	Image zone shift register transport clocks (Phase 4)	44
ΦS1	Storage zone shift register transport clocks (Phase 1)	55
ΦS2	Storage zone shift register transport clocks (Phase 2)	54
ΦS3	Storage zone shift register transport clocks (Phase 3)	52
ΦS4	Storage zone shift register transport clocks (Phase 4)	51
ΦVH	Parallel to serial register transfer clock	59
ΦH1	Serial readout register transport clock (Phase 1)	2
ΦH2	Serial readout register transport clock (Phase 2)	5

Pin	Pin description	Pin No.
ΦH3	Serial readout register transport clock (Phase 3)	3
ΦH4	Serial readout register transport clock (Phase 4)	6
ΦHC1	Serial readout register cascade clock for cascading 2 registers. (Clocked to bypass SR 1, 3, 5 & 7)	7
ΦHC2	Serial readout register cascade clock for cascading 4 registers. (Clocked to bypass SR 2 & 6)	8
ΦHC3	Serial readout register cascade clock for cascading 8 registers. (Clocked to bypass SR 4)	9
ΦHT1	Serial readout register tap clock for cascading 2 registers. (Clocked to read out SR 1, 3, 5 & 7)	26
ΦHT2	Serial readout register tap clock for cascading 4 registers. (Clocked to read out SR 2 & 6)	27
ΦHT3	Serial readout register tap clock for cascading 8 registers. (Clocked to read out SR 8)	28
ΦR1	Reset clock for outputs 1, 3, 5 and 7	31
ΦR2	Reset clock for outputs 2, 4, 6 and 8	30
VOG	Output gate DC bias	34
VRD1	Reset drain supply for outputs 1, 3, 5 and 7	49
VRD2	Reset drain supply for outputs 2, 4, 6 and 8	46
VDD1	Output amplifier drain supply for outputs 1, 3, 5 and 7	47
VDD2	Output amplifier drain supply for outputs 2, 4, 6 and 8	48
VOS1	Video output 1	10
VOS2	Video output 2	12
VOS3	Video output 3	14
VOS4	Video output 4	16
VOS5	Video output 5	18
VOS6	Video output 6	20
VOS7	Video output 7	22
VOS8	Video output 8	24
VS1	Amplifier signal ground 1	11
VS2	Amplifier signal ground 2	13
VS3	Amplifier signal ground 3	15
VS4	Amplifier signal ground 4	17
VS5	Amplifier signal ground 5	19
VS6	Amplifier signal ground 6	21
VS7	Amplifier signal ground 7	23
VS8	Amplifier signal ground 8	25
VTS1	Temperature Sensor 1	63
VTS2	Temperature Sensor 2	36
VHD	Heating Element	60
VPD	Protection Drain	62
VSS	Substrate contact / Light Shield	1
VSS	Substrate contact / Light Shield	4

Pin	Pin description	Pin No.
VSS	Substrate contact / Light Shield	29
VSS	Substrate contact / Light Shield	32
VSS	Substrate contact / Light Shield	33
VSS	Substrate contact / Light Shield	35
VSS	Substrate contact / Light Shield	37
VSS	Substrate contact / Light Shield	39
VSS	Substrate contact / Light Shield	42
VSS	Substrate contact / Light Shield	45
VSS	Substrate contact / Light Shield	50
VSS	Substrate contact / Light Shield	53
VSS	Substrate contact / Light Shield	56
VSS	Substrate contact / Light Shield	58
VSS	Substrate contact / Light Shield	61
VSS	Substrate contact / Light Shield	64

Device Operating Conditions:

Table 3. DC Operating Conditions:

Bias Names	Pin Symbol(s)	Number of device pins	Value (V)			Max current per pin	Number of bond pads	Remarks
			Min	Typical	Max			
Overflow Drain Bias	V_{OFD}	1	12	13	14	1nA	1	
Overflow Gate Bias	V_{OFG}	1	0.5	1	2	1nA	1	
Output Gate Bias	V_{OG}	1	0.5	1	2	1nA	1	
Protection Drain Bias	V_{PD}	1	12	13	14	1nA	1	
Reset Drain Bias	V_{DR1}	1	12	13	14	1.1μA	4	
	V_{DR2}	1					4	
Output Amplifier Drain Bias	V_{DD1}	1	17	18	19	30mA	4	
	V_{DD2}	1					4	
Output Amplifier Source Bias	V_{S1}- V_{S8}	8	0	0	0.1	|-8mA|	8	The eight V_s pins are the return paths for the eight output terminals.
Heat Dissipation Bias	V_{HD}	1					1	The operating conditions of the heat dissipator and the temperature sensors are to be finalised after devices are characterised.
Temperature Sensor	V_{TS1}	1					1	
	V_{TS2}	1					1	
Substrate Bias	V_{SS}	TBD	-0.1	0	0		12	These are the contacts to the P-type substrate.

Note: The currents specified are for each pin. The current is divided equally among the multiple pads if there. For example, the two V_{DD} pins will draw a maximum of 30mA each, which is again the sum of 7.5mA per bond pad.

Table 4. AC Operating Conditions:

Clock Names	Pin Symbol	Number of device pins	Low Level		High Level		Rise Time	Fall Time	Capacitance (per pin)	Number of bond pads
			Min	Max	Min	Max				
			V	V	V	V	ns	ns	pF	
Image Zone Shift Register Clocks	IΦ1 – IΦ4	4	0.4	0.6	11	13	200	200	3000	4
Storage Zone Shift Register Clocks	SΦ1 – SΦ4	4	0.4	0.6	11	13	200	200	3000	4
Parallel to Serial Transfer Clock	Φ_{VH}	1	0.4	0.6	11	13	200	200	150	1
Serial Register Transport Clocks	HΦ1	1	0.4	0.6	11	13	10	10	150	8
	HΦ2	1								9
	HΦ3	1								9
	HΦ4	1								8
Serial Register Tap and Cascade Clocks	HΦT1, HΦC1	1 + 1	0.4	0.6	11	13	10	10	50	4
	HΦT2, HΦC2	1 + 1								2
	HΦT3, HΦC3	1 + 1								1
Reset Clock	ΦR1	1	0.4	0.6	11	13	8	8	25	4
	ΦR2	1								4

Note: The capacitances specified are for each pin. For example, the fourHF pins have a capacitance load of 150pF each.

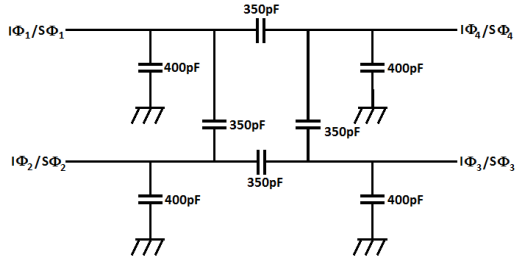


Fig. 1. Parallel shift register capacitance network

Clock Timing Details

The following figures depict the tentative timing relationships between the clock signals for normal device operation.From the functional requirements, the vertical fast transfer is at 200kHz. This is shown in the figure below. The relationships between the clocks may need to be tuned after the prototype devices are obtained.Based on the device architecture and the operational requirements, the serial readout register readout rate is determined.

- Fast transfer rate: 200kHz
- Number of vertical transfers: 52
- Time gap between vertical transfer and serial readout: 250ns
- HSR elements (including pre-scan elements): 512

From the required frame rate of 220fps, the serial readout has to take place at approximately 6.67MHz.

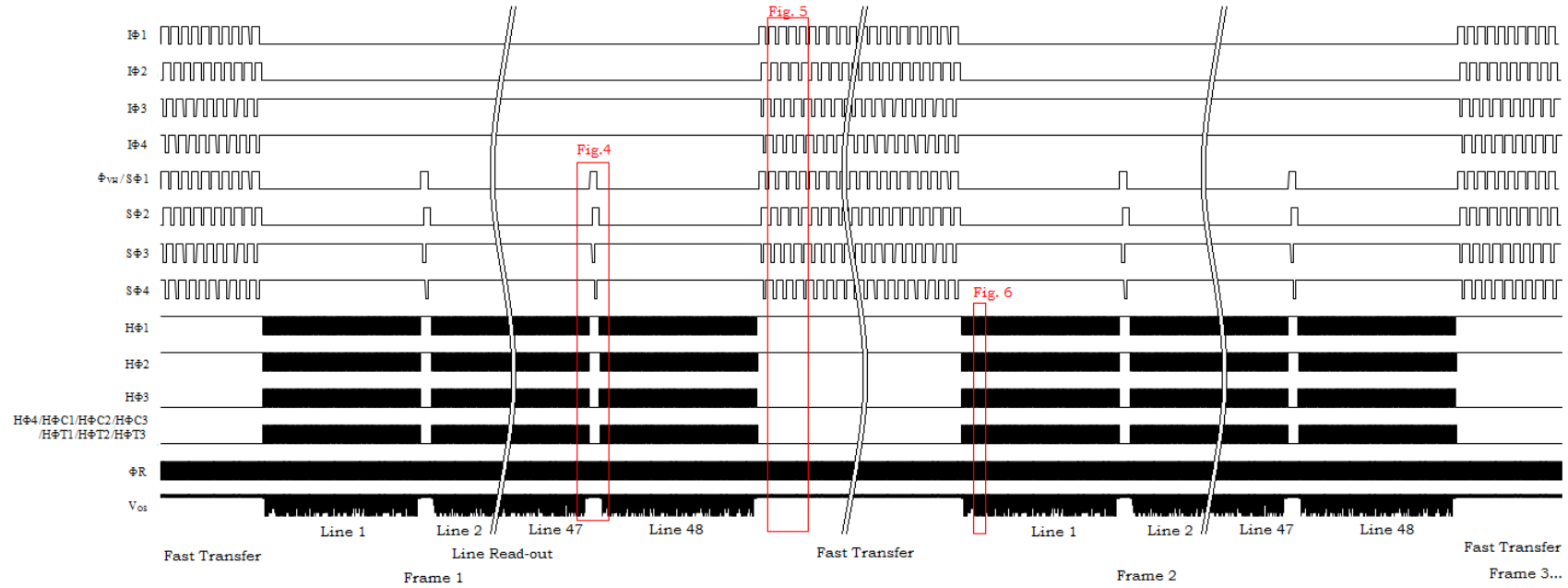


Fig. 2. Complete Frame Timing Diagram

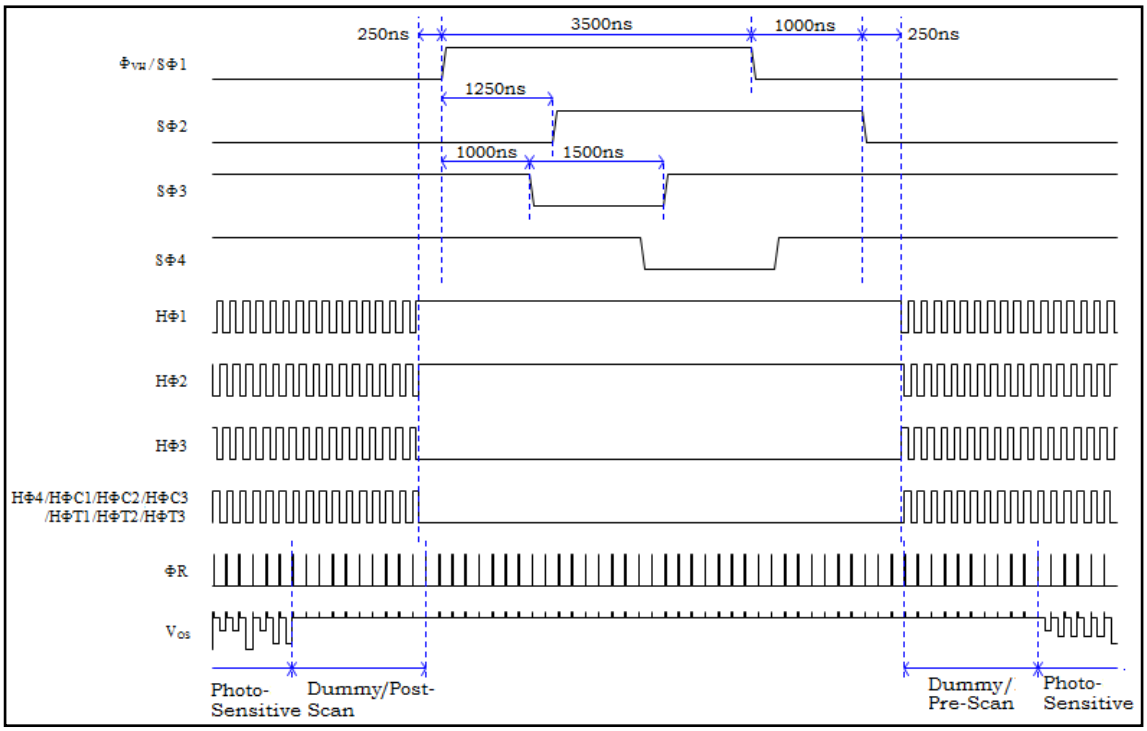


Fig. 3. Vertical Transfer and Read-out

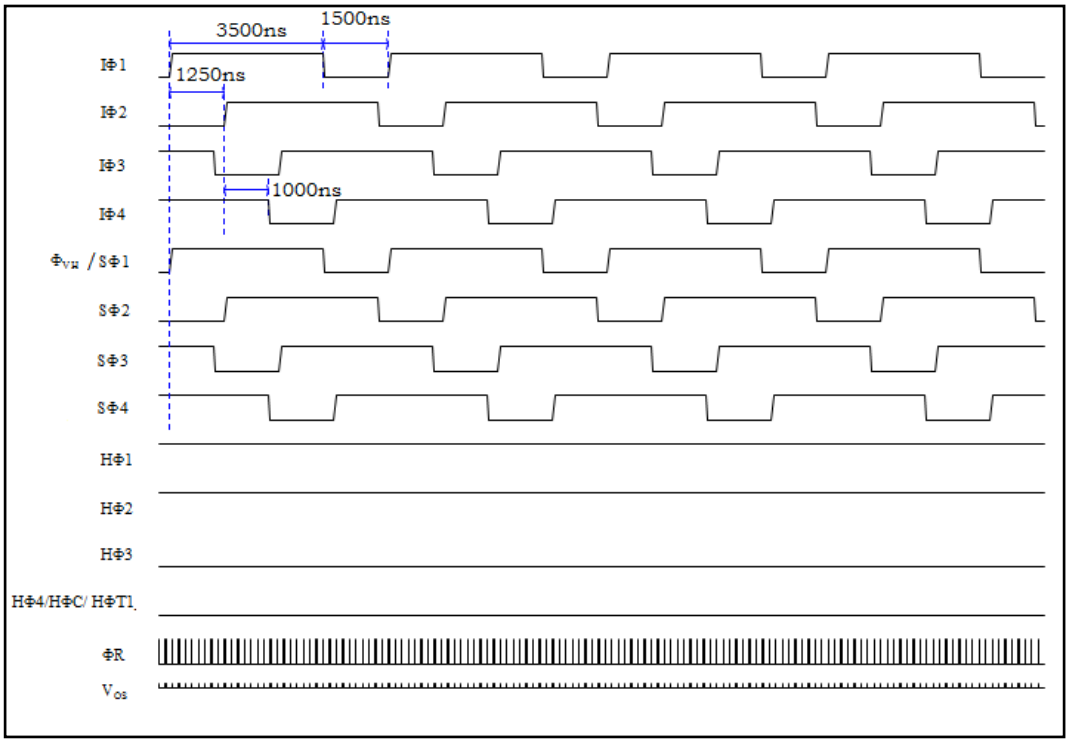


Fig. 4. Vertical Fast Transfer

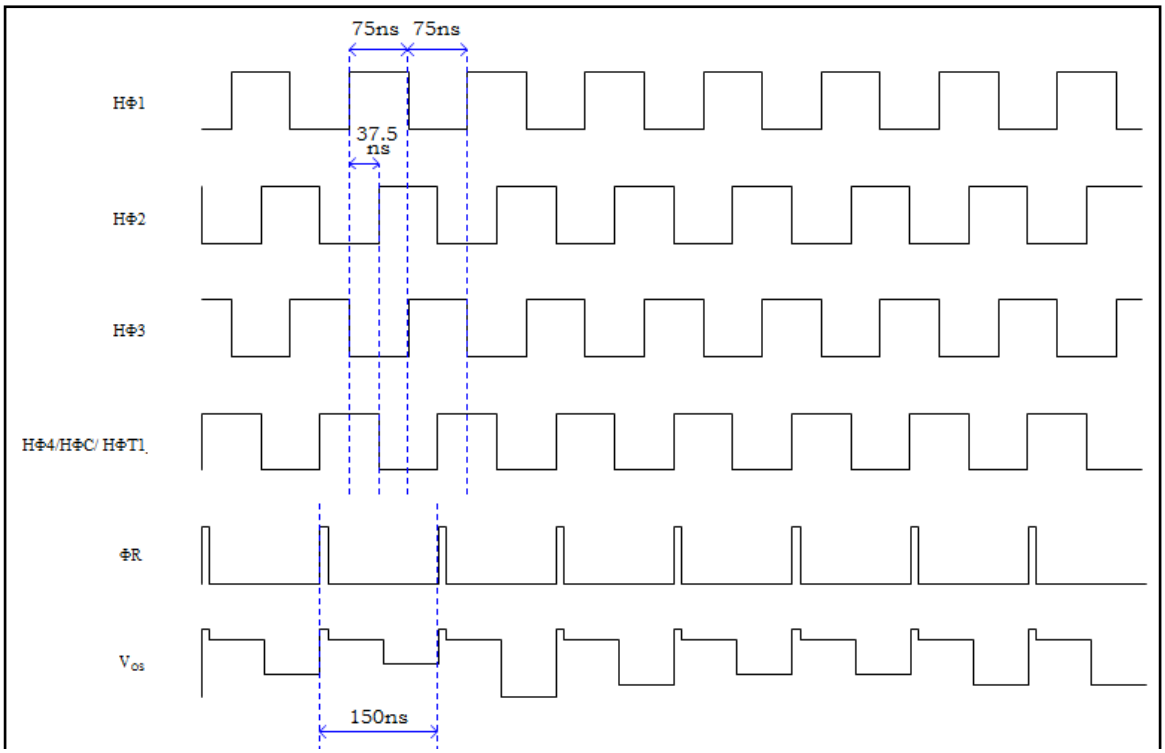


Fig. 5. Horizontal Read-out

Device Performance Characteristics

The following two tables list the target electrical and electro-optical parameter values for the device. Some of these values are estimated values and may change after the fabricated devices are characterised.
The electrical parameters are to be met for 220fps and 20fps.

Table 5. Device Electrical Parameters

Sr. No.	Parameter	Target Value	Remarks
1.	DC output level of video	10V to 15V	
2.	DC mismatch among outputs of same device	≤0.5V	
3.	Total power dissipation at nominal readout rate		Will be provided at CDR.
4.	Video o/p drive capability	220Ω to 250Ω	Final value with dispersion will be provided at CDR.
5.	Leakage current	≤5nA	All gates to substrate leakage
6.	Reference zone / Stable zone (ΔT1 / ΔT2)	Stable up to 10bit accuracy for ≥15% of pixel readout range.	To be demonstrated with output load capacitor value mentioned in the figure 2 below
7.	Image zone to storage zone vertical transfer rate	≥200kHz for both frame rates	
8.	Storage zone to horizontal shift register transfer rate	Commensurate to required frame rates	
9.	Horizontal shift register transfer rate	>5MHz	

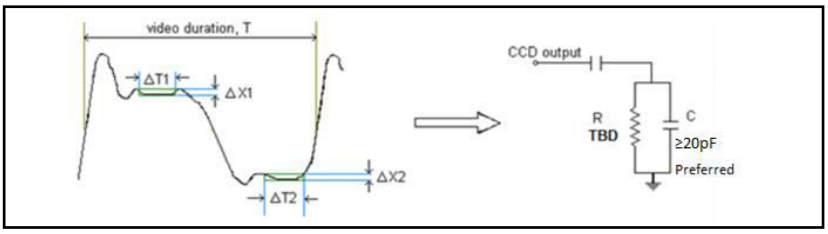


Fig. 6. Pixel output waveform stable zones definition and output load for measuring the same.

The electro-optical requirements specified below are to be met under test conditions of 20°C with frame rates of 220fps and 20fps and with F# 4.5 optics.

Table 6. Device electro-optical parameters

Sr. No.	Parameter	Target Value				Remarks
1.	Photo-site charge handling capacity (Qsat)	≥300ke				
2.	Signal to noise ratio	≥400 at 250ke				
3.	Conversion gain	>4μV/e				
4.	Readout noise	≤70e				
5.	Dark signal	≤3500e/p/s				
6.	Dark offset	≤50mV				
7.	Photo-site to light shield pixel cross-talk	≤1% at 250ke				
8.	RMS non-linearity error (for signal between 5% and 80% of Qsat)	≤1%				Linearity error to be demonstrated for different full well capacities (50% and 100% of Qsat)
9.	Quantum efficiency and MTF	Band	λ (nm)	QE (%)	MTF (%)	
		B1	412	>11	>30	
		B2	443	>11	>30	
		B3	490	>13	>30	
		B4	510	>15	>45	
		B5	555	>18	>45	
		B6	566	>16	>45	
		B7	620	>17	>45	
		B8	670	>17	>45	
		B9	681	>23	>45	
		B10	710	>18	>30	
		B11	780	>18	>30	
		B12	870	>10	>20	
		B13	1010	>8.3	>10	
10.	Band wise average responsivity					To be provided after prototype devices are characterised.
11.	Pk-Pk Dark signal non-uniformity	≤±5%				

Sr. No.	Parameter	Target Value	Remarks
12.	Pk-Pk band specific photo response non-uniformity within pixels of an array (for signal of 80% of Qsat)	≤±10%	For snapshot mode, presence of metal straps will be considered.[1]
13.	Vertical transfer inefficiency	≤±2% for 80% FWC	Ok
14.	Horizontal transfer inefficiency	For 80% FWC: ≤1% For 5% FWC: See remarks	For 5% FWC: To be provided after prototypes are characterised.
15.	Anti-blooming operation		Not provided

[1] The layout has metal straps across the photosensitive array of the device to feed clock signals to the polysilicon gates in order to meet the vertical transfer requirements. While this will reduce the effective fill factor of some pixels, it does not cause degradation of performance in actual operation because of off-chip TDI mode.