DATA SHEET

12-BIT 200 MSPS CURRENT STEERING DAC (Digital to Analog Converter)

SC9023-0

Version 1.0, March 2022

Semi–Conductor Laboratory

Government of India

PRODUCT DESCRIPTION:

The SC9023-0 is integrated 12-bit 200MSPS digital-to-analog converter with a tunable full-scale output current from 2mA to 20mA and having two complementary outputs. It has an on-chip precise low drift voltage reference of 1.2V. SC9023-0 can also operate with an external reference. This may improve the DC accuracy if the external reference circuitry is superior in its drift and accuracy. Latches are provided for high-speed synchronization providing better AC characteristics for DAC. The ASIC is fabricated in 180nm SCL CMOS technology.

FEATURES:

- **Operating Voltage: 3.3V/1.8V**
- **Resolution: 12Bits**
- **Data Rate: 200MSPS**
- **Full Scale Current: 2mA to 20mA**
- **On Chip Voltage References**
- **Input straight Binary Format**
- **Package: 64 PIN CQFP**
- **Radiation hardened (TID) up to 300Krad(Si)**

APPLICATIONS:

- **Software-Defined Radio**
- **Signal and waveform Generation**

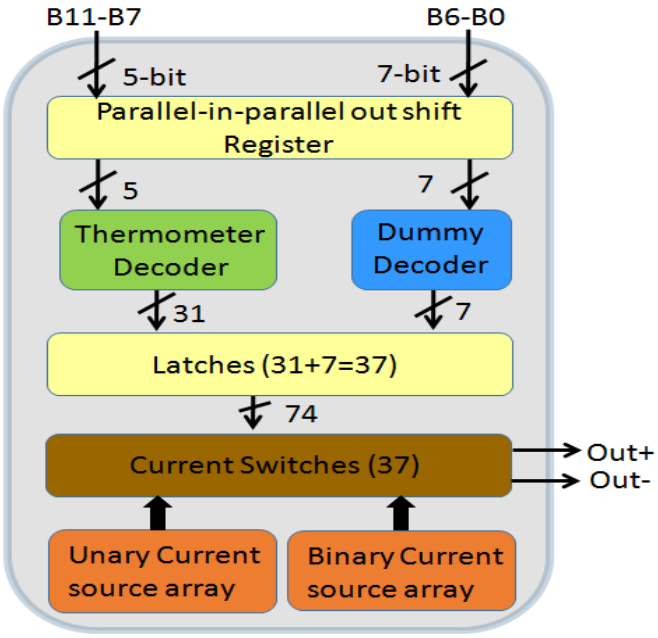


Figure-1: Device Block Diagram

DEVICE SUMMARY:

Table-1: Package Detail

Reference	Package	Pins	Lead Finish	Description	Junction Temp. Range
SC9023-0	CQFP Package	64	Gold	Engineering Model	-55°C to +125°C

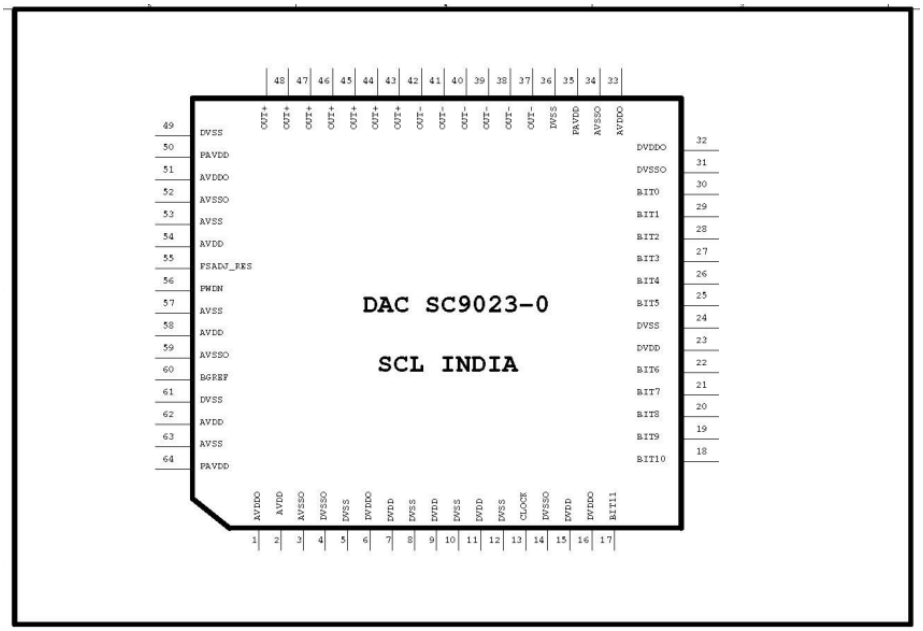


Figure-2: Pin Diagram

Table-2: Pin Configuration

Pin No.	Pin Name	Pin Type	Pin Description
1,33,51	AVDDO	AP	Analog Positive Supply (+3.3 V)
35,50,64	PAVDD	AP	Analog Positive Supply (+1.8 V)
2,54,58,62	AVDD	AP	Analog Positive Supply (+3.3 V)
7,9,11,15,23	DVDD	DP	Digital Positive Supply (+1.8 V)
6,16,32	DVDDO	DP	Digital Positive Supply (+3.3 V)
53,57,63	AVSS	AP	Analog Negative Supply (0 V)
3,34,52,59	AVSSO	AP	Analog Negative Supply (0 V)
5,8,10,12,24,36,49,61	DVSS	DP	Digital Negative Supply (0 V)
4,14,31	DVSSO	DP	Digital Negative Supply (0 V)
43,44,45,46,47,48	OUT+	AO	DAC+ output current. Full-scale current when all data bits are 1s. These pins are internally shorted and should also be shorted at the PCB level.
37,38,39,40,41,42	OUT-	AO	DAC- output current. Full-scale current when all data bits are 0s.These pins are internally shorted and should also be shorted at the PCB level.
55	FSADJ_RES	AI	Full-Scale output current Adjust. Connect 2kohm to analog ground for 20mA full-scale output current. (Note 1).
56	PWDN	DI	Power Down PIN (Active Low) PWDN = logic '0' (Power-down mode) PWDN = logic '1' (Normal Model)
60	BGREF	AO	Internal reference output (Bypass with 0.1µF to Analog Ground is recommended)
13	CLOCK	AI	Clock Input

Pin No.	Pin Name	Pin Type	Pin Description
17	BIT11	DI	Data Bits (MSB)
18	BIT10	DI	Data Bits
19	BIT9	DI	Data Bits
20	BIT8	DI	Data Bits
21	BIT7	DI	Data Bits
22	BIT6	DI	Data Bits
25	BIT5	DI	Data Bits
26	BIT4	DI	Data Bits
27	BIT3	DI	Data Bits
28	BIT2	DI	Data Bits
29	BIT1	DI	Data Bits
30	BIT0	DI	Data Bits(LSB)

PIN TYPE: AI = Analog Input, AO = Analog Output, DI = Digital Input, DO = Digital Output, AP = Analog Power, DP = Digital Power.

Note 1: FSADJ_RES Pin Functionality

This pin is for adjusting full-scale output current. At this pin, voltage is internally set at 1.22V (Typical). Based on resister connect at FSADJ_RES pin w.r.t. ground will set the desired full-scale output current. To get 20mA full-scale output current, a 2kΩ resistor (low drift) is required at FSADJ_RES pin w.r.t. ground.

Table-3: Full-scale current with an external resistor connected at FSADJ_RES pin w.r.t global ground

S. No.	Current flowing through an external resistor connected between FSADJ_RES pin and ground ($I_{REF}=1.22/R_{FSADJ\_RES}$) (µA)	Full-Scale Output Current $I_{FS}=32\times I_{REF}$ (mA)
1	625	20
2	62.5	2

ELECTRICAL SPECIFICATIONS:

All typical specifications are at T_A = 25°C, AVDDO=AVDD=DVDDO=3.3V, PAVDD=DVDD=1.8V, CLOCK=200MHz and I_{FS} = 20mA unless otherwise stated. All maximum specifications are assured across operating temperature and voltage ranges.

Table-4: Electrical Specifications

Parameters		Test Conditions	Min.	Typ.	Max.	Units
POWER SUPPLY						
Analog supply voltage AVDDO, PAVDD, AVDD			3.135	3.3	3.465	V
Digital supply voltage (DVVDO)			3.135	3.3	3.465	V
Digital supply voltage(DVVD)			1.71	1.8	1.89	V
Analog Supply Current	AVDDO		50	51	62	µA
	AVDD		23.5	23.6	23.7	mA
Digital Supply Current	DVDDO		460	470	480	µA
	DVDD		1.79	1.83	1.90	mA
Power Dissipation[2]			83	84	85	mW
Analog Supply Current (Power down mode)	AVDDO		50	51	62	µA
	AVDD		250	270	425	µA
Digital Supply Current (Power down mode)	DVDDO		50	51	70	µA
	DVDD		50	51	62	µA
Power Dissipation (Power Down)[3]			1.5	2.3	2.7	mW
INTERNAL REFERENCE						
Internal Reference Output, BGREF			1.2048	1.2216	1.2275	V
Full-Scale Output current Adjust, FSADJ_RES			599.1	610.5	619.8	µA
OUTPUT CURRENT						
Minimum Full Scale Output Current[4], $I_{FS(MIN)}$				2		mA
Maximum Full Scale Output Current[4], $I_{FS(MAX)}$				20		mA
Gain Error			-0.9		+0.9	% of FSR
Offset Error			-0.4		+0.8	% of FSR
Power Supply Gain Sensitivity (PSGS)	OUT+		1.10	1.11	1.36	% of FSR
	OUT-		1.08	1.09	1.29	% of FSR
DC ACCURACY						
Differential Non Linearity (DNL)			-0.6		0.7	LSB
Integral Non Linearity (INL)			-0.8		0.6	LSB
AC LINEARITY						

Parameters	Test Conditions	Min.	Typ.	Max.	Units
Signal To Noise Ratio (SNR)	f_{clk} = 1 MHz ; f_{out} = 100.021 KHz		74		dBc
	f_{clk} = 10 MHz ; f_{out} = 500.0305 KHz		70		dBc
	f_{clk} = 50 MHz ; f_{out} = 2.5002 MHz		60		dBc
	f_{clk} = 100 MHz; f_{out} = 2.5009 MHz		60		dBc
	f_{clk} = 200 MHz; f_{out} = 1.0040 MHz		61		dBc
	f_{clk} = 200 MHz; f_{out} = 5.0018 MHz		57		dBc
	f_{clk} = 200 MHz; f_{out} = 10.0006 MHz		53		dBc
Signal To Noise And Distortion (SINAD)	f_{clk} = 1 MHz; f_{out} = 100.021 KHz		73		dBc
	f_{clk} = 10 MHz ; f_{out} = 500.0305 KHz		69		dBc
	f_{clk} = 50 MHz ; f_{out} = 2.5002 MHz		59		dBc
	f_{clk} = 100 MHz; f_{out} = 2.5009 MHz		59		dBc
	f_{clk} = 200 MHz; f_{out} = 10.0006 MHz		53		dBc
Total Harmonics Distortion (THD)	f_{clk} = 1 MHz; f_{out} = 100.021 KHz		-82		dBc
	f_{clk} = 10 MHz ; f_{out} = 500.0305 KHz		-76		dBc
	f_{clk} = 50 MHz ; f_{out} = 2.5002 MHz		-70		dBc
	f_{clk} = 100 MHz; f_{out} = 2.5009 MHz		-69		dBc
	f_{clk} = 200 MHz; f_{out} = 10.0006 MHz		-71		dBc
Spurious-Free Dynamic Range (SFDR)	f_{clk} = 1 MHz; f_{out} = 100.021 KHz		83		dBc
	f_{clk} = 10 MHz ; f_{out} = 500.0305 KHz		80		dBc
	f_{clk} = 50 MHz ; f_{out} = 2.5002 MHz		73		dBc
	f_{clk} = 100 MHz; f_{out} = 2.5009 MHz		73		dBc
	f_{clk} = 200 MHz; f_{out} = 10.0006 MHz		68		dBc
Effective Number of Bits (ENOB)	f_{clk} = 1 MHz ; f_{out} = 100.021 KHz		11.9		Bits
	f_{clk} = 10 MHz ; f_{out} = 500.0305 KHz		11.1		Bits
TEMPERATURE RANGE		-55	25	125	°C
DIGITAL INPUT					
VIH : Logic-high input voltage		2.0		DVVDO	V
VIL : Logic-low input voltage		0.0		0.8	V
IIH : Logic-high input current		-10		10	µA
IIL : Logic-low input current		-10		10	µA

Note 2: Measured with I_{OUTFS} = 20mA, R_{LOAD} = 50 Ω at I_{OUT+} and I_{OUT-} w.r.t. Ground and 100 Ω resistance between I_{OUT+} and I_{OUT-}, f_{clock} = 200 MSPS and f_{in} = 41MHz digital sine wave applied at BIT11 to BIT0.
Note 3: Measured with All positive and negative supplies are applied. The clock input is connected to ground. PWDN input is made low. Digital inputs BIT11 to BIT0 are at '0' logic.
Note 4: Nominal full-scale current, I_{FS}, equals 32x the I_{REF} current.

ABSOLUTE MAXIMUM RATINGS:

Table-5: Absolute Maximum Ratings*

Parameter	With Respect To	Min.	Max.	Units
Digital Inputs (BIT11-BIT0) and CLOCK	DVSSO	-0.3	PDVDDO+0.3	V
Analog Output	AVSSO	-0.3	PAVDDO+0.3	V
AVDD	DVSS and AVSSO	-0.3	4.0	V
AVDDO	AVSSO	-0.3	4.0	V
DVDDO	DVSSO	-0.3	4.0	V
PAVDD	AVSSO	-0.3	2.0	V
DVDD	DVSSO	-0.3	2.0	V
AVSS	DVSS	-0.3	0.3	V
DVSSO	DVSS	-0.3	0.3	V
AVSSO	DVSS	-0.3	0.3	V
Storage Temperature		-65	150	ºC

- Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

TYPICAL TIMING DIAGRAM:

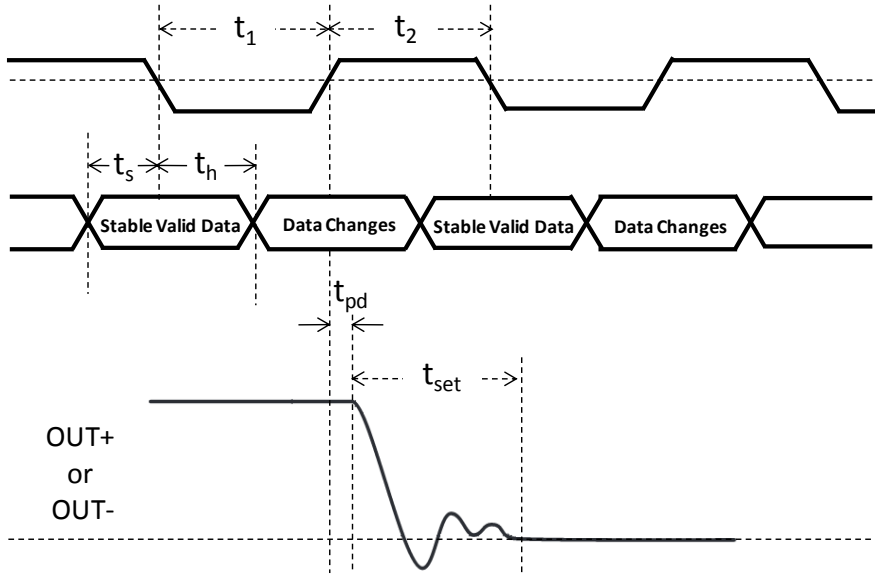


Figure-3: The typical timing diagram for DAC

Table 6: Typical timing for DAC

Symbol	Parameter	Value	Unit
t_1	Clock pulse low time	2.5	ns
t_2	Clock pulse high time	2.5	ns
t_s	Data setup time	1	ns
t_h	Data Hold Time	1	ns
t_{pd}	Propagation Delay Time	1	ns
t_{set}	Output Settling Time to 1%	< 30	ns

TYPICAL CHARACTERISTICS PLOTS:

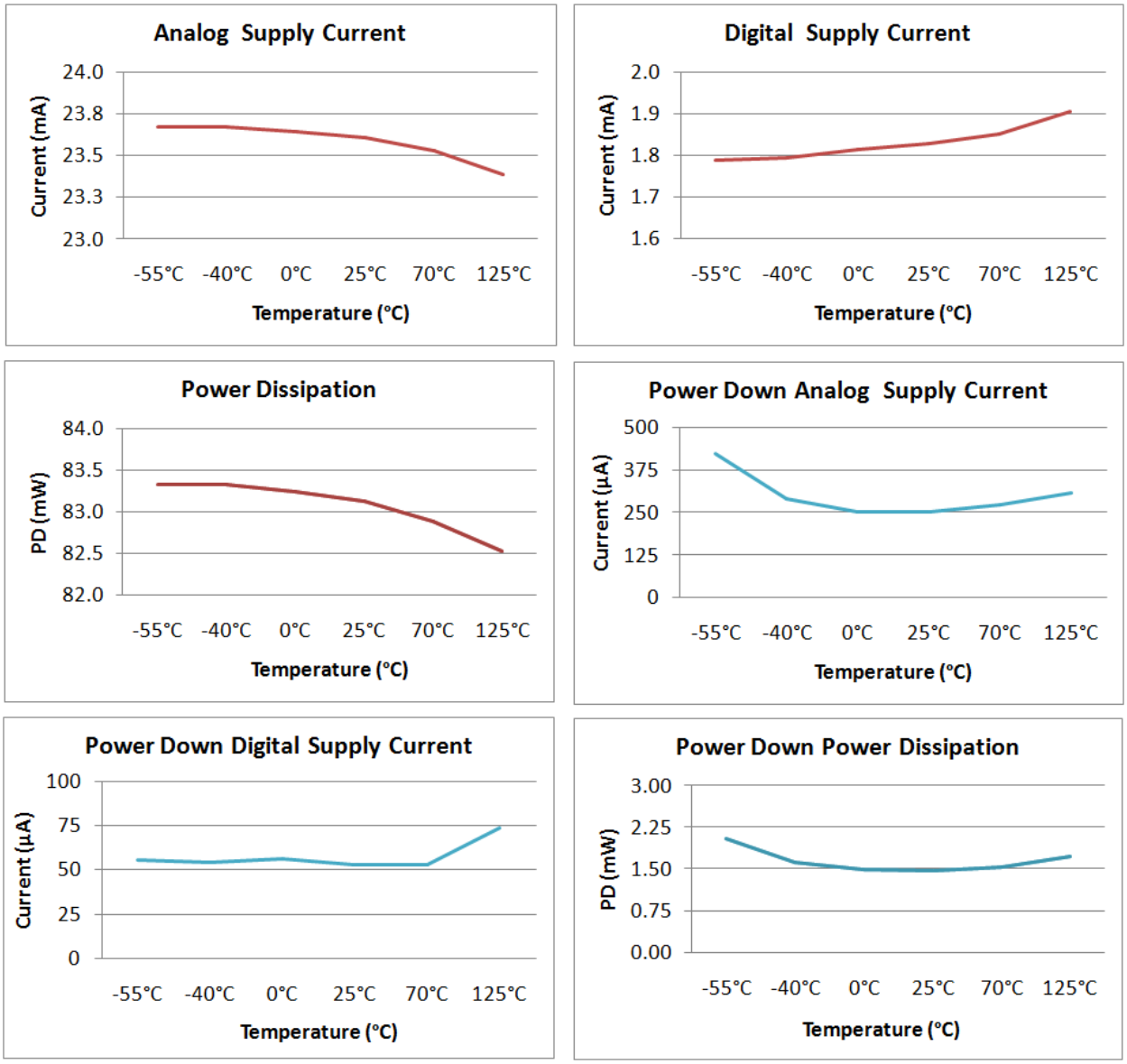


Figure 4: Typical Characteristics Plots

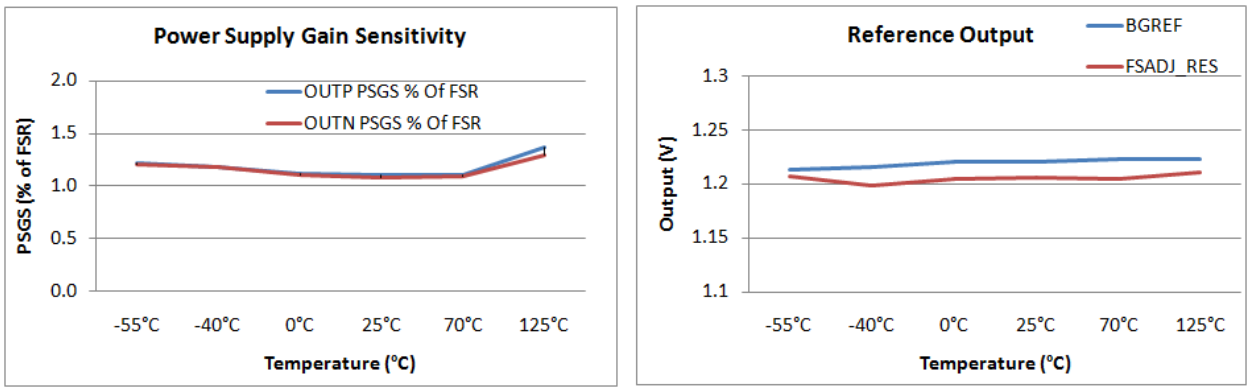
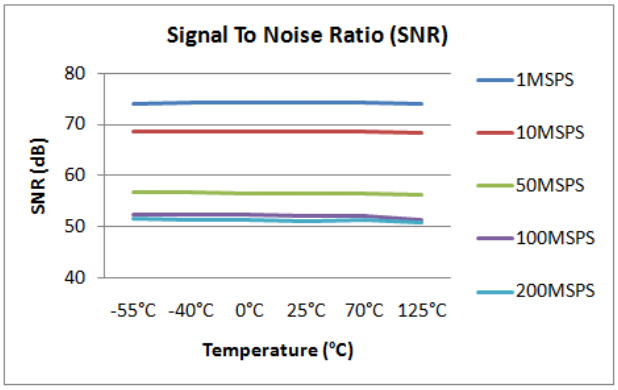
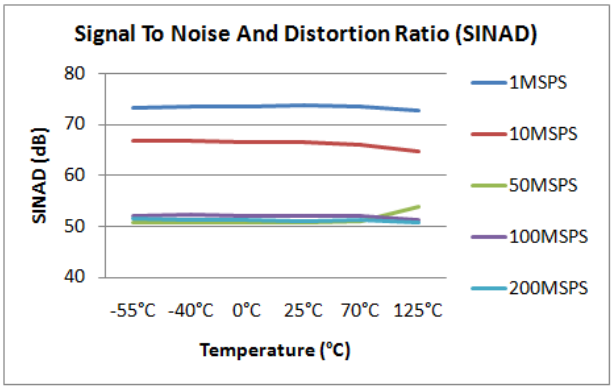
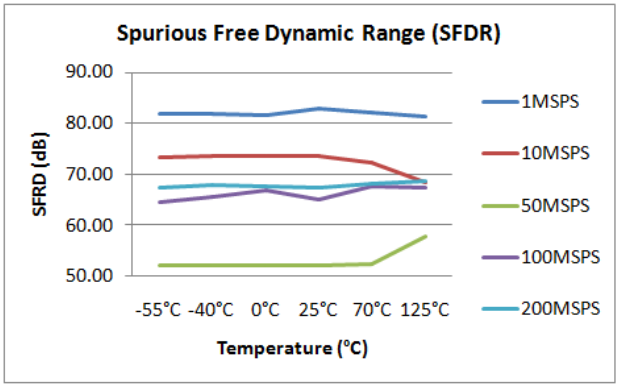
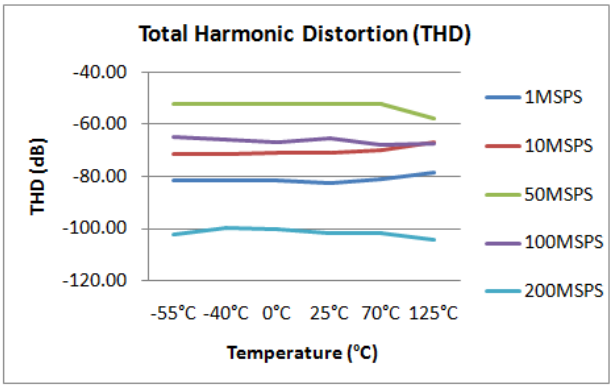


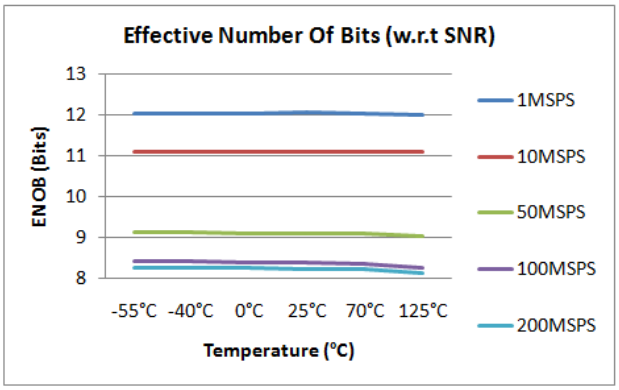
Figure 5: Power Supply Gain Sensitivity and Reference Output Voltage Plots











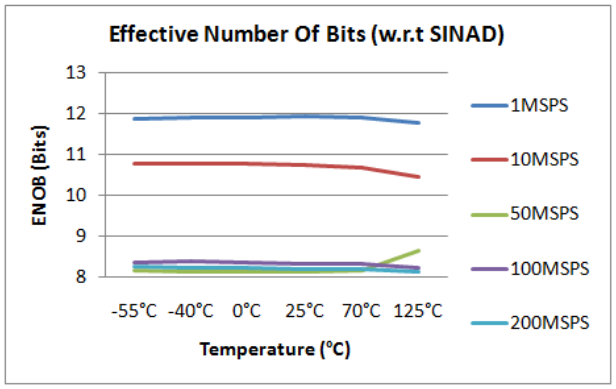
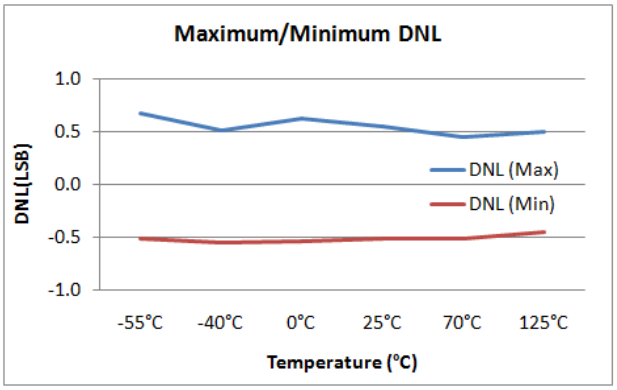


Figure 6: Typical AC Characteristics Plots



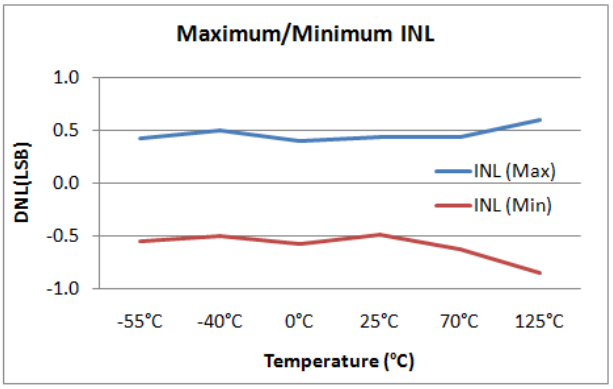


Figure 7: DNL/INL (Min/Max) Plots

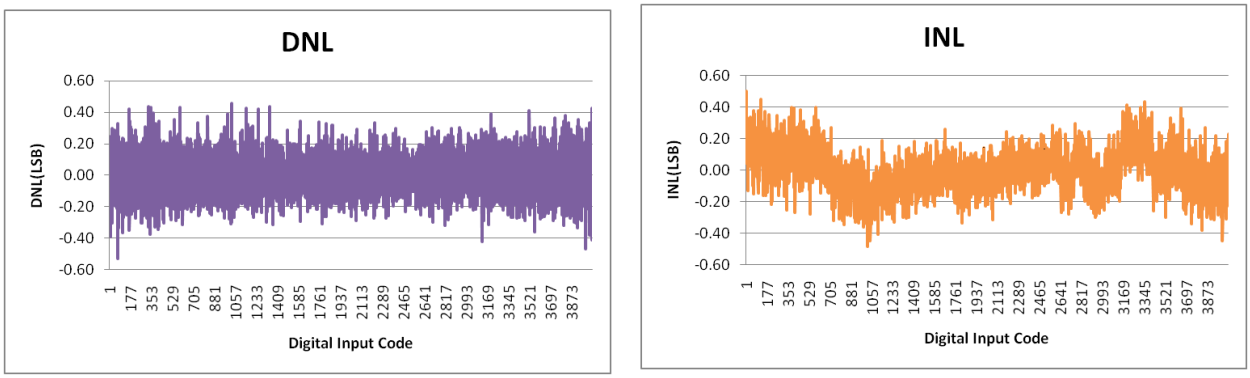


Figure 8: DNL and INL Plots (25°C)

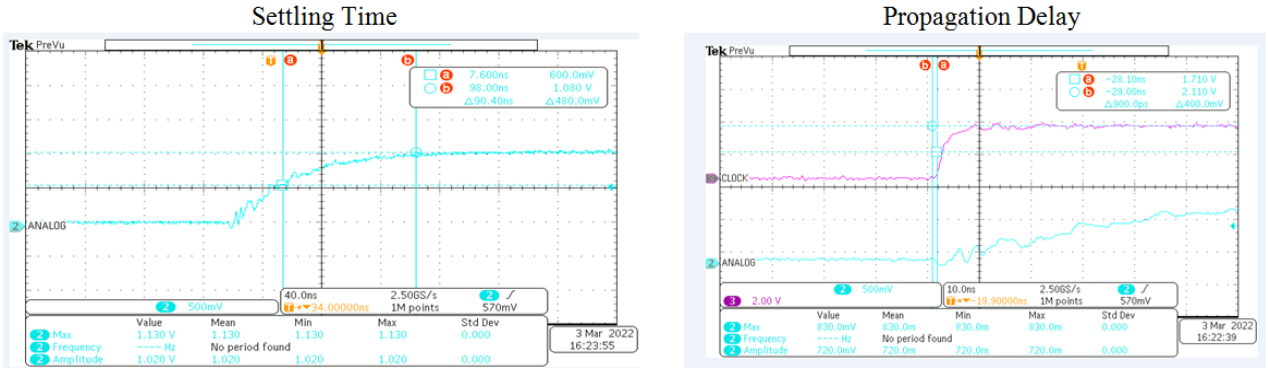


Figure 9: Settling Time and Propagation Delay

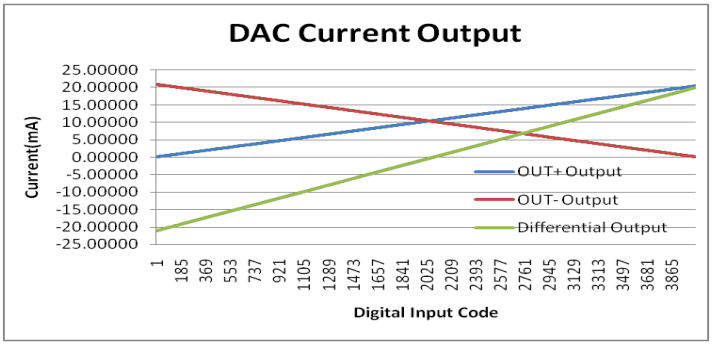


Figure 10: DAC Output currents (25°C)

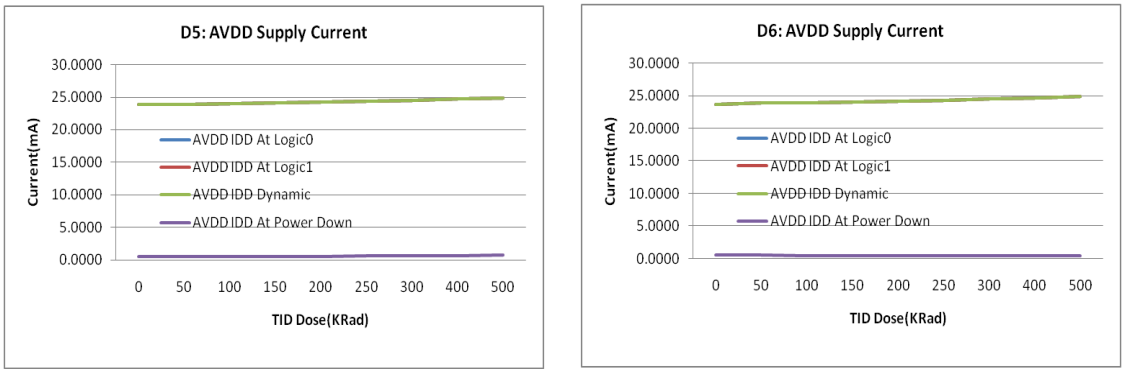


Figure11: AVDD Supply Current with Different TID Dose

OVERVIEW:

SC9023-0 is 12-Bit 200MSPS Current Steering Digital to Analog Converter. Segmentation architecture is being used in the design. Five MSB bits are unary decoded and remaining seven bits are binary decoded. Block diagram of the DAC is shown in Fig.1. A 12-bit data from the external world is coming into latch. Latch stores the data at the falling edge of the clock. After that thermometer decoder encodes five MSB bits into thermometer code. Thermometer blocks generate finite delay and to match the delay among binary and thermometer decoded output, dummy decoder has been used for the remaining seven LSB bits. These outputs from Thermometer decoder and dummy decoder derives latch outputs which generate differential output for select current switches connected between the output and current sources. Based on the input bits, DAC will provide differential output current. Sum of differential current is fixed and it is equal to full scale output current of the DAC.

TERMINOLOGY

Integral Nonlinearity (INL)
Linearity error is defined as the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero to full scale.

Differential Nonlinearity (DNL)
DNL is the measure of the variation in analog value, normalized to full scale, associated with a 1 LSB change in digital input code.

Gain Error
The difference between the actual and ideal output span. The actual span is determined by the output when all inputs are set to 1s minus the output when all inputs are set to 0s.

Offset Error
The deviation of the output current from the ideal of zero is called the offset error. For I_{OUT+}, 0mA output is expected when the inputs are all 0s. For I_{OUT-}, 0mA output is expected when all inputs are set to 1s.

Settling Time
The time required for the output to reach and remain within a specified error band about its final value, measured from the start of the output transition.

Spurious-Free Dynamic Range (SFDR)
The difference, in dB, between the rms amplitude of the output signal and the peak spurious signal over the specified bandwidth.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal. It is expressed as a percentage or in decibels (dB).

Power Supply Gain Sensitivity (PSGS)
Power supply gain sensitivity is defined as change in percentage of full scale output current w.r.t. supply variation.

$$PSGS_{\text{from 3.3 to 3.135}} = \frac{I_{FS\,(3.3V)} - I_{FS\,(3.135V)}}{I_{FS\,(IDEAL\,)}} \times 100$$

$$PSGS_{\text{from 3.3 to 3.465}} = \frac{I_{FS\,(3.3V)} - I_{FS\,(3.465V)}}{I_{FS\,(IDEAL\,)}} \times 100$$

Signal-to-Noise Ratio (SNR)

$$SNR = 10 \log \left(\frac{\text{Signal Power}}{\text{Noise Power}}\right)$$

Signal-to-Noise And Distortion (SINAD)

$$SINAD = 10\log \left(\frac{\text{Signal Power}}{\text{Noise Power} + \text{ Distortion Power}}\right)$$

Effective Number of Bits (ENOB)

$$ENOB = \left(\frac{SINAD - 1.76}{6.02}\right)$$

APPLICATION DIAGRAM:

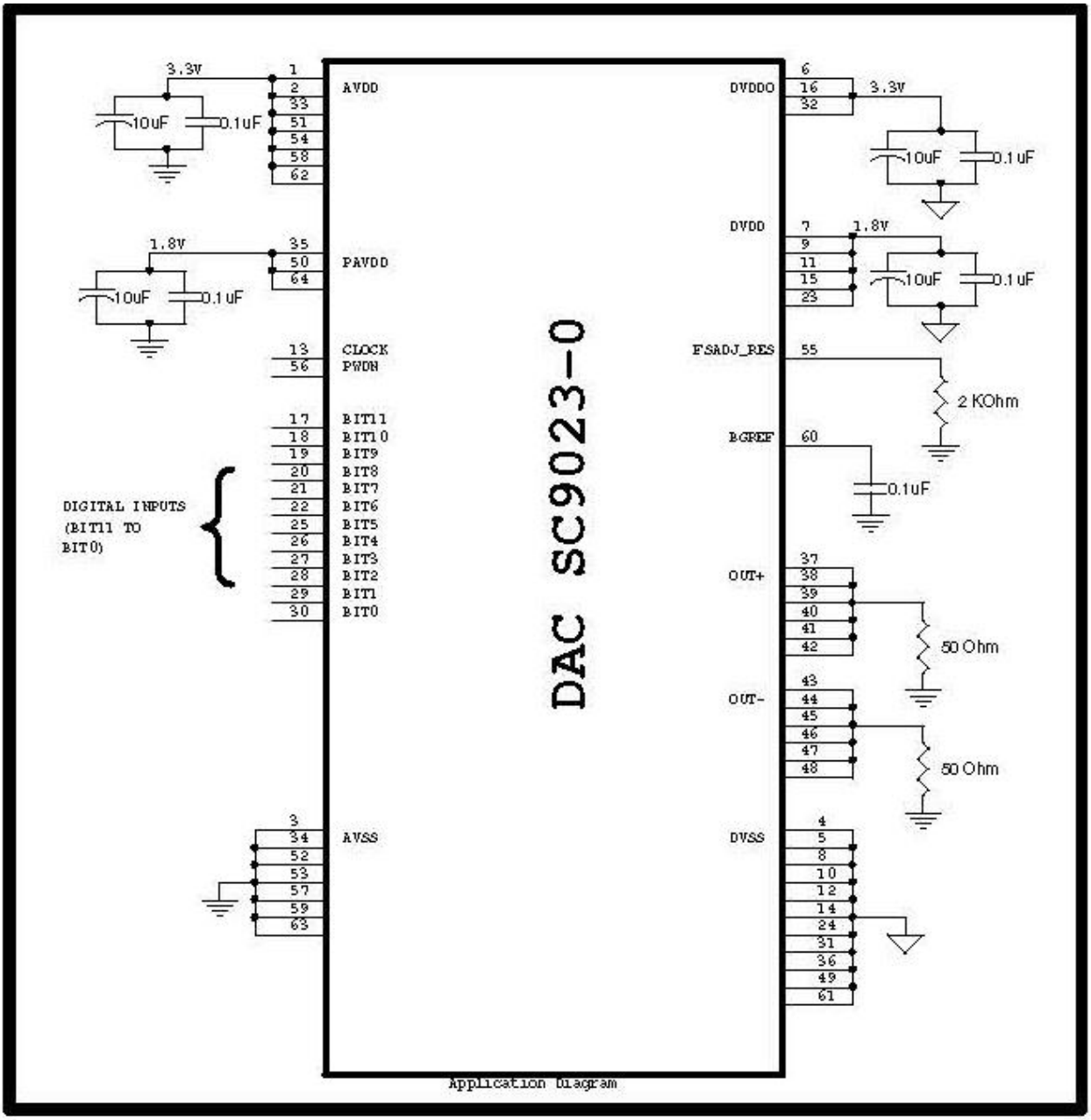


Figure-12: Application Diagram

PACKAGE DRAWING (64 Pin CQFP):

All linear dimensions are in inches (mm.)

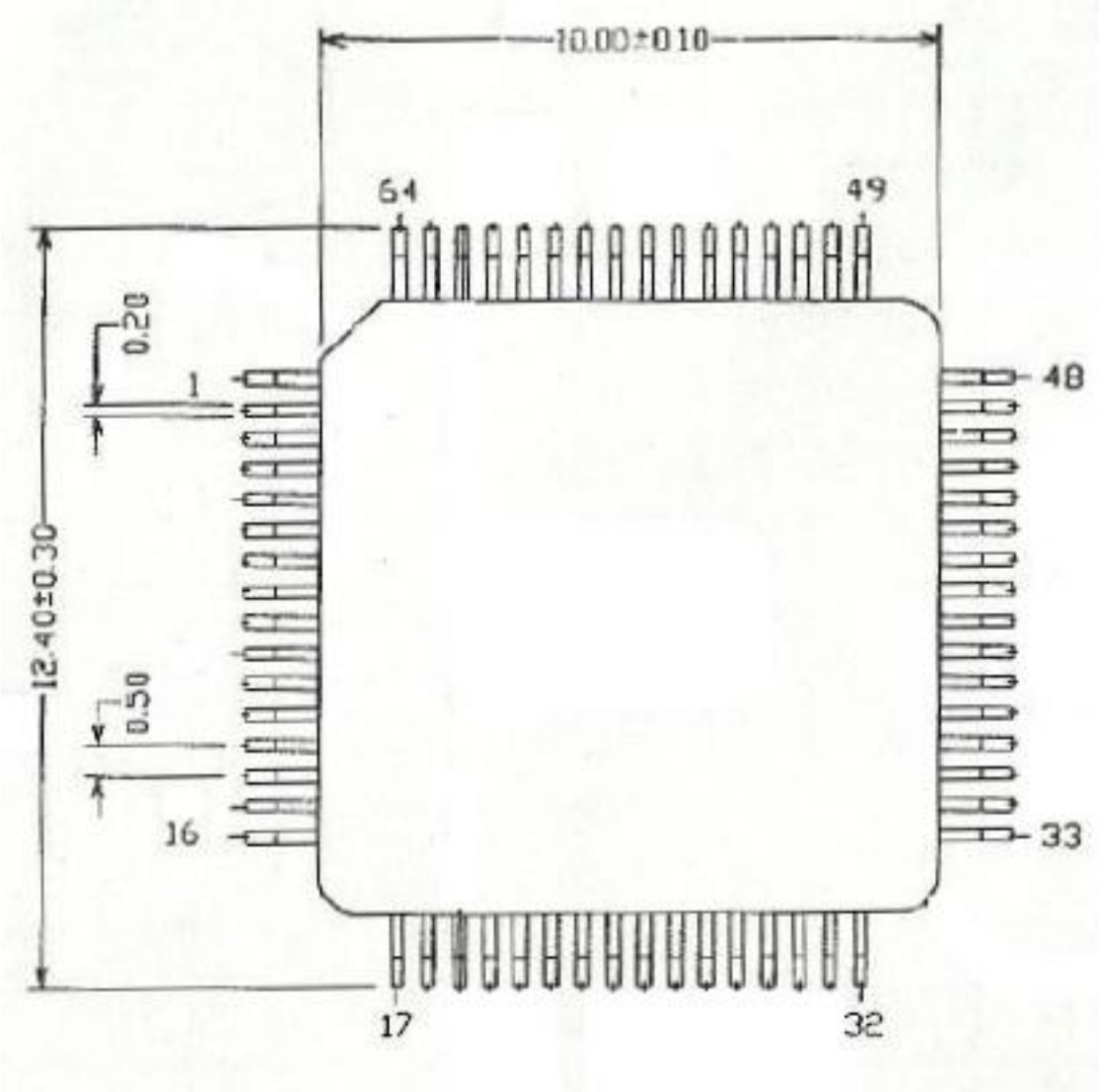


Figure-13: Package Drawing

REVISION HISTORY:

Revision History			
SI. No.	**Version**	**Date of release**	**Description**
1	1.0	March 22,2022	
2			
3			
4			

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