2 MBit Synchronous SRAM

(SC1702-0)

DATA SHEET

Version-1.2, January 2021

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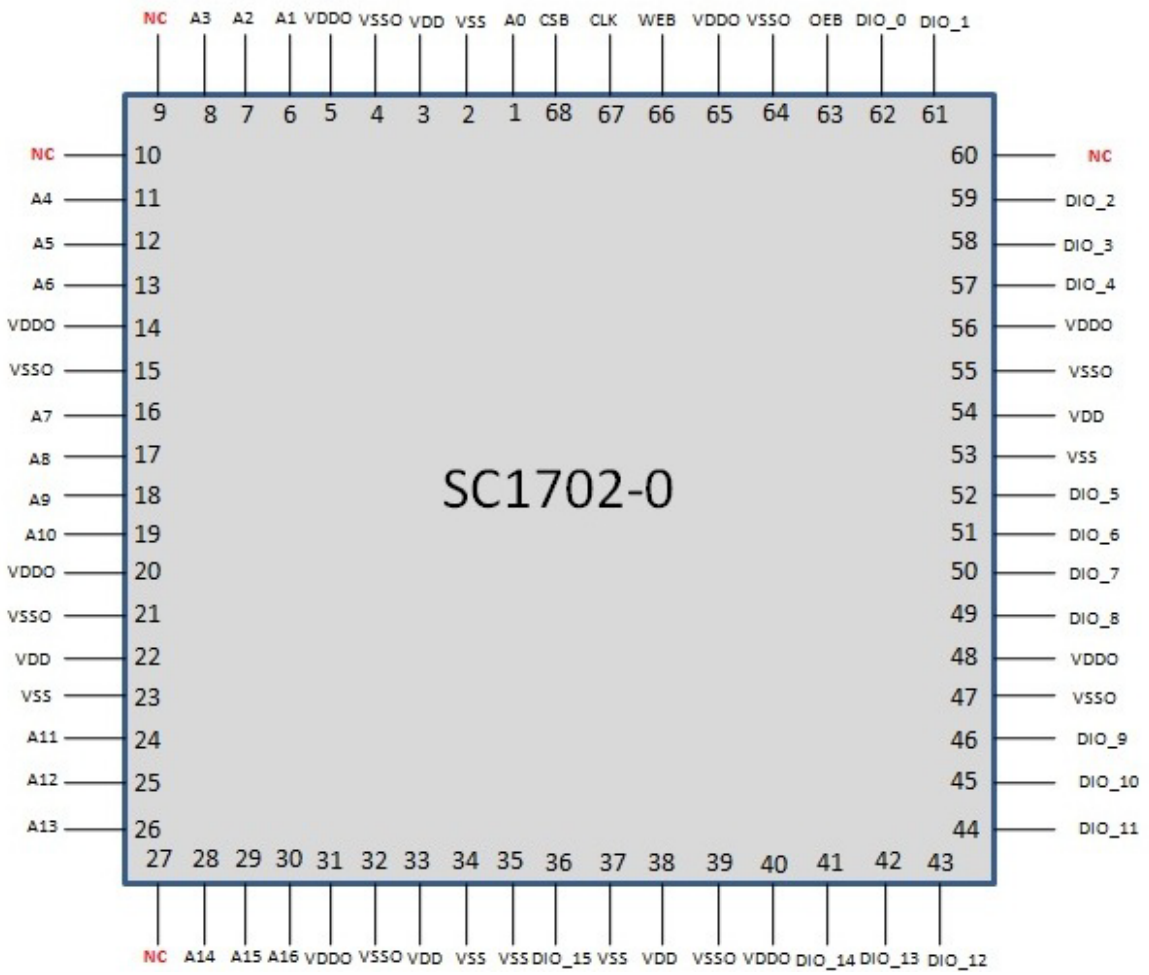
PRODUCT DESCRIPTION:

SC1702-0 is 2 MBit Synchronous SRAM. Memory has 17 address lines (A0 to A16) and 16 data lines (DIO_0 to DIO_15). A Chip Select (CSB) pin allows the user to deselect the device when desired. If CSB is high, no new memory operation is initiated. No operations will be performed on falling edge of CLK. WEB controls read and write operations. OEB enables and disables (Hi-Z) data outputs in read operations (WEB=H).

FEATURES:

- **Power Supply for I/O pads 3.3V ± 10%**
- **Power Supply for Core 1.8V ± 10%**
- **High speed 40 MHz operation**
- **Access Time 10ns**
- **Operating Temperature -55ºC to 125ºC**
- **Designed in SCL's 180nm CMOS process technology**
- **Packaged in 68 lead CQFJ**

PIN CONFIGURATION:



FUNCTIONAL TABLE:

CLK	WEB	CSB	OEB	DIO_0 - DIO_15	Function
X	X	H	X	High-Z	Disabled
↑	H	L	H	High-Z	Read Data (Output Disabled)
↑	H	L	L	D_{OUT}	Read Data
↑	L	L	X	D_{IN}	Write Data
↓	X	L	X	-	No Operation

PIN DESCRIPTION:

Pin no.	Signal	Pin no.	Signal	Pin no.	Signal	Pin no.	Signal
1	A0	18	A9	35	VSS	52	DIO_5
2	VSS	19	A10	36	DIO_15	53	VSS
3	VDD	20	VDDO	37	VSS	54	VDD
4	VSSO	21	VSSO	38	VDD	55	VSSO
5	VDDO	22	VDD	39	VSSO	56	VDDO
6	A1	23	VSS	40	VDDO	57	DIO_4
7	A2	24	A11	41	DIO_14	58	DIO_3
8	A3	25	A12	42	DIO_13	59	DIO_2
9	NC	26	A13	43	DIO_12	60	NC
10	NC	27	NC	44	DIO_11	61	DIO_1
11	A4	28	A14	45	DIO_10	62	DIO_0
12	A5	29	A15	46	DIO_9	63	OEB
13	A6	30	A16	47	VSSO	64	VSSO
14	VDDO	31	VDDO	48	VDDO	65	VDDO
15	VSSO	32	VSSO	49	DIO_8	66	WEB
16	A7	33	VDD	50	DIO_7	67	CLK
17	A8	34	VSS	51	DIO_6	68	CSB

ABSOLUTE MAXIMUM RATINGS (1):

Over operating free-air temperature range (unless otherwise noted),

PARAMETER	UNIT
V_{DDO} , I/O Pads Supply Voltage Range	–0.5 V to 4.3V
V_{DD} , Core Supply Voltage Range	–0.5 V to 2.2V
V_I , Input Voltage Range	–0.5 V to V_{DDO} +0.5
Max. Junction Temperature (T_J)	150°C
T_{stg} , Storage Temperature Range	–65°C to 150°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS:

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DDO}	Supply voltage	2.97	3.3	3.63	V
V_{DD}	Core Voltage	1.62	1.8	1.98	V
V_{IL}	Low level input voltage	0	-	$0.3V_{DDO}$	V
V_{IH}	High level input voltage	$0.7V_{DDO}$	-	V_{DDO}	V
V_{OL}	Low level output voltage (I_{OL} = 4mA)	0	-	0.3	V
V_{OH}	High level output voltage (I_{OH} = -4mA)	3.0	-	V_{DDO}	V
T_A	Free Air Operating Temperature	-55	-	+125	ºC

Power-Up Sequence: Both the supply voltages V_{DDO} (3.3V) & V_{DD} (1.8V) can be applied simultaneously. Ensure that voltage at V_{DDO} pins should not power-up before voltage at V_{DD}.

Power-Down Sequence: Both the supply voltages V_{DDO} (3.3V) & V_{DD} (1.8V) can be down simultaneously. Ensure that voltage at V_{DD} pins should not power-down before voltage at V_{DDO}.

DC ELECTRICAL SPECIFICATIONS:

Test Condition: V_{DDO}=3.3 ± 0.3V, V_{DD}=1.8 ± 0.18V, V_{SSO} = V_{SS} = 0V, T_{AMB} = -55°C to +125°C (unless otherwise noted)

Symbol	Parameter	Test Conditions	Test Results			Units
			Min.	Typ.(1)	Max.	
I_I	Control and Address Inputs Leakage Current (V_{DDO} = 3.63V, V_{DD}=1.98V)	V_{IN} = V_{DDO}	-	±10	±100	nA
		V_{IN} = 0	-	±10	±100	nA
	Data Inputs Leakage Current (V_{DDO} = 3.63V, V_{DD}=1.98V)	V_{IN} = V_{DDO}	-	±10	±100	nA
		V_{IN} = 0	-	±10	±100	nA
V_{OL}	Low Level Output Voltage (V_{DDO} = 3.3V, V_{DD}=1.8V)	I_{OL} = 0	V_{SS}	0.01	0.05	V
		I_{OL} = 4mA	V_{SS}	0.07	0.3	V
V_{OH}	High Level Output Voltage (V_{DDO} = 3.3V, V_{DD}=1.8V)	I_{OH} = 0	3.25	3.29	V_{DDO}	V
		I_{OH} = -4mA	3.0	3.17	V_{DDO}	V
I_{DD}	Static Core Supply Current at V_{DD}	V_{IN}=V_{DDO}	-	0.02	2.0	mA
		V_{IN}=V_{SSO}	-	0.02	2.0	mA
I_{DDO}	Static I/O Pads Supply Current at V_{DDO}	V_{IN}=V_{DDO}	-	0.02	0.1	mA
		V_{IN}=V_{SSO}	-	0.02	0.1	mA
Dynamic I_{DD}	Average Dynamic Supply Current (No Load, CL=30pF)	V_{DD} =1.8V 10 MHz 20MHz	-	 2.0 3.7	 10 10	mA
		V_{DDO} =3.3V 10 MHz 20MHz	-	 17 28	 30 40	mA

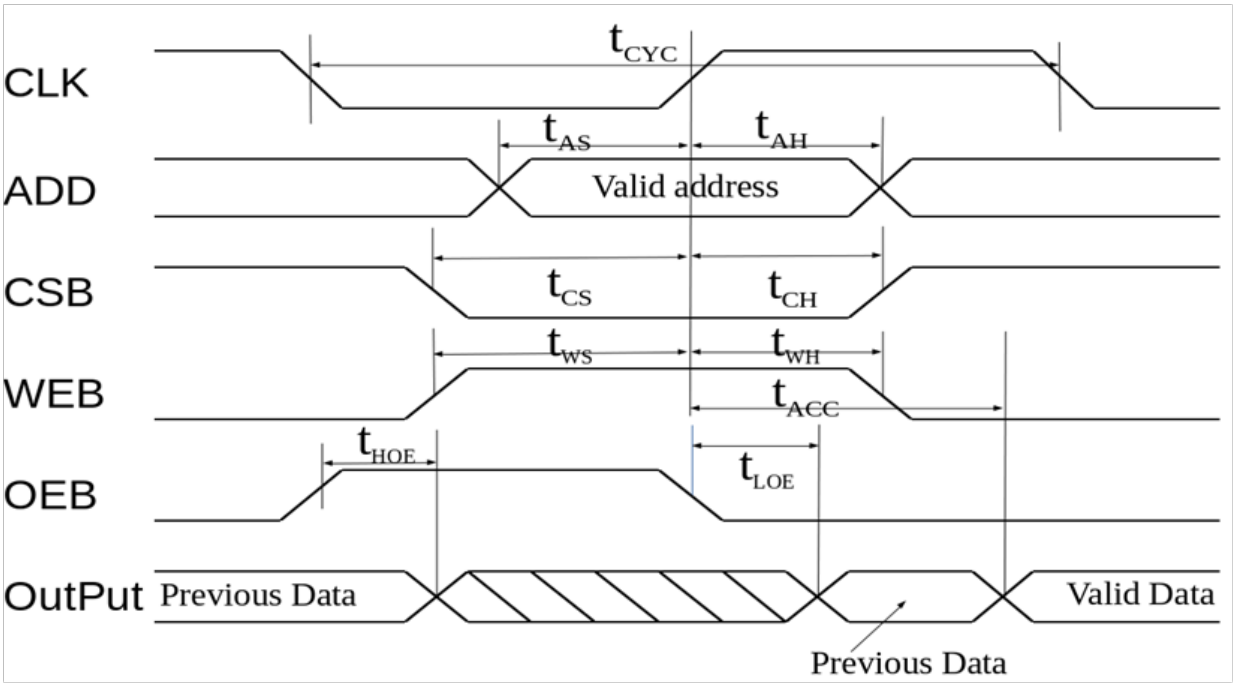
AC ELECTRICAL SPECIFICATIONS:

Test Condition: V_{DDO}=3.3 ± 0.3V, V_{DD}=1.8 ± 0.18V, V_{SSO} = V_{SS} = 0V, T_{AMB} = -55°C to +125°C

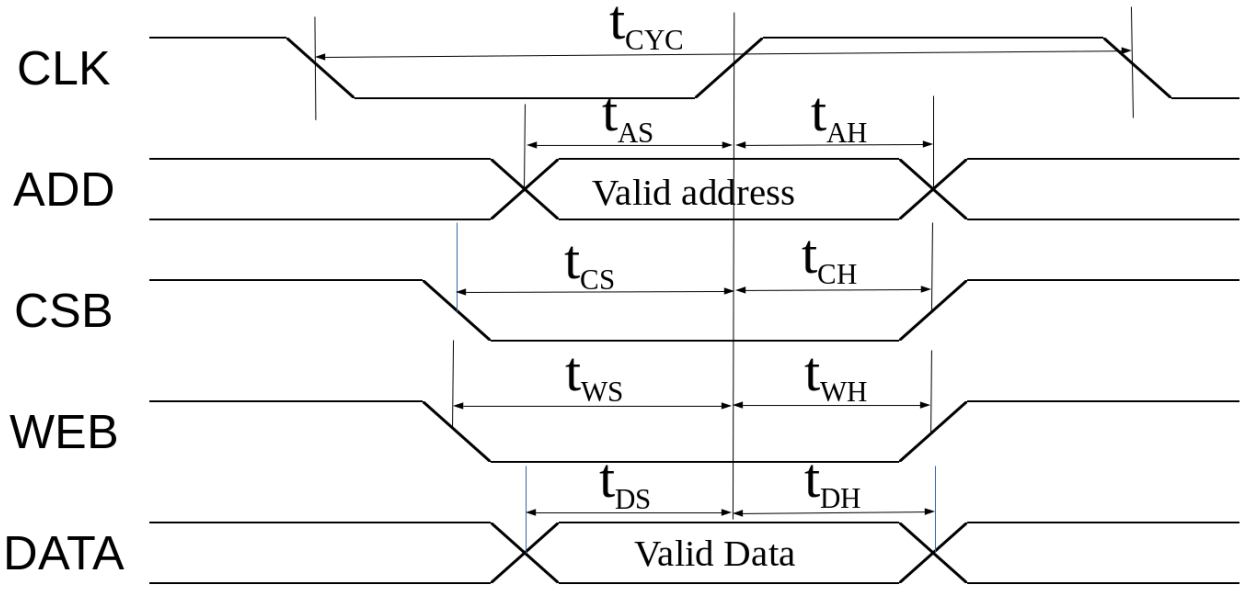
Symbol	Parameter	Min.	Typ.(1)	Max.	Unit
t_{CYC}	Clock Cycle Time	25	-	-	ns
t_{ACC}	Access Time	7	10	14	ns
t_{AS}	Address Setup Time	2.4	2.6	2.8	ns
t_{AH}	Address Hold Time	1.0	1.4	1.8	ns
t_{DS}	Input Data Setup Time	0.8	1.5	2.5	ns
t_{DH}	Input Data Hold Time	0.8	1.2	1.8	ns
t_{WS}	Write Enable Setup Time	3.8	4.1	4.4	ns
t_{WH}	Write Enable Hold Time	0.8	1.2	1.6	ns
t_{CS}	Chip Select Setup Time	1.1	1.5	3.0	ns
t_{CH}	Chip Select Hold Time	0.5	1.0	1.5	ns
t_{LOE}	Output Enable time	3.1	3.5	4.2	ns
t_{HOE}	Output Disable Time	2.2	2.6	4.4	ns

(1) Typical Values are measured at V_{DDO}=3.3V, V_{DD}=1.8 V, V_{SSO} = V_{SS} = 0V, T_{AMB} = 25°C.

Timing Diagrams:

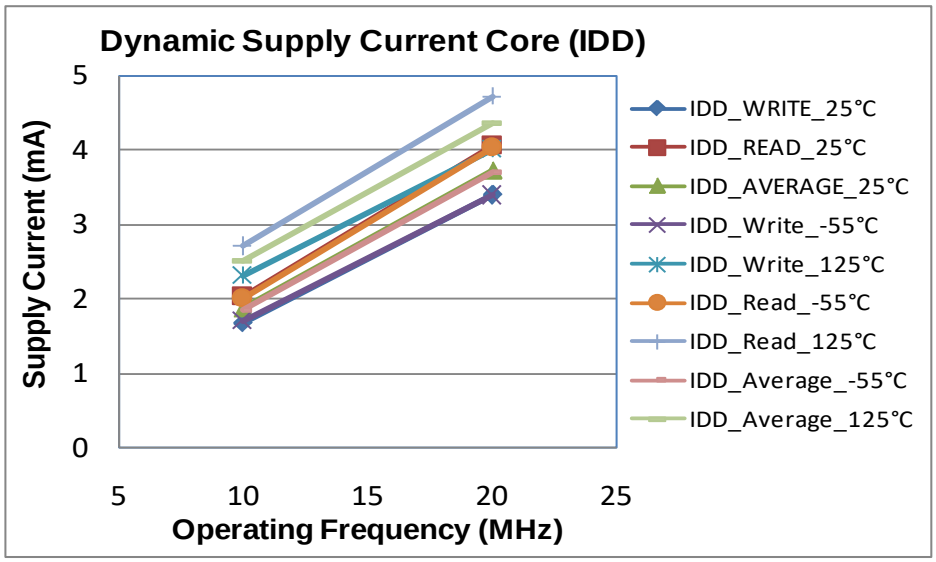


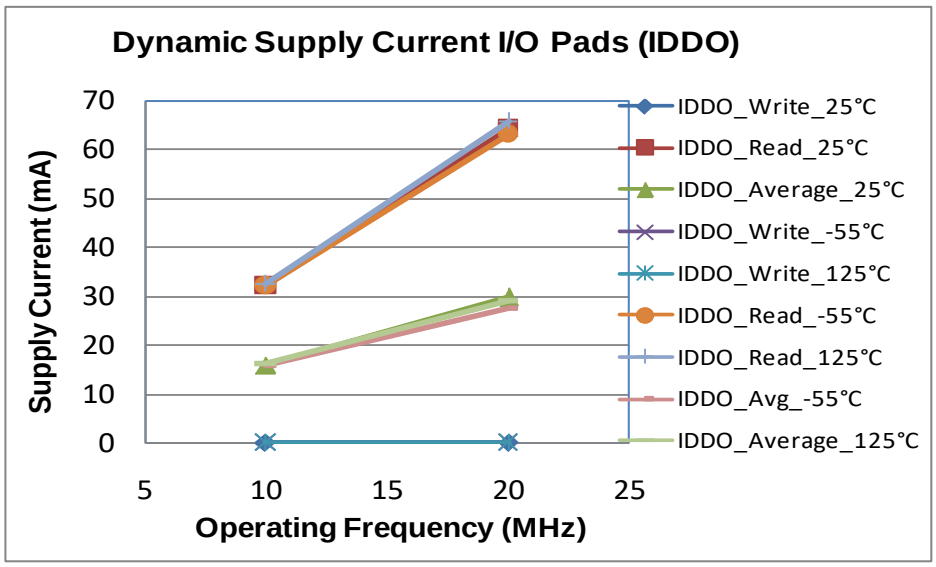
Timing Diagram Read Cycle

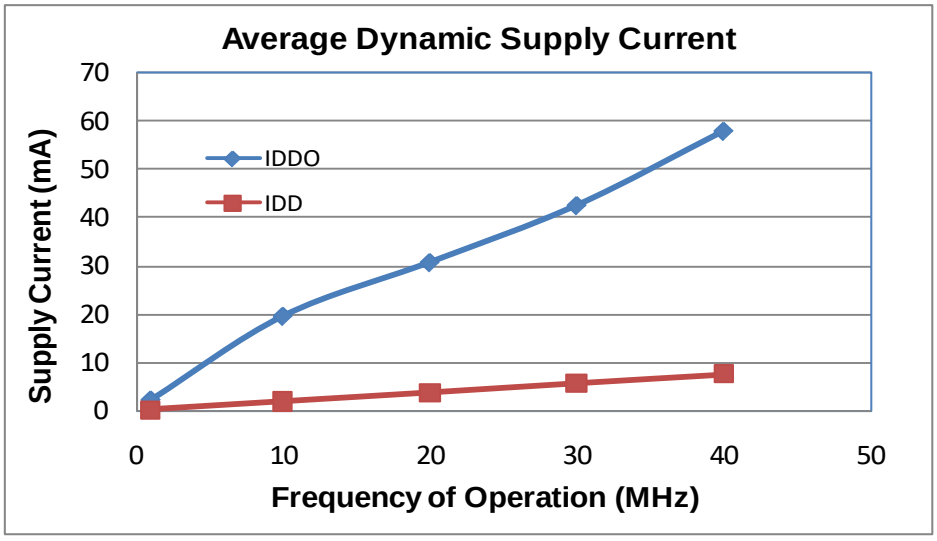


Timing Diagram Write Cycle

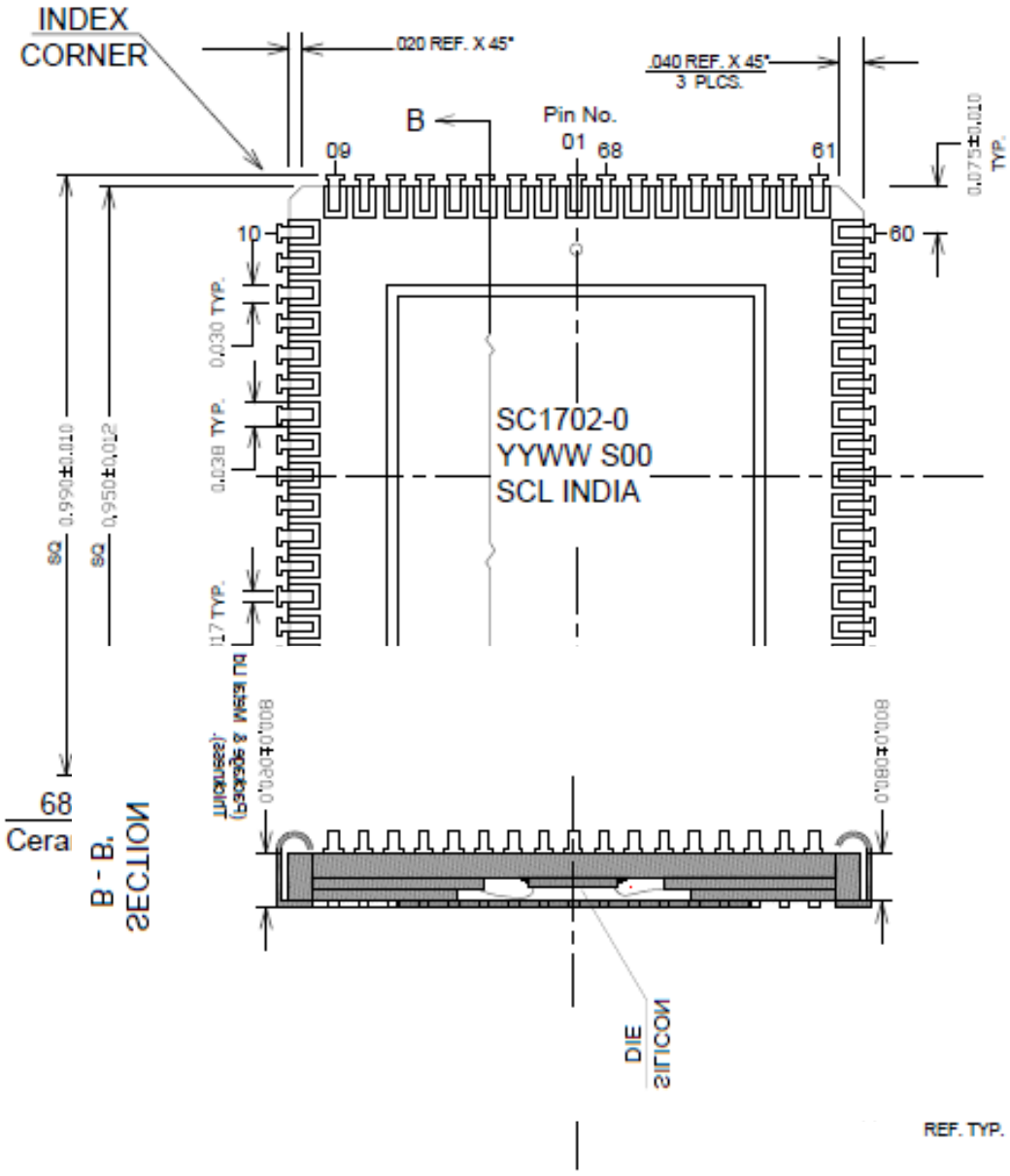
Dynamic Supply Current Characteristics (V_{DDO}=3.3V, V_{DD}=1.8V)







PACKAGE DRAWING (68 Pin CQFJ):
NOTE: All linear dimensions are in inches (mm.)



Revision History:

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S. No.	**Version**	**Release Date**	**Description**
1	DRAFT	April 2017	Draft Release
2	DRAFT	October 2019	Modified Draft Release (Simulation AC Timings Added)
3	Version-1.0	January 2020	AC Timings characterized and modified
4	Version-1.1	December 2020	Power-Up & Power-Down sequence added in Recommended Operating Conditions
5	Version-1.2	January 2021	AC Electrical Specification Table Modified