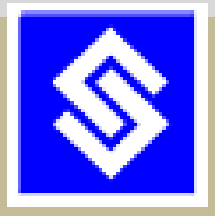
RS422 Transceiver

SC1604-0

Preliminary Datasheet

Version 1.0, April 2017



Semi–Conductor Laboratory

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PRODUCT DESCRIPTION:

RS422 (SC1604-0) is a low power differential line transceiver designed for multi-point data transmission standard RS422 applications. The CMOS design offers significant power saving over its bipolar counterpart without sacrificing ruggedness against ESD damage. It offers a choice of active-high or active-low inputs. The device is designed for line/bus transmission at switching rates up to 5 MHz

FEATURES:

- **Operates From Single 3.3V V_{CC}**
- **Switching Rates up to 5 MHz**
- **Transmission Rate to 10 Mbps**
- **Designed for RS422 applications**
- **Fail safe feature guarantees high output state when receiver inputs are left open.**
- **Common Mode Output Voltage Range: 0V to 3V**

DEVICE SUMMARY:

Silicon No.	Package	Pins	Lead Finish	Description	Temp. range
SC1604-0	DIP	16	Gold	RS422 Transceiver	-40 to +125 °C

Table 1: Device Summary

PIN CONFIGURATION:

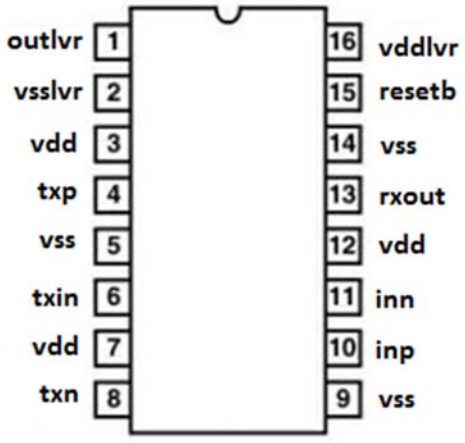

Figure-1: Device Pin diagram

LOGIC DIAGRAM:

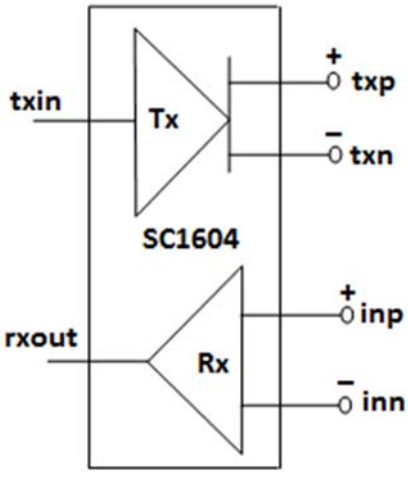

Figure-2: Device Logic Diagram

PIN DESCRIPTION:

SYMBOL	PIN	PIN DESCRIPTION
vdd	3,7,12	Supply Voltage (3.3V)
vddlvr	16	3.3V supply of LVR
resetb	15	Active low regulator reset
txin	6	Driver input
txp, txn	4, 8	Driver outputs
rxout	13	Receiver output
outlvr	1	Output of LVR
Inp, inn	10, 11	Receiver inputs
vss & vsslvr	5,9,14 & 2	Ground (0V)

Table-2: Device Pin description

***0.1uF Capacitor must be between connected lvrout and vsslvr Pins.**

FUNCTIONAL TABLE:

Driver			Receiver		
Input	Output		Input		Output
1	H	L	1	0	H
0	L	H	0	1	L

Table 3: Truth table

BASIC DC-PARAMETER TESTING & TEST CONDITIONS:

Test name	Test Parameter	Pins Tested	Force	Min	Typ.	Max	Unit
ESD Diode Test	Positive Diode	All Input / Output Pins	100uA	416.175		541.205	mV
	Negative Diode		-100uA	-569.982		-479.224	
Static supply current	I_{DD}	All inputs Low	VDD = 3.3V VIL=0V		944.074		nA
		All Inputs High	VDD = 3.3V VIH=3.3V		944.074		
Static supply current of LVR	$I_{DD\ LVR}$	All inputs Low	VDD = 3.3V VIL=0V	4.541		4.749	mA
		All Inputs High	VDD = 3.3V VIH=3.3V	4.541		4.673	

Input Gate Leakage Test (VDD = 3.3V)	IIL	Inputs (txin, Resetb)	V_{IN} = 0V	-0.170		-0.063	µA
	IIH		V_{IN} = 3.3V	-0.039		0.016	
	IIL	Inputs (inn, inp)	V_{IN} = 0V	-7.071		-2.924	
	IIH		V_{IN} = 3.3V	2.391		7.561	
V_{OL}	Output Voltage Low	Load = 0.1mA		0.698		21.973	mV
		Load = 20mA		275.808		311.104	
V_{OH}	Output Voltage High	Load = -0.1mA		3.205		3.287	V
		Load =-20mA		2.860		2.890	

DRIVER ELECTRICAL AND SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Condition		Min	Typical	Max	Unit
$\|V_{OD(SS)}\|$	Steady-State differential output voltage	R_L = 100 Ω Refer Figure 3	Driver Input = 0V		-2.537		V
			Driver Input = 3.3V		2.547		
		V_{CM} = 0V to 3V Refer Figure 4	Driver Input = 0V		-2.032		
			Driver Input = 3V		2.049		
$\Delta\|V_{OD(SS)}\|$	Change in magnitude of Steady-State differential output voltage between states	R_L = 100 Ω Refer Figure 3	Driver Input = 0V		0.010		
			Driver Input = 3.3V		0.017		
$V_{OD(RING)}$	Differential output voltage overshoot and undershoot	R_L = 100 Ω C_L = 50 pF Input PRR=500KHz, 50% Duty Cycle Refer Figure 6	Positive Overshoot		7.933		%
			Negative Overshoot		19.04		
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage	-			To be done		
$V_{OC(SS)}$	Steady-state common-mode output voltage	-			To be done		
I_{DD} (D)	Dynamic Current Supply Test	V_{DD} = 3.3V Input Pulse Rate = 5 MHz			4.9		mA
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 100 Ω C_L = 50 pF			6.2		ns
t_{PHL}	Propagation delay time, high-to-low-level output				7.8		

RECEIVER ELECTRICAL AND SWITCHING CHARACTERISTICS

Parameter	Test Condition	Min	Typical	Max	Unit
Input Sensitivity	V_{CM}= 0 to 3V	50	200		mV
Input Hysteresis	V_{CM}= 1.65V, Refer Figure 9		43		mV
Dynamic Current Supply Test	V_{DD} = 3.3V Input Pulse Rate = 5 MHz		4.8		mA
t_{PLH}	Propagation Delay Refer Figure 10		10.8		ns
t_{PHL}			8.8		ns
Duty Cycle			49.88		%

DRIVER TEST CIRCUITS AND WAVEFORMS:

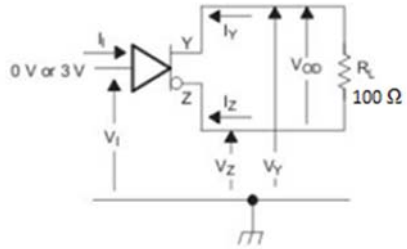

Figure3: Driver VOD Test Circuit

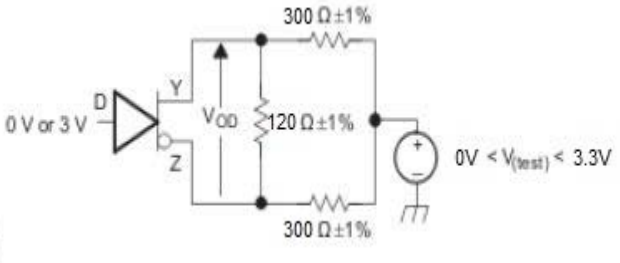

Figure4: Driver VOC Test Circuit

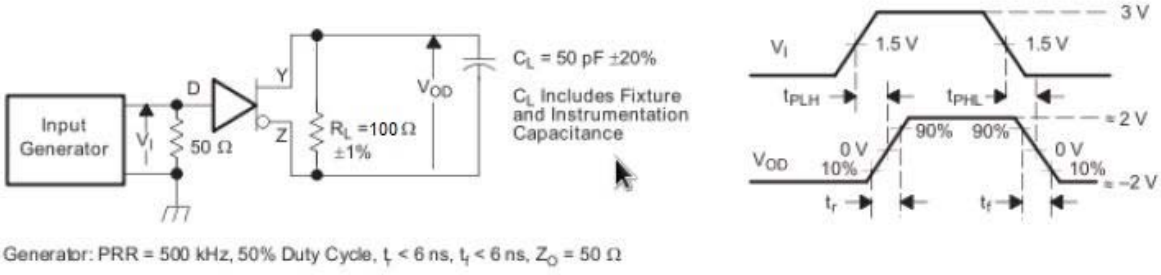

Figure5: Driver Propagation Delay Test Circuit and Waveforms

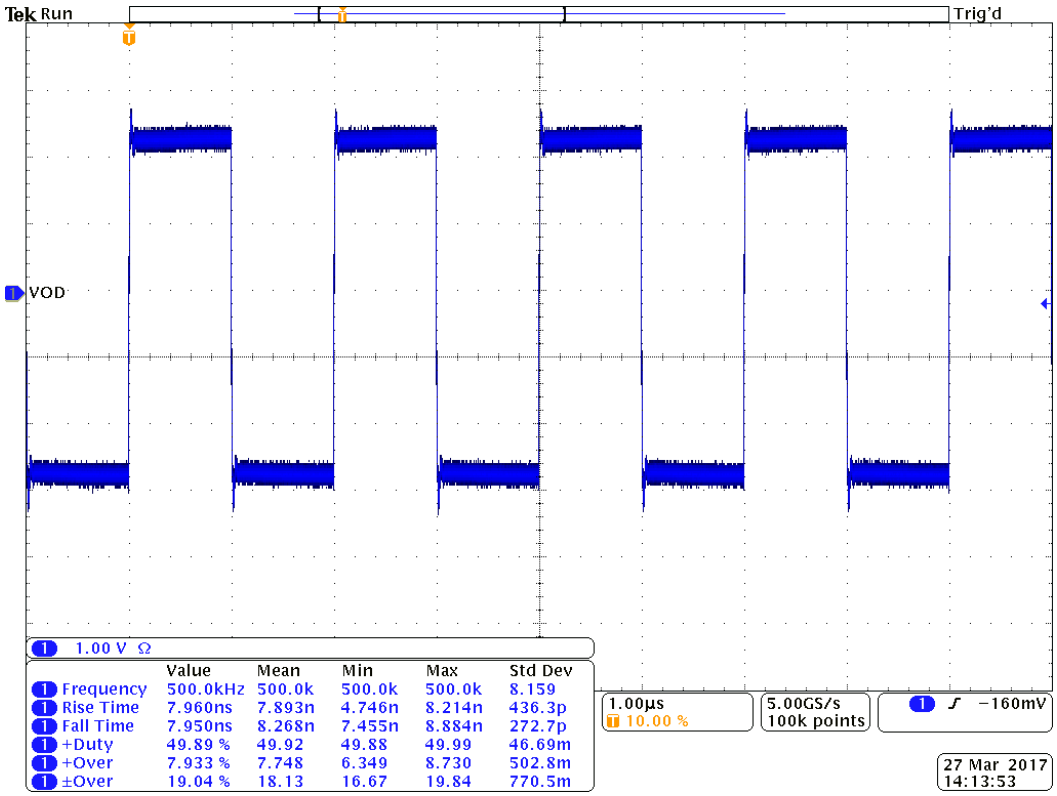

Figure6: The Driver VOD (Ring) Test Waveform

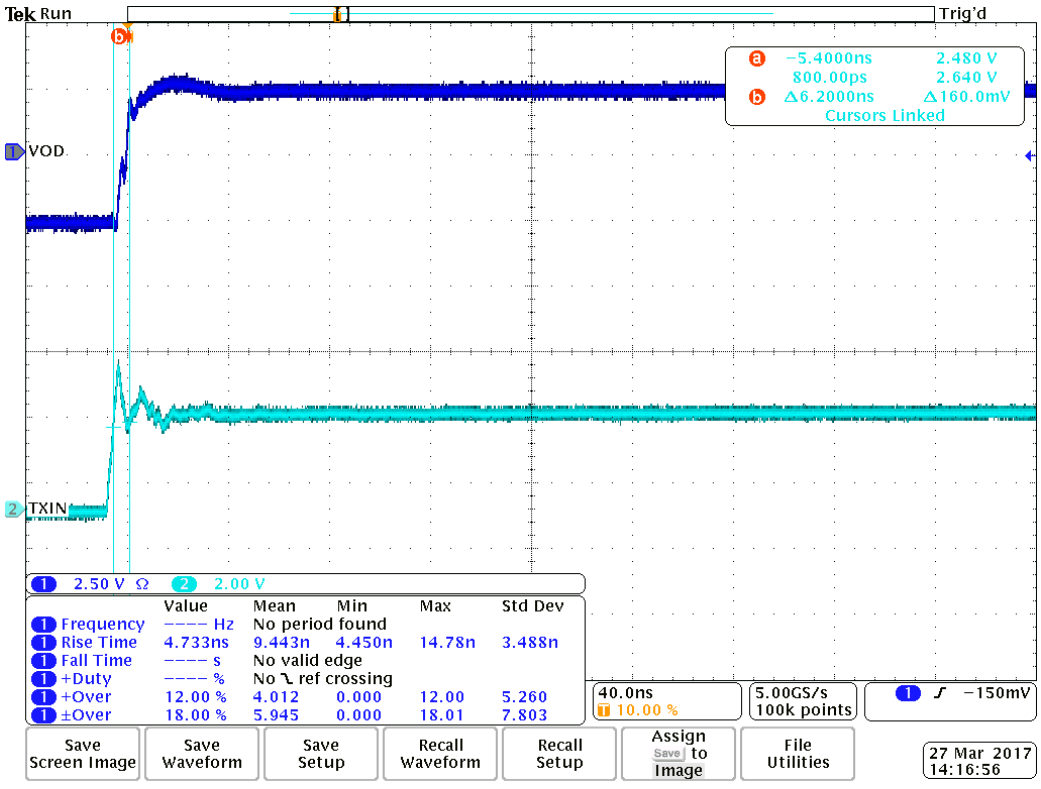

Figure7: Propagation delay time, low-to-high-level output

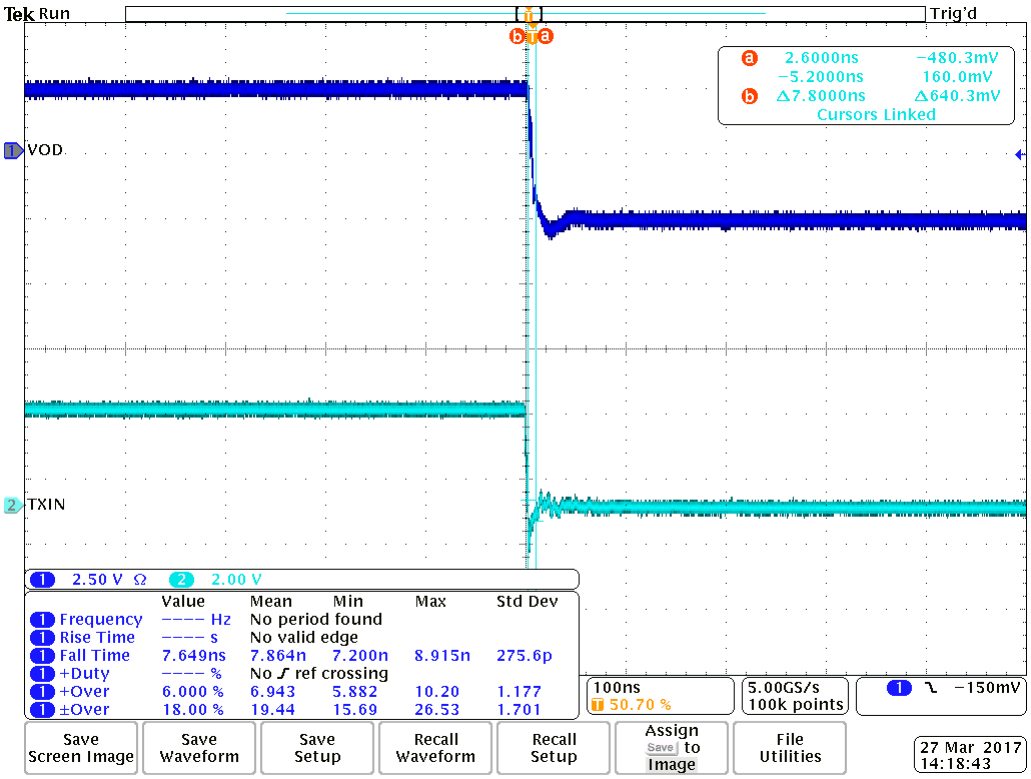

Figure8: Propagation delay time, high-to-low-level output

RECEIVER TEST CIRCUIT AND WAVEFORM:

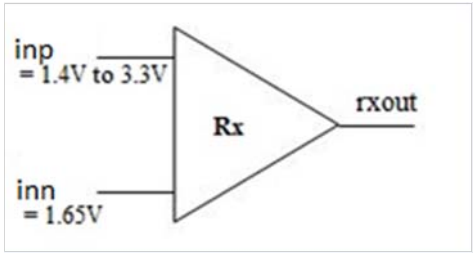

Figure9: Receiver Input Hysteresis Test Circuit

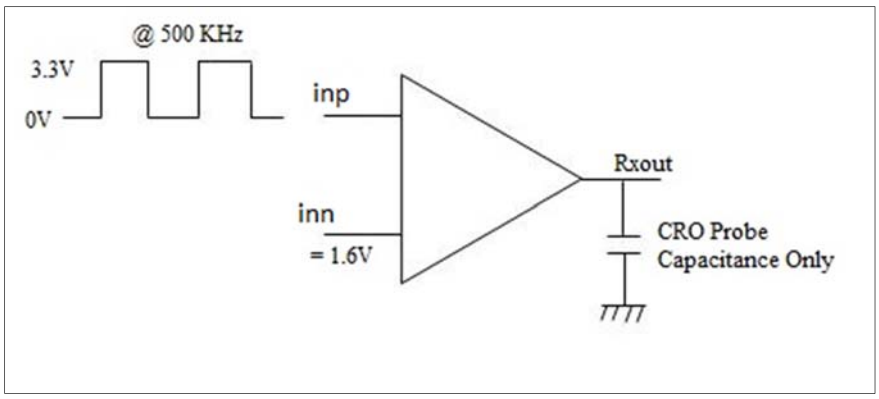

Figure10: Receiver Propagation Delay Test Circuit

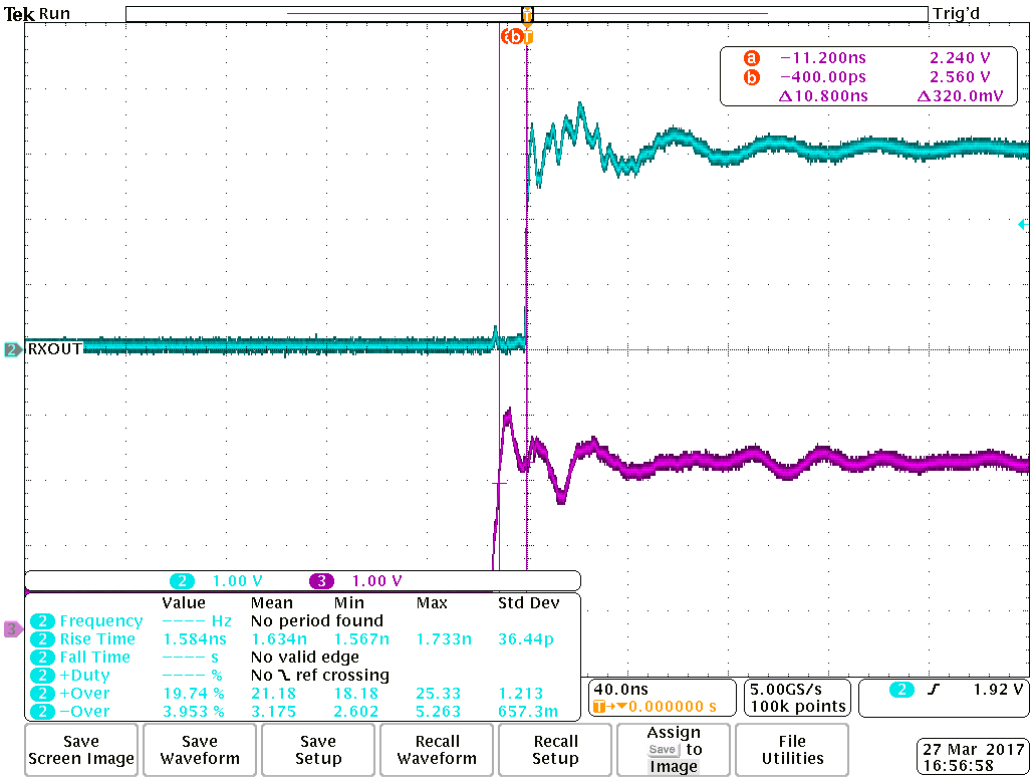

Figure11: Propagation delay time, low-to-high-level output

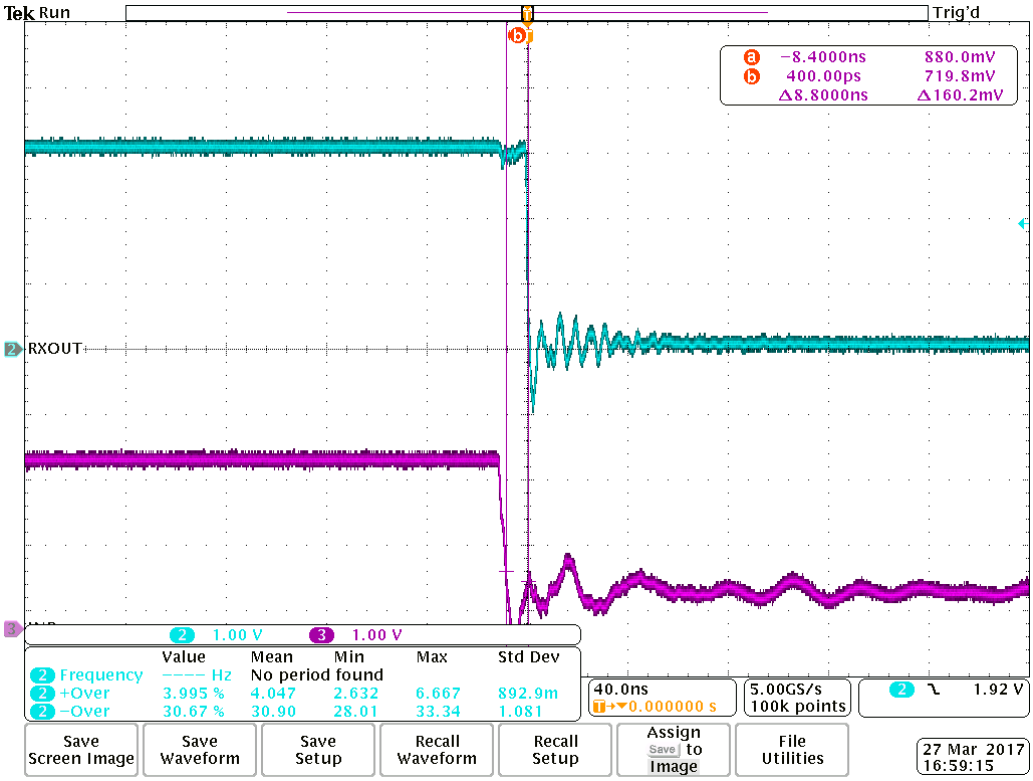

Figure12: Propagation delay time, high-to-low-level output