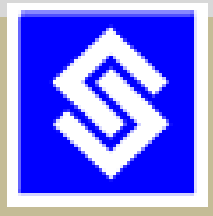
RS485 Transceiver

SC1603-0

DATA SHEET

Version 1.0, Feb 2017



Semi–Conductor Laboratory

Government of India

RS485 Transceiver (SC1603-0)

PRODUCT DESCRIPTION:

RS485 (SC1603-0) is a low power differential line transceiver designed for multi-point data transmission standard RS485 applications. The enable function is different for both transmitter and receiver lines. It offers a choice of active-high or active-low inputs. The device is designed for line/bustransmission at switching rates up to 5 MHz

FEATURES:

- **Operates From Single 3.3V V_{CC}**
- **Switching Rates up to 5 MHz**
- **Transmission Rate to 10 Mbps**
- **Designed for RS485 applications**
- **Fail safe feature guarantees high output state when receiver inputs are left open.**
- **Common Mode Output Voltage Range: 0V to 3V**
- **Operating Temperature:-40°C to 125°C**

DEVICE SUMMARY:

Reference	Package	Pins	Lead Finish
SC1603-0	DIP	16	Gold

Table 1: Device Summary

PIN CONFIGURATION: LOGIC DIAGRAM:

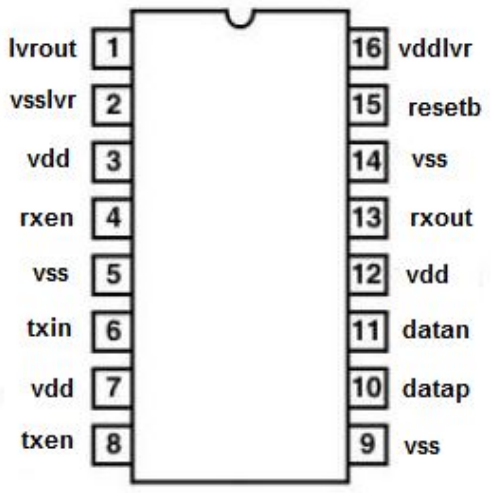


Figure-1: Device Pin diagram

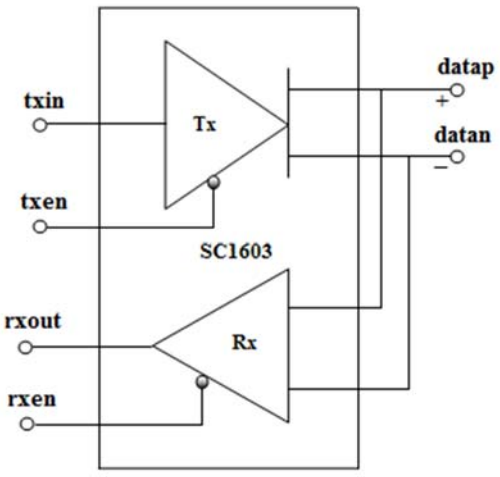


Figure-2: Device Logic Diagram

PIN DESCRIPTION:

SYMBOL	PIN	PIN DESCRIPTION
vdd	3,7,12	Supply Voltage (3.3V)
Vddlvr	16	3.3V supply of LVR
resetb	15	Active low regulator reset pin
txin	6	Driver input
Datap, Datan	10,11	Bidirectional Pins
rxout	13	Receiver output
Lvrout	1	Output of LVR (1.8V)
txen, rxen	8,4	Enable Pins
Vss&vsslvr	5,9,14& 2	Ground (0V)

Table-2: Device Pin description

FUNCTIONAL TABLE:

Driver				Receiver			
Enable	Input	Output		Enable	Input		Output
0	1	H	L	0	1	0	H
0	0	L	H	0	0	1	L

Table 3: Truth table

BASIC DC-PARAMETER TESTING & TEST CONDITIONS:

Test name	Test Parameter		Pins Tested	Force	Min	Typ.	Max	Unit
ESD Diode Test	Positive Diode		All Input / Output Pins	100uA	406.523		561.035	mV
	Negative Diode			-100uA	-564.061		-471.288	
Static supply current	I_{DD}	Tx Mode	All inputs Low	VDD = 3.3V VIL=0V			100	µA
			All Inputs High	VDD = 3.3V VIH=3.3V			100	
		Rx Mode	All inputs Low	VDD = 3.3V VIL=0V			500	nA
			All Inputs High	VDD = 3.3V VIH=3.3V			500	

Static supply current of LVR	$I_{DD\ LVR}$	Tx Mode	All inputs Low	VDD = 3.3V VIL=0V	4.654		4.703	mA
			All Inputs High	VDD = 3.3V VIH=3.3V	4.827		4.887	
Static supply current of LVR	$I_{DD\ LVR}$	Rx Mode	All inputs Low	VDD = 3.3V VIL=0V	4.632		4.695	mA
			All Inputs High	VDD = 3.3V VIH=3.3V	4.514		4.564	
Input Gate Leakage Test (VDD = 3.3V)	IIL		Inputs (txen, rxen, txin, Resetb)	V_{IN} = 0V	-49.4		-11.8	nA
	IIH			V_{IN} = 3.3V	12.1		17.9	
	IIL		Bidirectional (Datap, Datan)	V_{IN} = 0V	-10.18		-0.74	µA
	IIH			V_{IN} = 3.3V	0.04		9.81	

DRIVER ELECTRICAL AND SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Condition		Min	Typical	Max	Unit
$\|V_{OD\ (SS)}\|$	Steady-State differential output voltage	R_L = 54 Ω Refer Figure3	Driver Input = 0V		-2.034		V
			Driver Input = 3.3V		2.092		
		V_{CM} = 0V to 3V Refer Figure4	Driver Input = 0V		-2.113		
			Driver Input = 3V		2.149		
$\Delta\|V_{OD\ (SS)}\|$	Change in magnitude of Steady-State differential output voltage between states	R_L = 54 Ω Refer Figure3	Driver Input = 0V		0.058		
			Driver Input = 3.3V		0.036		
$V_{OD\ (RING)}$	Differential output voltage overshoot and undershoot	R_L = 54 Ω C_L = 50 pF Input PRR=500KHz, 50% Duty Cycle Refer Figure 6	Positive Overshoot		12.98		%
			Negative Overshoot		9.97		
$V_{OC\ (PP)}$	Peak-to-peak common-mode output voltage	Refer Figure 7			0.45		V
$V_{OC\ (SS)}$	Steady-state common-mode output voltage	Refer Figure 7			1.3		
V_{OL}	Output Voltage Low	Load = -0.1mA		0.0114		0.938	mV
		Load = -20mA		281.43		291.96	
V_{OH}	Output Voltage High	Load = 0.1mA		3.192		3.287	V
		Load = 20mA		2.868		2.879	
$I_{DD}(D)$	Dynamic Current Supply Test	V_{DD} = 3.3V Input Pulse Rate = 5 MHz			6.8		mA
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 54 Ω C_L = 50 pF			15		ns
t_{PHL}	Propagation delay time, high-to-low-level output				16		

RECEIVERELECTRICAL AND SWITCHING CHARACTERISTICS

Parameter	Test Condition	Min	Typical	Max	Unit
Input Sensitivity	V_{CM}= 0 to 3V	50	200		mV
Input Hysteresis	V_{CM}= 1.65V, Refer Figure 10		68		mV
Output Voltage High(V_{OH})	Load = -0.1mA		3.286		V
	Load = -20mA		2.886		
Output Voltage Low(V_{OL})	Load = -0.1mA		102.916		mV
	Load = -20mA		282.179		
Dynamic Current Supply Test	V_{DD} = 3.3V Input Pulse Rate = 5 MHz		6.3		mA
t_{PLH}	Propagation Delay Refer Figure 11		5		ns
t_{PHL}			6		ns
Differential Skew	t_{PHL}- t_{PLH}		1		ns
Duty Cycle			49.54		%

DRIVERTEST CIRCUITS AND WAVEFORMS:

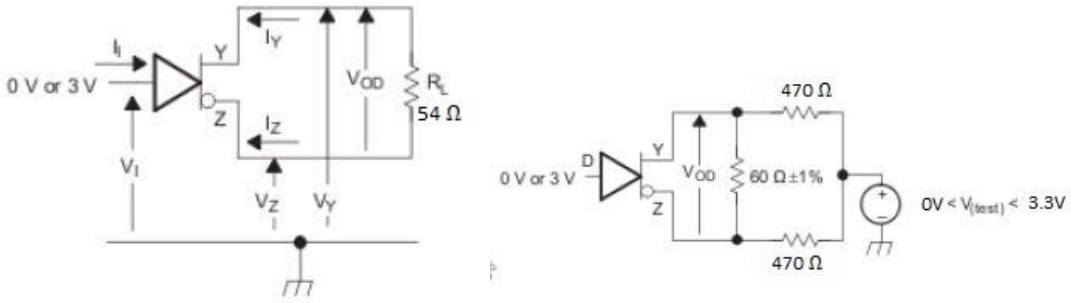


Figure3: Driver VOD Test CircuitFigure4: Driver VOC Test Circuit

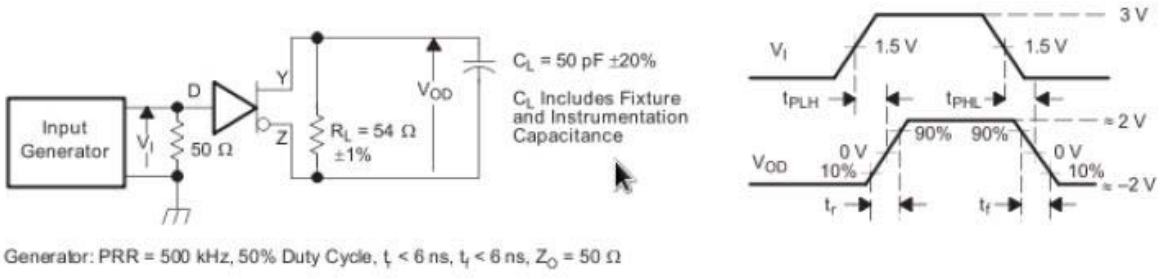


Figure5: Driver Propagation Delay Test Circuit and Waveforms

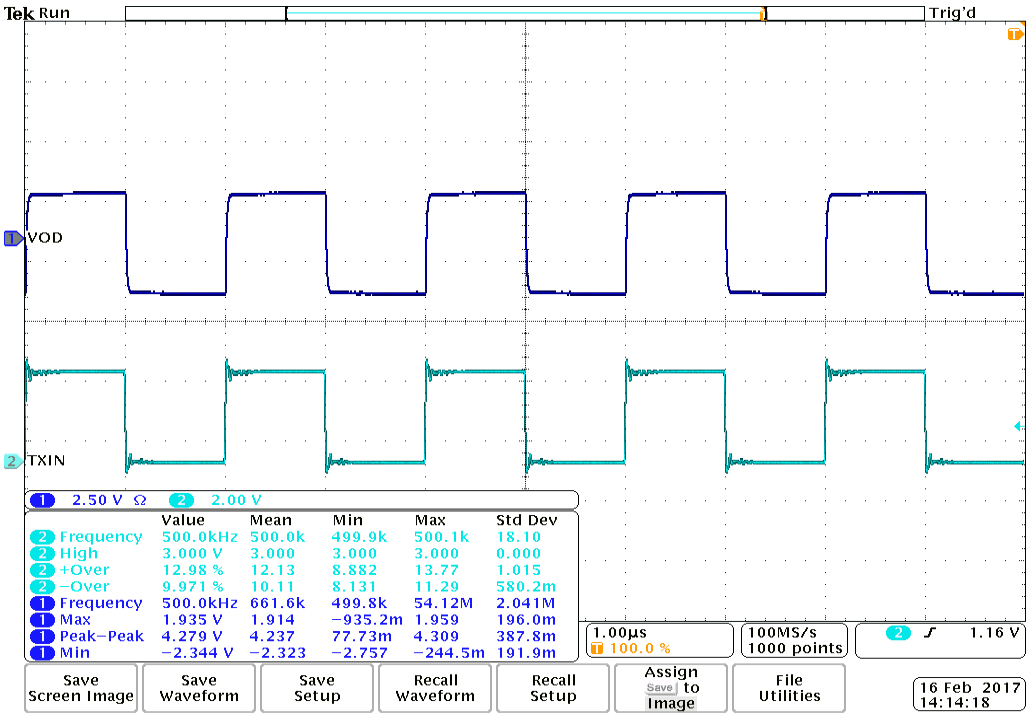


Figure6: The Driver VOD (Ring) Test Waveform

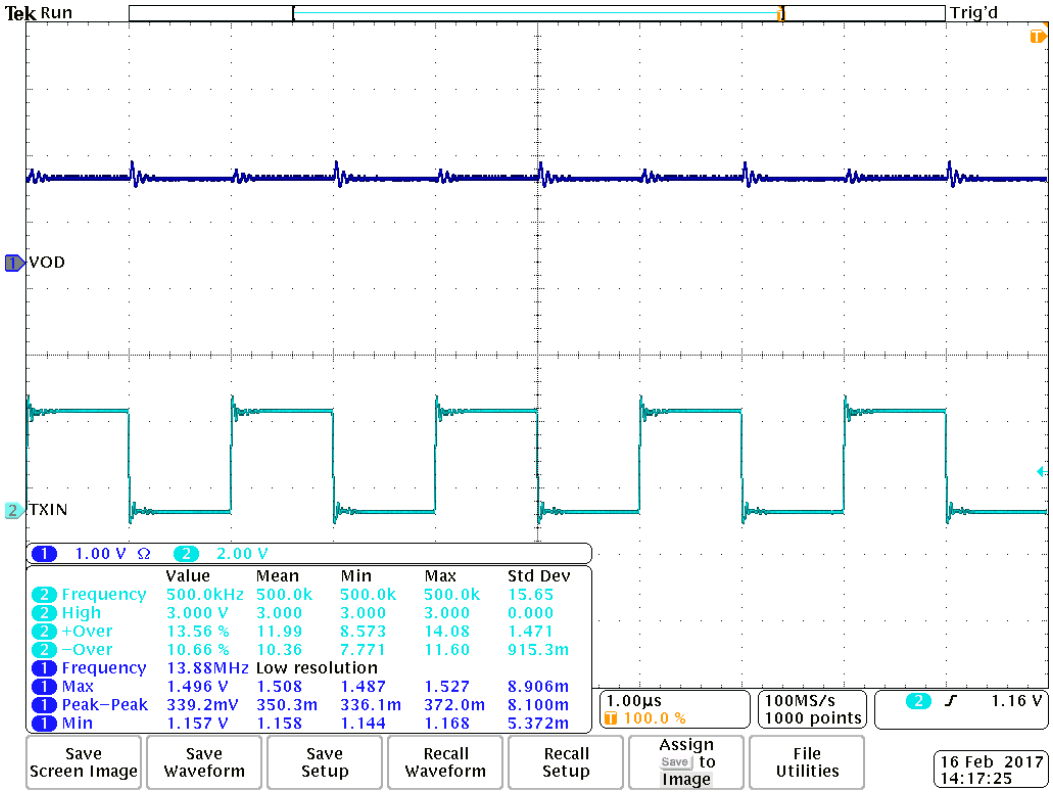


Figure7: The Driver common-mode output voltage

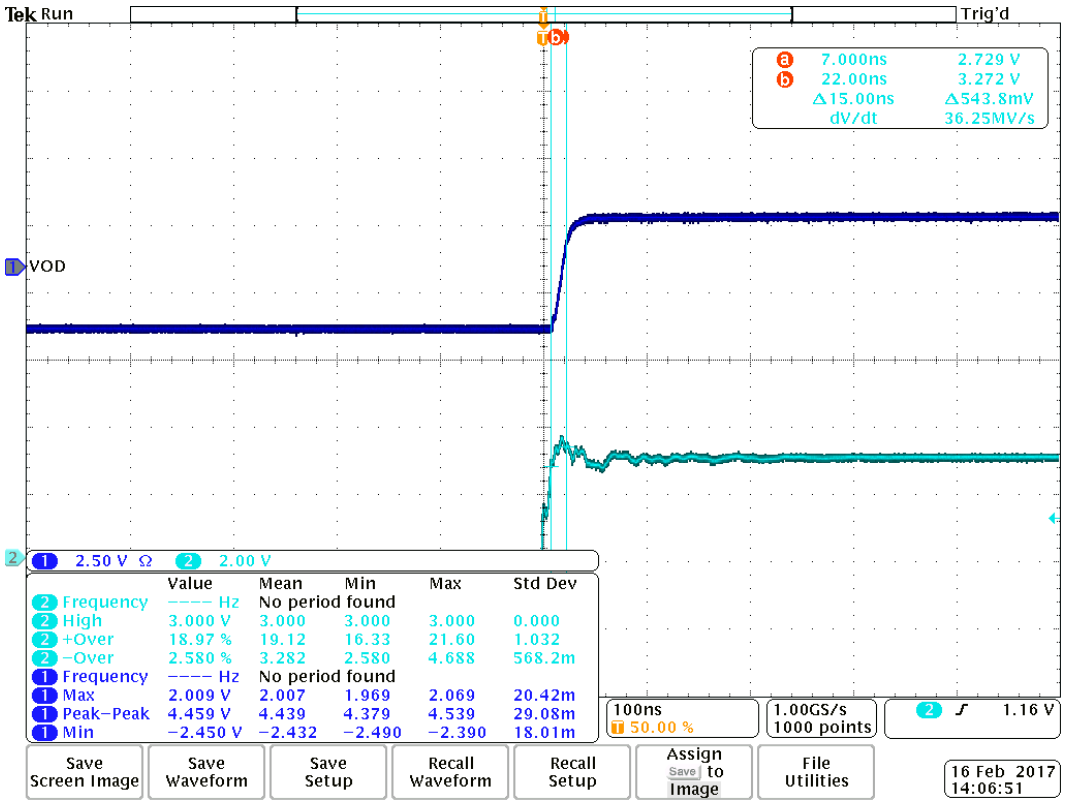


Figure8: Propagation delay time, low-to-high-level output

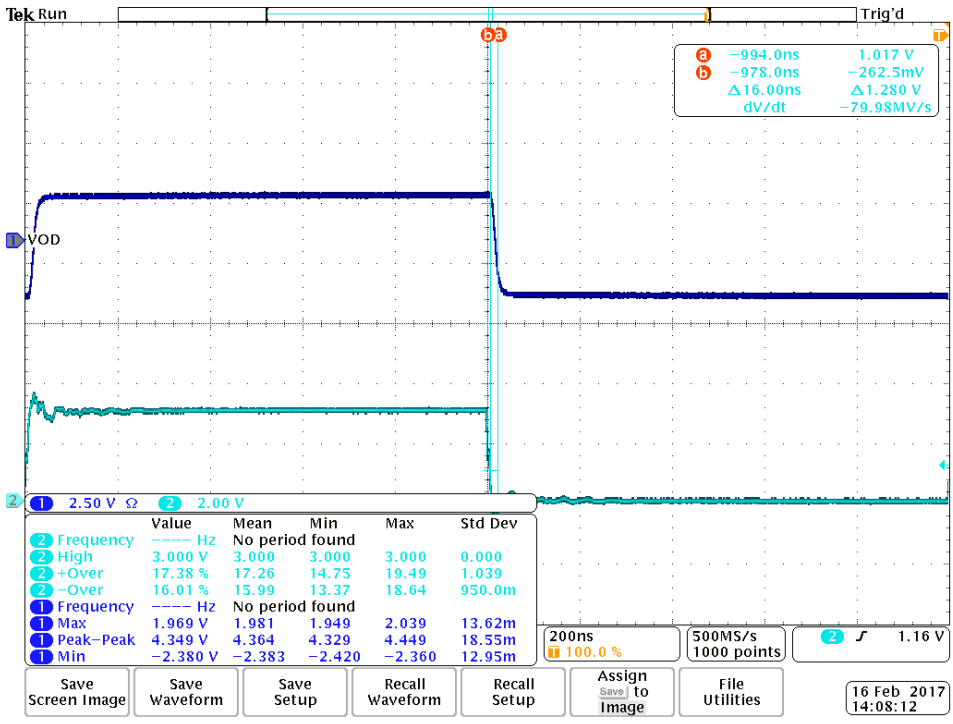


Figure9: Propagation delay time, high-to-low-level output

RECEIVERTEST CIRCUIT AND WAVEFORM:

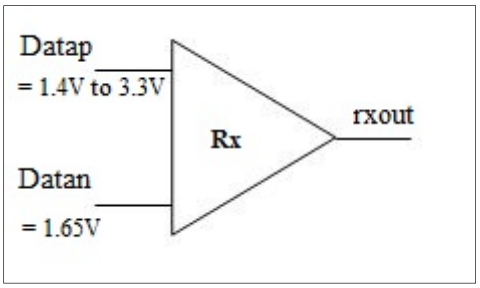


Figure10: Receiver Input Hysteresis Test Circuit

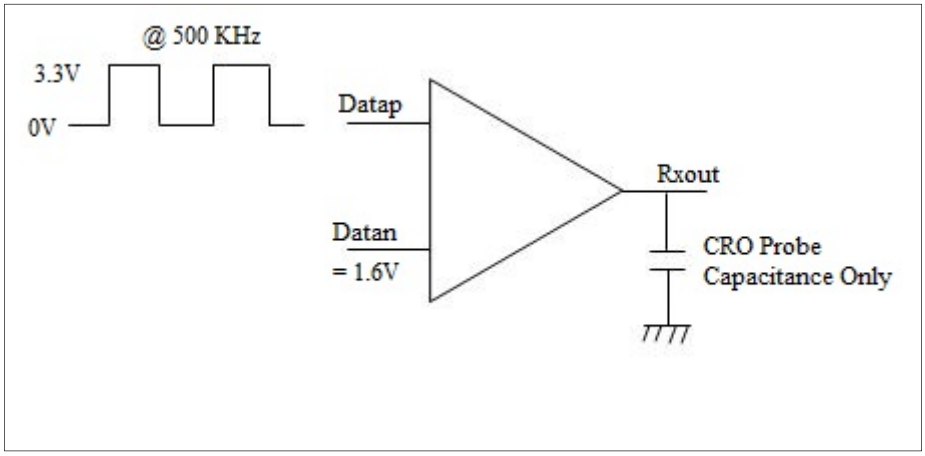


Figure11: Receiver Propagation Delay Test Circuit

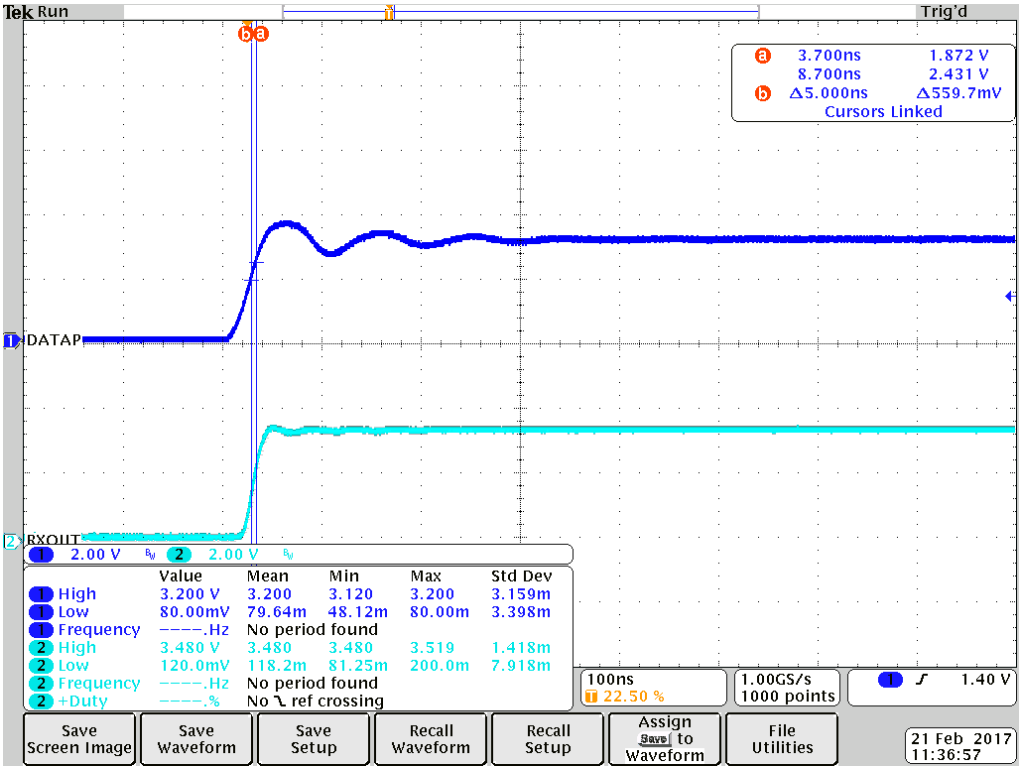


Figure12: Propagation delay time, low-to-high-level output

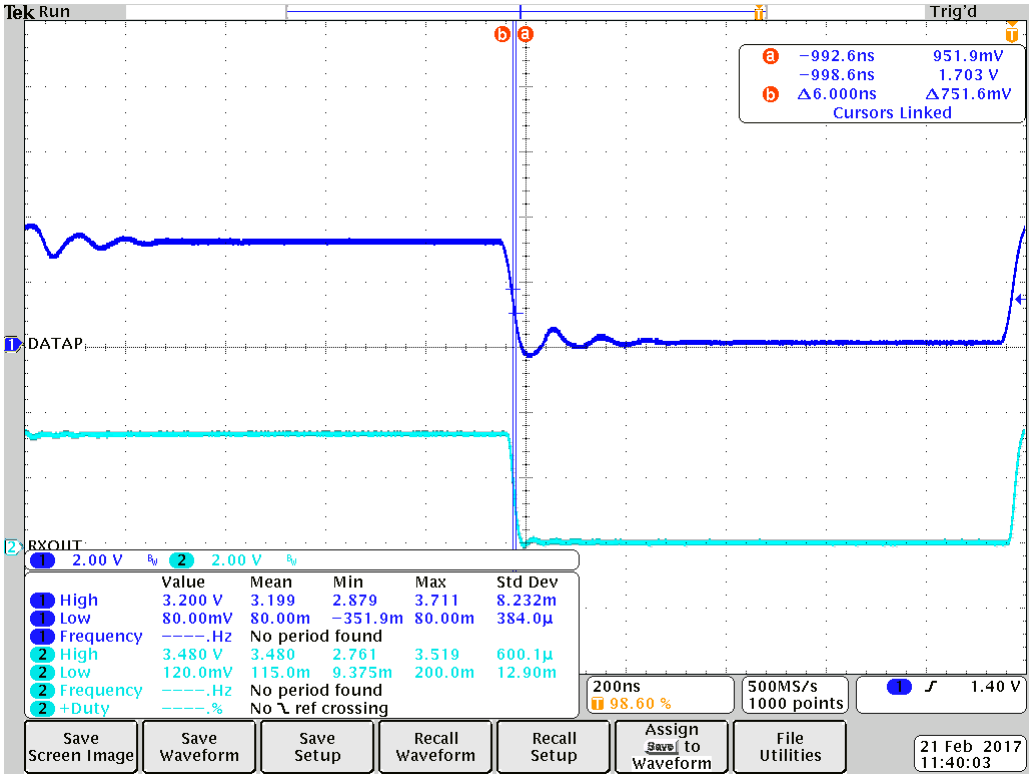
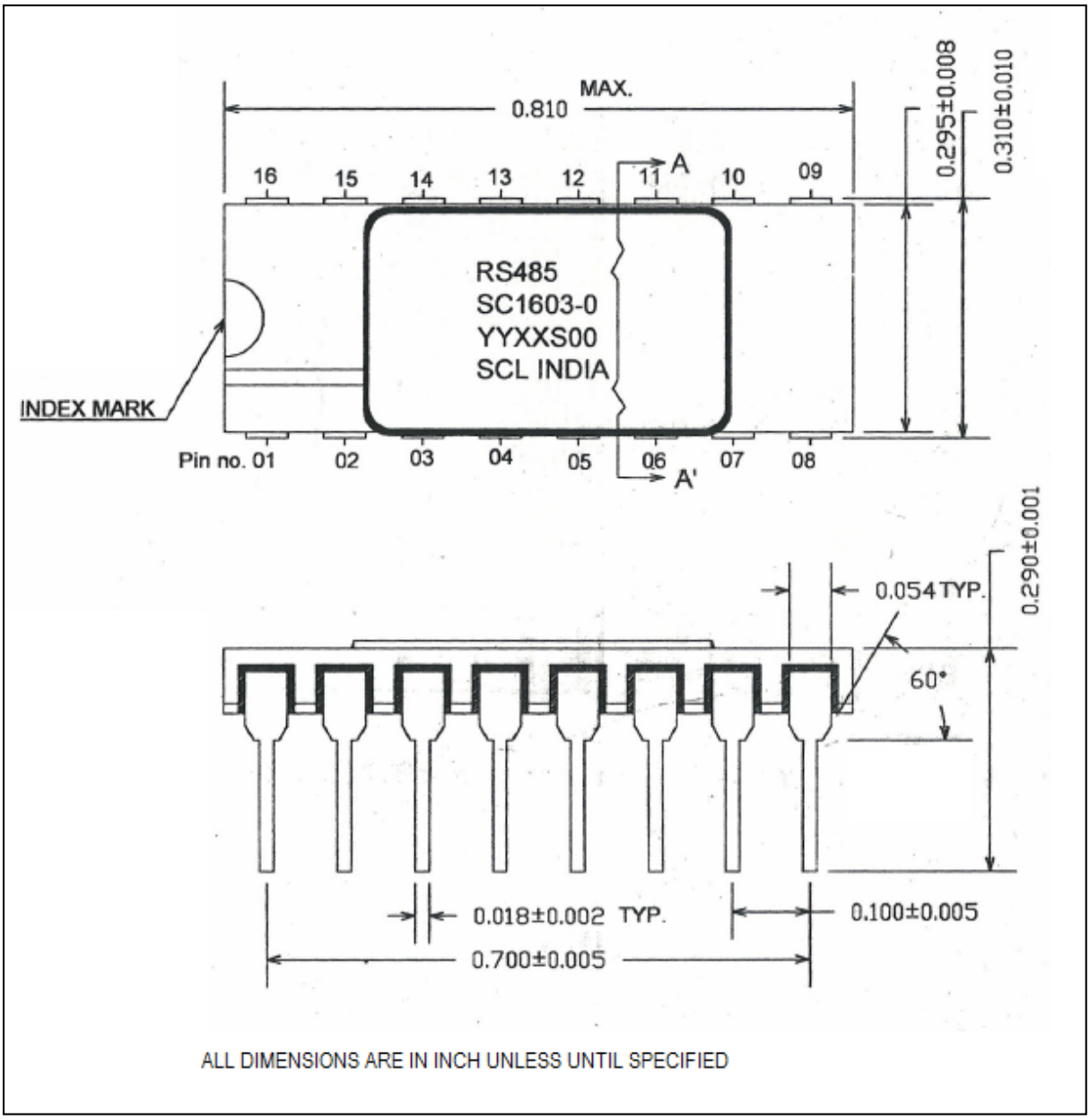


Figure13: Propagation delay time, high-to-low-level output

PACKAGE DIMENSIONS:

16 PIN S/B CERAMIC



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