SC1602-0

PRELIMINARY DATASHEET

Version 1.0 December 2017

CAPACITANCE-TO-DIGITAL CONVERTER

FEATURES:

- **16 BITS RESOLUTION**
- **Non Linearity: 0.7% FSR**
- **PROGRAMMABLE DATA OUTPUT RATESUP TO 4KHZ**
- **PROGRAMMABLE INPUT CAPACITANCE: 4pF TO 28 pF**
- **PROGRAMMABLE OFFSET CAPACITANCE: 4pF TO 28 pF**
- **NON-LINEARITY CORRECTION OF SENSOR (UP TO 2ND ORDER)**
- **SPI COMPATIBLE**
- **3.0V TO 3.6V**
- **180NM SCL CMOS STANDARD LOGIC PROCESS**

DESCRIPTION:

SC1602 is a high resolution, Sigma Delta based capacitance-to-digital converter (CDC). The capacitance to be measured is connected directly to the device inputs. The device also offers offset and non-linearity correction (up to second order) of the sensor via on-chip digital signal processer. The SC1602 is configurable for capacitive sensors with capacitances up to 28 pf. It can also accept up to 28pf common mode capacitance. It is designed for single ended capacitive sensors (both terminals must be available). The serial interface is SPI compatible.

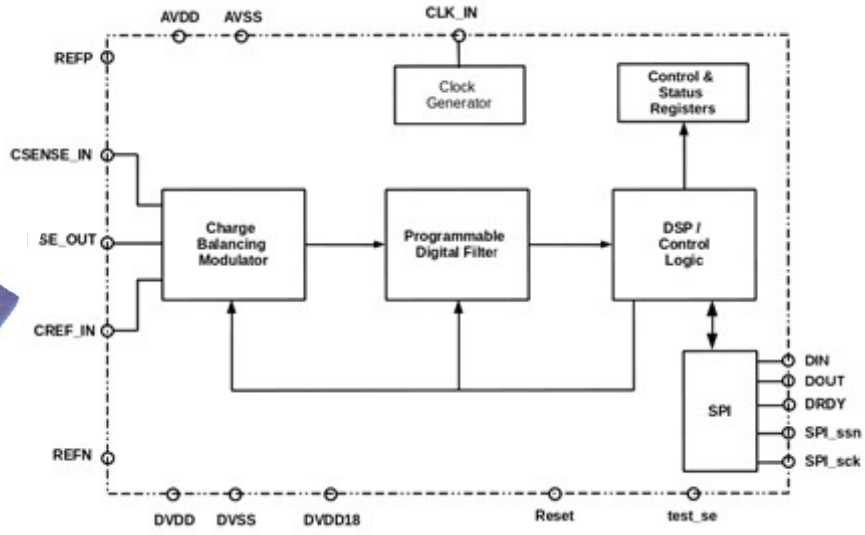

Figure 1: Block Diagram

PIN CONFIGURATION:

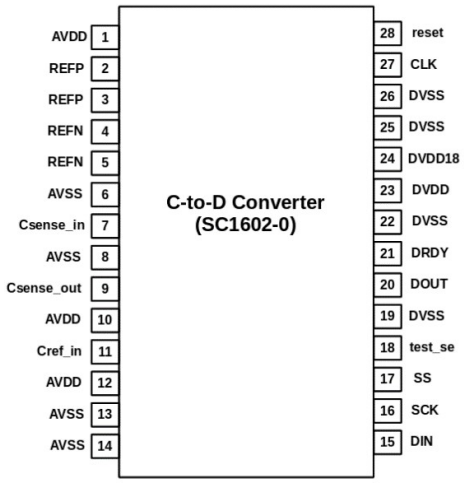

Figure 2: Pin Configuration

PIN DESCRIPTIONS:

PIN No.	Name	Description
1	AVDD	Analog Power Supply (3.3 V)
2	REFP	Positive Differential Reference Input
3	REFP	Positive Differential Reference Input
4	REFN	Negative Differential Reference Input
5	REFN	Negative Differential Reference Input
6	AVSS	Analog Core Ground
7	Csense_in	Input Terminal of Sensor Capacitance
8	AVSS	Analog ground
9	Csense_out	Output Terminal of Sensor Capacitance
10	AVDD	Analog Power Supply (3.3 V)
11	Cref_in	External Reference Capacitor
12	AVDD	Analog Power Supply (3.3 V)
13	AVSS	Analog ground
14	AVSS	Analog ground
15	DIN	Serial Data Input
16	SCLK	Serial Clock
17	SS	Serial Interface Enable (Active Low)
18	test_se	Scan Enable
19	DVSS	Digital Core Ground
20	DOUT	Serial Data Output
21	DRDY	Data Ready (Active Low)
22	DVDD	Digital I/O Power Supply (3.3 V)
23	DVDD18	Digital Core Power Supply (1.8 V)
24	DVSS	Digital Core Ground
25	DVSS	Digital Core Ground
26	CLK	Clock Input
28	reset	Enable low reset

Table 1: Pin Descriptions

TIMING SPECIFICATIONS:

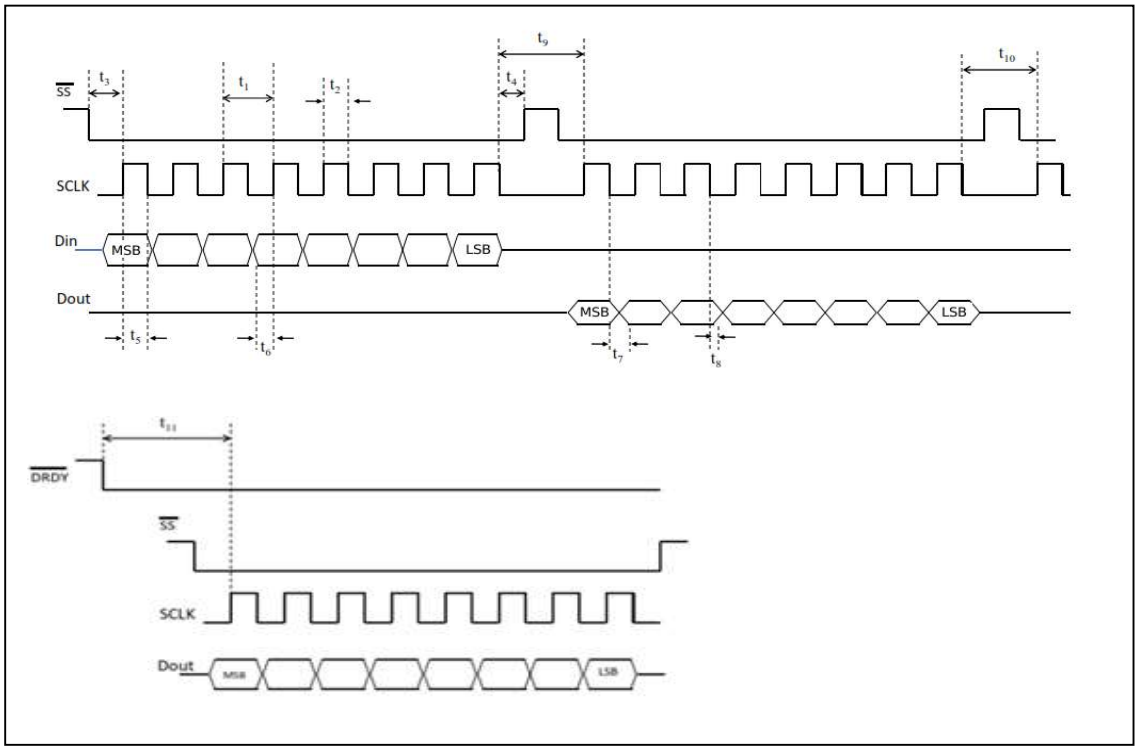

Figure3: Timing Waveform

TIMING SPECIFICATION TABLE:

SPEC	DESCRIPTION	MIN	MAX	UNIT
t_1	SCLK period	4 cycle		t_{CLK}Period
t_2	SCLK pulse width (High and Low)	2 cycle		t_{CLK}Period
t_3	SS low to first SCLK edge	100		ns
t_4	Last SCLK falling edge to SS HIGH	100		ns
t_5	SCK rising edge to DIN valid (Hold time)	50		ns
t_6	DIN valid to SCLK rising edge (Setup time)	50		ns
t_7	SCLK falling Edge to valid new DOUT		50	ns
t_8	SCLK falling Edge to DOUT, Hold Time	0		ns^2
t_9	Delay between last SCLK edge of 1st byte transfer and first SCLK edge for subsequent 2nd byte transfer : RDATA, RDATAC, RREG, WREG Command	50		t_{CLK}Period
t_{10}	Final SCLK edge of one command until first edge SCLK of next command	4		t_{CLK}Period
t_{11}	DRDY LOW to first SCLK edge of first byte transfer for RDATAC command	15		t_{CLK}Period
t_{11}	DRDY LOW to first SCLK edge of first byte transfer for RDATA command	0		t_{CLK}Period

Table 2: Timing Specification

Notes: (1) DOUT goes immediately into tri-state whenever SS is high

(2) DOUT should be sampled externally on rising edge of SCLK. DOUT will remain valid till next falling edge.

ELECTRICAL CHARACTERISTICS

All Specifications AVDD, DVDD = +1.8V, Temp. = 25^0C, OSR=2048, , f_{CLK} = 2.5MHz,f_{MOD} = 78.125KHz,f_{DATA} = 38.14Hz, unless otherwise specified.

PARAMETER	TEST CONDITIONS/ COMMENT	SC1602-0			UNITS
		MIN	TYP	MAX	
CAPACITIVE INPUT					
Input Offset Capacitance C_0	User Selectable	0		28.0	pF
Full Scale Input Range C_{FS}	User Selectable	0		28.0	pF
Resolution			16		Bits
Non-Linearity Error	Best Fit Method			±0.7	% of FSR
Offset Error	After Calibration			0.3	% of FSR
Gain Error	After Calibration			0.1	% of FSR
PSRR	At 50 Hz	80			dB
REFERENCE					
REFP- RFEN				3.3	V
CLOCK INPUT					
f_{CLK}				10	MHz
POWER SUPPLY					
Analog Supply	AVDD	3.0	3.3	3.6	V
Digital Supply	DVDD	3.0	3.3	3.6	V
Digital Supply	DVDD18	1.62	1.8	1.98	V
Analog Current	I_{AVDD}			3	mA
Digital Current (Static)	I_{DVDD}			100	µA
Digital Current (Static)	I_{DVDD18}			100	µA
TEMPERATURE RANGE					
Operating		-55		125	ºC

Table3: Electrical Specifications

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ELECTRICAL CHARACTERISTICS

All Specifications AVDD, DVDD = +1.8V, Temp. = 25^0C, OSR = 2048, f_{CLK} = 2.5 MHz, f_{MOD} = 78.125 KHz, f_{DATA} = 38.14 Hz, unless otherwise specified.

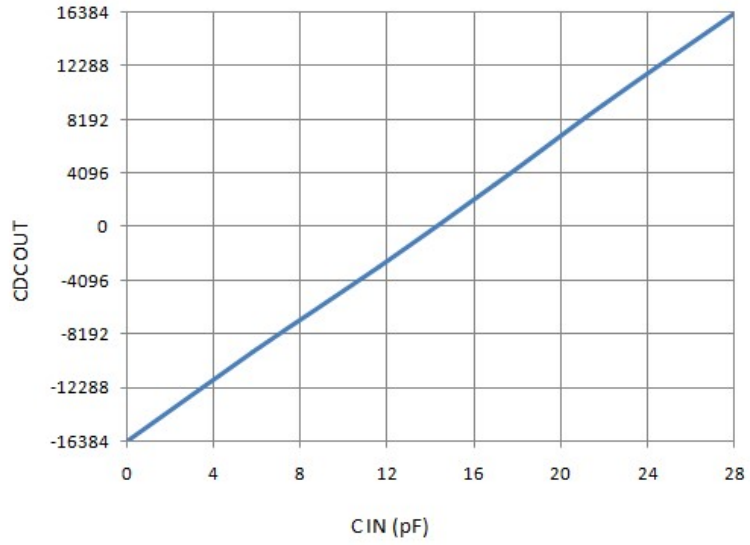


Figure 4: CDC OUT versus C_{IN}

DIGITAL CHARACTERISTICS

DVDDO= 3.0V to 3.6V

PARAMETER	TESTS CONDITIONS	SC1602-0			UNITS
		MIN	TYP	MAX	
Logic Family			CMOS		
Logic Level: V_{IH}		2		DVDD	V
V_{IL}		DVSS		0.8	V
V_{OH}	I_{OH}=8mA	3.0			V
V_{OL}	I_{OL}=8mA	DVSS		0.4	V
Input Leakage: I_{IH}	V_I=DVDD			1	µA
I_{IL}	V_I=DVSS	-1			µA

Table 4: Digital Specification

ABSOLUTE MAXIMUM RATING

PARAMETER	SC1602-0		UNITS
	MIN	MAX	
AVDD to AVSS	-0.3	4.3	V
DVDD to DVSS	-0.3	4.3	V
DVDD18 to DVSS	-0.3	2.2	V
Digital Input Voltage to DGND	-0.3	DVDD+0.3	V
Digital Output Voltage to DVSS	-0.3	DVDD+0.3	V
Digital Output Current		8	mA
Maximum Ambient Temperature		125	°C

Table 5: Absolute Ratings

OVERVIEW

CHARGE BALANCING MODULATOR

A first order charge balancing modulator is used to convert the input capacitance to one bit pulse stream. The average duty cycle of the pulse train represents the digitized signal information. The integrator used in the CDC is switched capacitor based. This integrator is also auto-zeroed.

The charge balancing modulator runs at modulator frequencyf_{MOD}. The modulator frequency can be adjusted by setting the appropriate value of PRE1: PRE0 of CR2 control register as shown in the following table:

PRE1:PRE0	f_{MOD}
00	f_{CLK} /8
01	f_{CLK} /16
10	f_{CLK} /32
11	f_{CLK} /64

Table 6: Prescaler value

Where f_{CLK} is external clock frequency.

The modulator is designed to work at a maximum sampling frequency of 500 KHz.

The CDC output is proportional to the ratio of the sensor capacitor to the internal reference capacitor (C_{REF}). The value of the internal capacitor can be adjusted using REF2:REF0 bits of CR1 control register. To optimize the measured end- resolution further, another internal capacitor (C_{OFF}) allows the subtraction of a defined offset capacitance. The value of C_{OFF} can be adjusted using COFF2:COFF0 bit of control register CR1.Follwing equations describe the output of CDC.

$Z_{SENSOR} = (C_{IN} - C_{OFF}) / C_{REF}$
$C_{OFF} = CDC_{OFF} * 1pf$
$C_{REF} = CDC_{REF} * 1pf$
Where

Z_{SENSOR}: Measured sensor ratio, must be in the range 0-1.

$C_{IN:}$ Sensor Input Capacitance
$C_{OFF:}$ Offset Capacitance
$C_{REF:}$ Reference Capacitance

CDC_{OFF}: Decimal equivalent of COFF2:COFF0 bit of control register CR1

CDC_{REF}: Decimal equivalent of REF2:REF0 bits of control register CR1

In the CDC, an option of external reference capacitor is also there. In this case:

$Z_{SENSOR} = (C_{IN} - C_{OFF}) / C_{REF\_EXT}$
Where
C_{REF_EXT}: External Reference Capacitor

CAPACITANCERANGE SELECTION:

For different input sensor, the correct range of input capacitance must be selected using CREF2:CREF0 bits and COFF2:COFF0 bit of control register CR1. The minimum and maximum value of input capacitance must fall in the specified range only. Use following table as guidance to select appropriate values for the CDC_{OFF} and CDC_{REF} for a particular capacitance input range.

C_{OFF} (pF)	C_{REF} (pF)															
	0		1		2		3		4		5		6		7	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
0	0	C_{REF_EXT}	0	4	0	8	0	12	0	16	0	20	0	24	0	28
1	4	C_{REF_EXT}	4	8	4	12	4	16	4	20	4	24	4	28	4	32
2	8	C_{REF_EXT}	8	12	8	16	8	20	8	24	8	28	8	32	8	36
3	12	C_{REF_EXT}	12	16	12	20	12	24	12	28	12	32	12	36	12	40
4	16	C_{REF_EXT}	16	20	16	24	16	28	16	32	16	36	16	40	16	44
5	20	C_{REF_EXT}	20	24	20	28	20	32	20	36	20	40	20	44	20	48
6	24	C_{REF_EXT}	24	28	24	32	24	36	24	40	24	44	24	48	24	52
7	28	C_{REF_EXT}	28	32	28	36	28	40	28	44	28	48	28	52	28	56

Table 7: Capacitance Range Selection

PROGRAMMABLE DIGITAL FILTER

The on-chip digital filter processes the 1-bit data stream from the charge balancing modulator using a sinc2 filter. The sinc filters are conceptually simple, efficient and flexible, especially where variable resolution and data rates are required. Output data rate of digital filter can be programmed by setting OSR2:OSR0 bits of CR2 control register as mentioned in Table 8.

OSR2:OSR1:OSR0	Output Data Rate
000	f_{MOD}/8192
001	f_{MOD} /4096
010	f_{MOD} /2048
011	f_{MOD} /1024
100	f_{MOD} /512
101	f_{MOD} /256
110	f_{MOD} /128

Table 8: Output Data Rate

SERIAL INTERFACE

The serial interface is standard four-wire SPI compatible (DIN, DOUT, SCK and SS_N). USER can communicate to ASC using serial interface. The SPI works in mode 00 i.e. clock phase is 0 and clock polarity is also 0. SPI serial interface signals are described below:

SS_N (Serial Interface Enable)

The SS_N input must be externally asserted before a master device can exchange data with the ADC. SS_N must be low for the duration of the transaction. DOUT pin will become tri-state when SS_N goes high. After data read operation, it should be made high.

SCK(serial clock)

SCK function as a clock for serial communication. The device will sample serial data on positive edge of SCK. Data from CDC will be launched on negative edge of SCK.

DIN (Data input)

DIN is the serial data input port. DIN is internally sampled at positive edge of SCK by SPI.

DOUT (Data Output)

DOUT is the serial data output port. DOUT is internally launched by SPI at negative edge of SCK by SPI. DOUT immediately goes into tri-state when SS_N is high.

DRDY (DATA READY)

The DRDY pin is used as a status signal to indicate when new digital code is ready to be read from the CDC. DRDY goes low when new data is available. It is reset high when a read operation from the data register is completed using RDATA or RDATAC command.

CALIBRATION

Raw data from digital filter can be corrected up to second order with on chip calibration module.

Steps for Offset/Gain calibration:

1. Disable the OCEN & GCALEN bits in CR1 register. Now the output from the module would be raw data directly given by the filter.

2. Get the CDC raw output values (y_{RAW}) at different value of input capacitance C_{in} from the module in 2's complement format. Take raw output values at minimum 5 different capacitance covering the CDC input range and make the table as below.

Input Capacitance C_{in}	Raw output y_{RAW}	Desired Output y_{CORR}
C_{in1}	y_{RAW1}	y_{CORR1}
C_{in2}	y_{RAW2}	y_{CORR2}
C_{in3}	y_{RAW3}	y_{CORR3}
C_{in4}	y_{RAW4}	y_{CORR4}
C_{in5}	y_{RAW5}	y_{CORR5}

Table 9: RAW Data

3. Perform 2nd order curve fitting between y_{RAW} and y_{CORR} and obtain the corresponding coefficients of the equation:

$$y_{CORR} = a y_{RAW}^2 + b y_{RAW} + c$$

4. The decimal coefficients need to be

converted to the required format necessary for the calibration unit. The maximum limits set in the system for a, b and c are 0.01, 3 and 16383 respectively. The formats to be given to the system are:

A_{IN} = a * 2^21 (In 2's complement)

B_{IN} = b * 2^13 (In 2's complement)

C_{IN} = c (In 2's complement)

5. For offset calibration only; Load COEFF_C register with C_{IN} value. Enable OCEN bit in CR1 Register. COEFF_A and COEFF_B register are to be set to 0.

6. For both offset and gain calibration, Load $A_{IN,}$ B_{IN} & C_{IN} values in corresponding COEFF Registers.

COMMAND DEFINITIONS

The commands listed below control the operation of SC1602-0 Device. Some commands are stand-alone commands (e.g. STOPC) while others require additional bytes (e.g., WREG requires command and the data bytes).

COMMANDS	DESCRIPTION	COMMANDBYTE	2NDCOMMANDBYTE
RDATA	Read Data	0001xxxx ($1x_H$)	-N.A.-
RDATAC	Read Data Continuously	0010xxxx($3x_H$)	-N.A.-
STOPC	Stop Read Data Continuously	0011xxxx(Fx_H)	-N.A.-
RREG	Read from Register rrrr	0100rrrr($4r_H$)	-N.A.-
WREG	Write to Register rrrr	0101rrrr($5r_H$)	nnnn_nnnn (value of reg–rrrr)

Table 10: Commands

rrrr represents the register address.
nnnnnnnn represents the data.

xxxx: these bits will be ignored while instruction decoding.

RDATA (Read Data):
This command reads a single 16-bit CDC conversion result. In response to RDATA command CDC transmit 16-bit digital code. Digital code is available at DOUT pin in 8-bit format with most significant byte first. RDATA command must be followed by 2-byte read operation. On completion of read operation, DRDY goes high.

Operands: None
Bytes: 1
Encoding: 0001 xxxx

RDATAC (Read Data Continuous)
RDATAC (Read Data Continuous) command enables the continuous output of new data on each DRDY. This command eliminates the need to send the Read Data Command on each DRDY. In case of read data continuous command user can directly perform 2 read operation to read 16-bit digital code. DRDY will go high in response to 2-byte read operation. This mode will be terminated by the STOPC (Stop Read data Continuous) command.

RDATAC command must be followed by STOPC command before issuing any other command.

Operands: None
Bytes: 1
Encoding: 0011xxxx

STOPC (Stop Read Data Continuous)
Description: Ends the continuous data output mode. After this command DRDY will also go high.
Operands: None
Bytes: 1
Encoding: 1111xxxx

RREG (Read Register)
RREG command reads content of the specified register. The address of the

register to be read is specified in the LSB nibble of the instruction.

Operands: None
Bytes: 2
Encoding: 0100rrrr

rrrr: Defines register address as mentioned in the Table 10.

WREG (Write Register)
WREG command writes the data to specified register. The address of the register to be written is specified in the LSB nibble of the instruction. Second byte represents the data to be written.

Operands: r,n
Bytes: 2
Encoding: 0101rrrrnnnnnnnn

rrrr: Defines register address as mentioned in the Table 10.
nnnnnnnn : value of reg–rrrr

CONTROL / STATUS REGISTERS

The operation of the device is set up through following control / status registers.

Address	Register	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0_H	digital_code_B0 (R)	DC7	DC6	DC5	DC4	DC3	DC2	DC1	DC0
1_H	digital_code_B (R)	DC15	DC14	DC13	DC12	DC11	DC10	DC9	DC8
2_H	CR1 (RW)	CREF2	CREF1	CREF0	OCEN	GCALEN	COFF2	COFF1	COFF0
3_H	CR2(RW)	PDM	-	-	PRE1	PRE0	OSR2	OSR1	OSR0
4_H	COEFF_A_B0 (RW)	AIN7	AIN6	AIN5	AIN4	AIN3	AIN2	AIN1	AIN0
5_H	COEFF_A_B1 (RW)	AIN15	AIN14	AIN13	AIN12	AIN11	AIN10	AIN9	AIN8
8H	COEFF_B_B0 (RW)	BIN7	BIN6	BIN5	BIN4	BIN3	BIN2	BIN1	BIN0
9_H	COEFF_B_B1 (RW)	BIN15	BIN14	BIN13	BIN12	BIN11	BIN10	BIN9	BIN8
A_H	COEFF_C_B0 (RW)	CIN7	CIN6	CIN5	CIN4	CIN3	CIN2	CIN1	CIN0
B_H	COEFF_C_B1 (RW)	CIN15	CIN14	CIN13	CIN12	CIN11	CIN10	CIN9	CIN8
E_H	STATUS (R)	DRDY	MOD_ RST	MULT_DR DY	FCLK	FDI	RST	0	0

Table 11: Control / Status Registers

R: Read only registers
RW: Read / Write registers
Note: All registers are initialized to 00_H on reset.

DIGITAL_CODE_B0 (ADD: 00_H) DIGITAL OUTPUT CODE (LEAST SIGNIFICANT BYTE)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
DC07	DC06	DC05	DC04	DC03	DC02	DC01	DC00

DIGITAL_CODE_B1 (ADD: 01_H) DIGITAL OUTPUT CODE (MOST SIGNIFICANT BYTE)

BIT7	BIT6	BIT5	BIT4		BIT3	BIT2	BIT1	BIT0
DC15	DC14	DC13	DC12		DC11	DC10	DC09	DC08

CR1 (ADD: 02_H) CONTROLREGISTER-1

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CREF2	CREF0	CREF0	OCEN	GCALEN	COFF2	COFF1	COFF0

Bit 7-5 : CREF2:CREF1:REF0: Reference control for analog selection Bits.
Refer to Table 7 for more details
Bit 4: OCEN: Offset Calibration Enable bit
OCE = 1: Enable offset calibration
OCE = 0: Disable offset calibration

Bit 3: GCALEN: Gain calibration Enable bit
GCALEN = 1: Enable Gain calibration
GCALEN = 0: Disable Gain calibration

Bit 2-0: OFF2:OFF1:OFF0: Offset control for analog section Bits.
Refer to Table 7 for more details

CR2 (ADD: 03_H) CONTROL REGISTER- 2

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
PDM	-	-	PRE1	PRE0	OSR2	OSR1	OSR0

Bit 7: PDM

Bit 4-3: PRE1:PRE0: Prescaler Bits.
Refer to Table 6 for more details.
Bit 2-0: OSR2:OSR0: OSR control bits.
Refer to Table 8 for more details.

COEFF_A_B0 (ADD: 04_H): 2^{ND} ORDER COEFFICIENT (LEAST SIGNIFICANT BYTE)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
AIN7	AIN6	AIN5	AIN4	AIN3	AIN2	AIN1	AIN0

COEFF_A_B1 (ADD: 05_H): 2^{ND} ORDER COEFFICIENT (MOST SIGNIFICANT BYTE)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
AIN15	AIN14	AIN13	AIN12	AIN11	AIN10	AIN9	AIN8

COEFF_B_B0 (ADD: 08_H): 1^{st} ORDER COEFFICIENT (LEAST SIGNIFICANT BYTE)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
BIN7	BIN6	BIN5	BIN4	BIN3	BIN2	BIN1	BIN0

COEFF_B_B1 (ADD: 09_H): 1^{st} ORDER COEFFICIENT (MOST SIGNIFICANT BYTE)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
BIN15	BIN14	BIN13	BIN12	BIN11	BIN10	BIN9	BIN8

COEFF_C_B0 (ADD: $0A_H$): OFFSET COEFFICIENT (LEAST SIGNIFICANT BYTE)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CIN7	CIN6	CIN5	CIN4	CIN3	CIN2	CIN1	CIN0

COEFF_C_B1 (ADD: $0B_H$): OFFSET COEFFICIENT (MOST SIGNIFICANT BYTE)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CIN15	CIN14	CIN13	CIN12	CIN11	CIN10	CIN9	CIN8

STATUS (ADD: $0E_H$): STATUS REGISTER

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
DRDY	MOD_RST	MULT_DRDY	FCLK	FDI	RST	0	0

Bit 7: This bit duplicate the status of DRDY pin

Bit6: This bit gives the reset signal of modulator

Bit 5: This is the data ready signal coming from the multiplier module that signifies the end of multiplication operation.

Bit 4: Clock given to the comb section of the CIC filter.

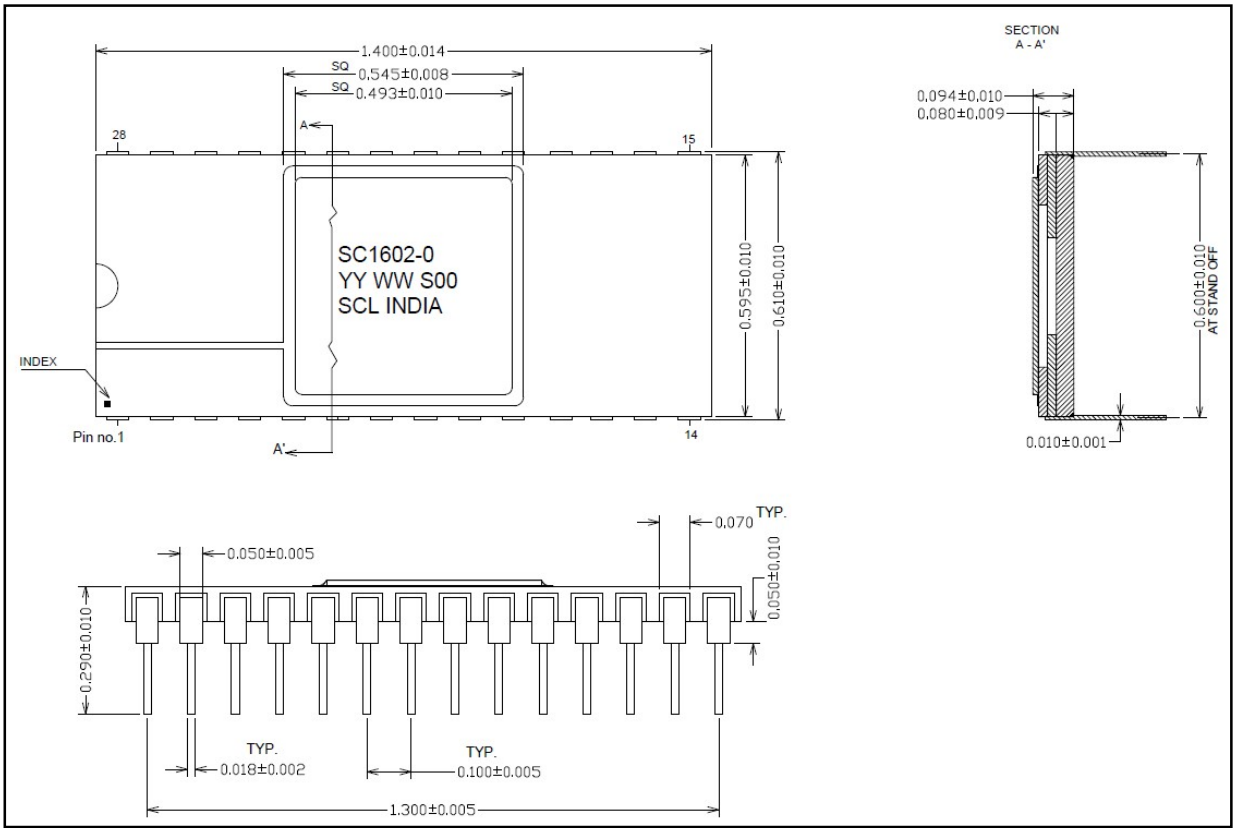
Bit 3: Single bit stream going to the CIC filter.

Bit 2: Reset signal.

PACKAGE INFORMATION

Package: 16 Pin DIP

All dimensions are in inch unless until specified.



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