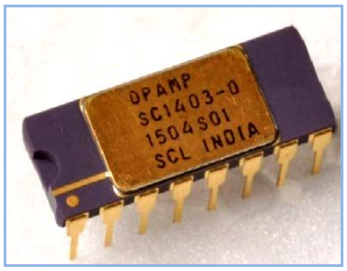
Operational Amplifier

(SC1403-0)



DATA SHEET

Version 1.0, Dec' 2015

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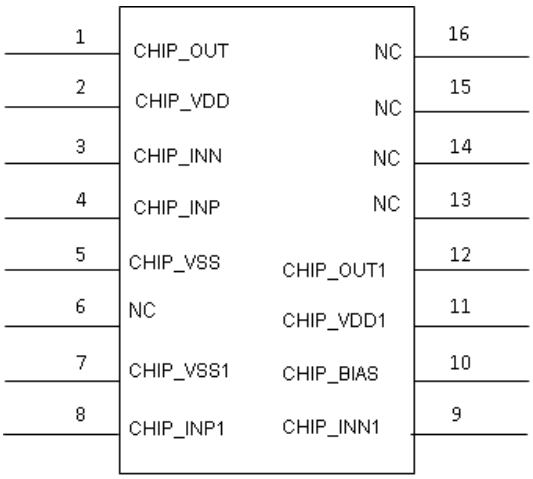
PRODUCT DESCRIPTION:

SC1403-0 is an op amp that is designed as an IP block. This chip consists of 2 nos. of internally compensated CMOS input op-amps in folded cascade architecture. First op-amp has internal bias resistor whereas second op-amp requires approx. 33kΩ external bias resistor with V_{DD}.

FEATURES:

- **Operating Supply Voltage: 3.0V± 0.3V**
- **Open loop Gain > 80db**
- **Settling Time (0.05%) < 40ns**
- **Unity Gain Bandwidth > 20MHz**
- **Power Dissipation < 15mW**
- **Load Resistance > 1KΩ**
- **Load Capacitance < 30pF**
- **Operating Temperature: -55ºC to 125ºC**
- **Ceramic 16-pin DIP packages**

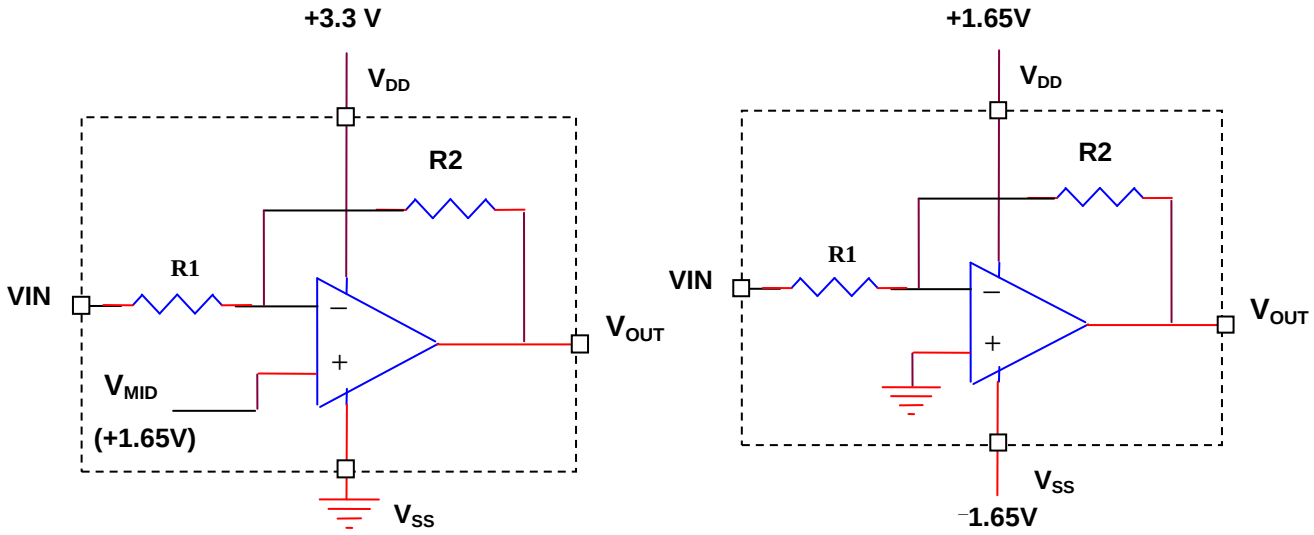
DEVICE PIN DIAGRAM:



DEVICE PIN DESCRIPTION:

DIE – 1			DIE – 2		
Pin No.	**Pin Name**	**Description**	**Pin No.**	**Pin Name**	**Description**
1	CHIP_OUT	Output	**7**	CHIP_VSS	Supply Ground
2	CHIP_VDD	Supply Power	**8**	CHIP_INP	Non-inverting Input
3	CHIP_INN	Inverting Input	**9**	CHIP_INN	Inverting Input
4	CHIP_INP	Non-inverting Input	**10**	CHIP_BIAS	Bias Resister (33K)
5	CHIP_VSS	Supply Ground	**11**	CHIP_VDD	Supply Power
6,13,14,15,16	NC	Not connected	**12**	CHIP_OUT	Output

OP AMP IN SINGLE SUPPLY AND DUAL SUPPLY CONFIGURATION:



RECOMMENDED OPERATING CONDITIONS:

SYMBOL	PARAMETER	Min	Max	Unit
V_{DD}	Supply Voltage	3.0	3.6	V
V_{IN}	Input Voltage Range	0	V_{DD}	V
I_{OH}	High level output current (Source)	-	-0.8	mA
I_{OL}	Low level output current (Sink)	-	12	mA
T_{AMB}	Operating Ambient Temperature	-55	125	ºC

ABSOLUTE MAXIMUM RATINGS (1):

Over operating free-air temperature range (unless otherwise noted),

Symbol	Parameter	Unit
V_{DD}	Supply Voltage Range	–0.5V to 4.3V
V_{IN}	Input Voltage Range	–0.5V to V_{DD}+0.5V
T_J	Max. Junction Temperature	150°C
T_{stg}	Storage Temperature Range	–65°C to 150°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DC ELECTRICAL SPECIFICATIONS:

@V_{dd} = ± 1.65V, V_{CM}=0V, T_A = 25°C

Specifications	Symbol	Test Inputs	Test Conditions	Test Results (Typ.)	Unit
INPUT CHARACTERISTICS					
Input Offset Voltage	V_{OS}	Test Method 4001.1 (Table - 5)	R2/R1 = 30K/100 R3 = 10K Test Circuit-1	-6.70	mV
Input Offset Current	I_{OS}			0.664	µA
Input Bias Current	I_{IB}			0.355	µA
Input Voltage Range (ICMR)	V_{IH}	VIN+ (RAMP) = 3.6Vpp (f = 100Khz)	G = +1 Test Circuit-2	0.935	V
	V_{IL}			-1.586	V
Common Mode Rejection Ratio	CMRR	Test Method 4003.1	R2/R1 = 30K/100 Test Circuit-1	34.41	dB
Large Signal Voltage Gain	A_{OL}	Test Method 4004.1		83.52	dB
Offset Voltage Drift	$\Delta V_{OS} / \Delta T$	Test Method 4001.1	-40°C to 125°C	4.0	µV/°C
OUTPUT CHARACTERISTICS					
Output Voltage High	VOH	Vdd = ±1.65V VIN+ (DC) = 2.0V	IL = 1mA, ACL = 1	0.982	V
			IL = 10mA, ACL = 1	0.958	V
Output Voltage Low	VOL		IL = 1mA, ACL = 1	-1.647	V
			IL = 10mA, ACL = 1	-1.338	V
Output Short Circuit Current	I_{OUT+} (source)	Vdd = ±1.65V V_{IN+} = 1.65V	G = +1 o/p short with GND Test Circuit-2	31.36	mA
	I_{OUT-} (sink)	Vdd = ±1.65V V_{IN+} = -1.65V		30.65	mA
Output Impedance	Z_{0UT}	f = 50Mhz	Test circuit 4	470	Ohm
Output Resistance	R_{0UT}	V_{IQ} = V_{OUT} = 100mV R1 = 100Ω, R2 = 467Ω C2 = 0, V2 = 1V	Test circuit 4	0.05	Ohm
POWER SUPPLY					
Supply Current	Idd	Vdd = ±1.65V V_{OUT} = 0V	G = +1 Test Circuit-2 (No Load)	± 4.2	mA
Power Dissipation	Pd			14.0	mW
PSRR	PSRR+	Vdd+ =1.65 ± 0.165V Vdd- = -1.65V	Test Circuit-1	-53.14	dB
	PSRR-	Vdd+ = 1.65V Vdd- = -1.65 ± 0.165V		-53.89	

AC ELECTRICAL SPECIFICATIONS:

@V_{dd} = ± 1.65V, V_{CM}=0V, T_A = 25°C

Specifications	Symbol	Test Inputs	Test Conditions	Test Results (Typ.)	Unit
DYNAMIC CHARACTERISTICS					
Slew Rate (Rise)	SR+	Vdd+ = 1.65V Vdd- = -1.65V VIN+ (SQUARE) = 3Vpp (f = 1Mhz)	G = +1 RL = 10K Test Circuit-2	70	V/us
Slew Rate (Fall)	SR-			74	V/us
Full Power Bandwidth	FPBW			11	MHz
Gain Bandwidth Product	GBP	VOUT(SINE) = 400mVpp (freq sweep)	G = +1 Test Circuit-2	50	MHz
Unity Gain Bandwidth	UGB	VIN+(SINE) = 100mVpp (freq sweep)	R2/R1 = 9K/1K VIN = VOUT Test Circuit-3	32	MHz
Settling Time to 0.05% (Rise)	TSS	VOUT = 1V STEP	G = +1, RL = 1K , CL = 30pF	65	nsec
Phase Margin	ϕM	Vdd = ±1.65V VOUT(SINE) = 1Vpp	G = +1	80	Degree
NOISE PERFORMANCE					
Total Harmonic Distortion + Noise	THD + N	VOUT = 1V STEP F = 1 Mhz	G = +1	0.006	%
				-84.44	dB

Table 3

TYPICAL CHARACTERISTICS:

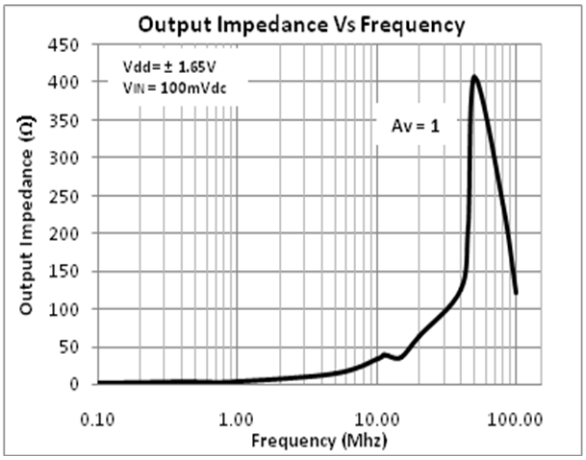


Figure 4

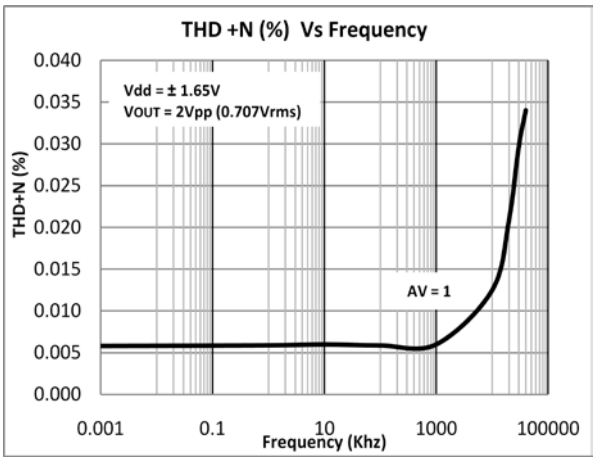


Figure 5

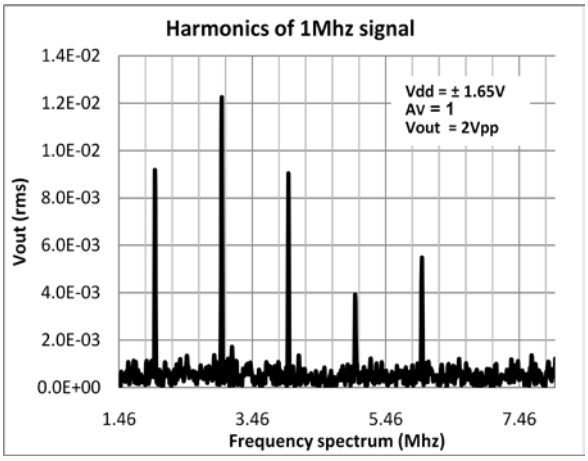


Figure 6

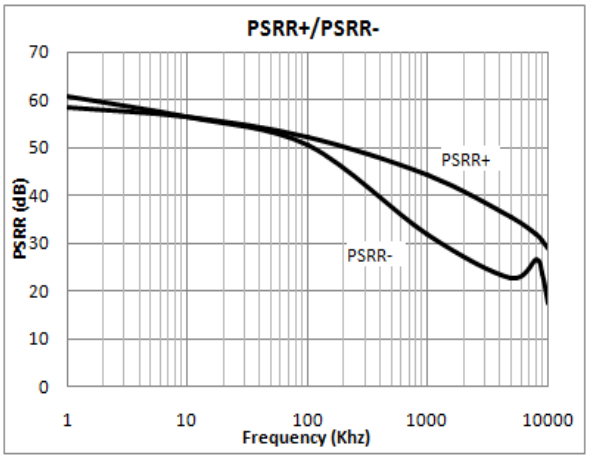


Figure 7

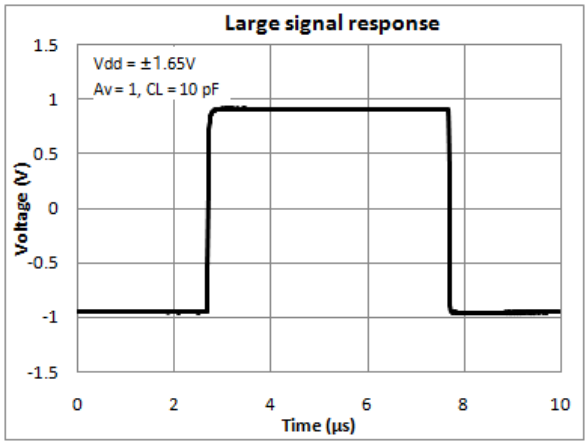


Figure 8

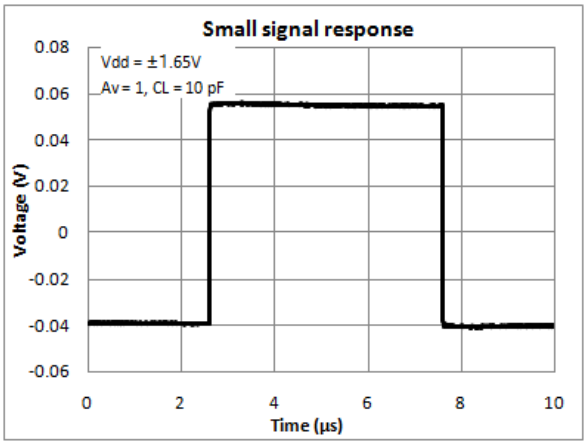


Figure 9

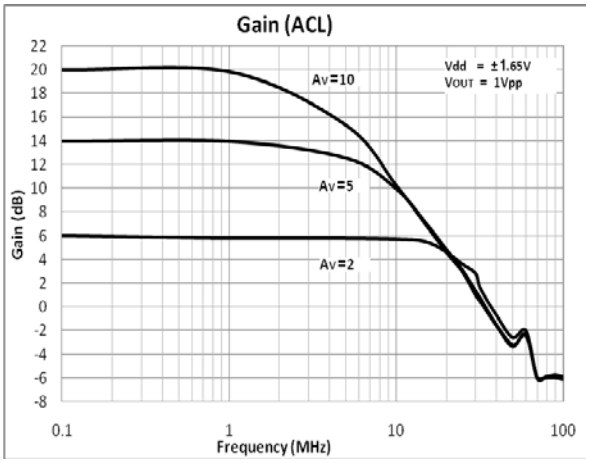


Figure 10

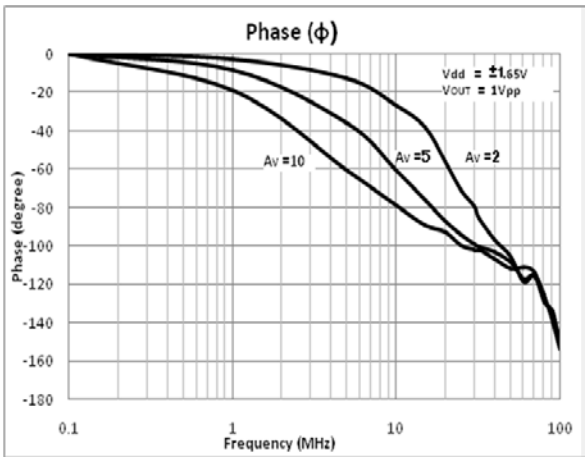


Figure 11

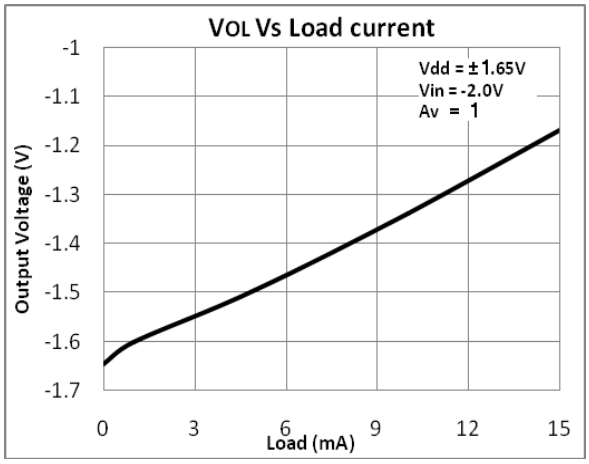


Figure 12

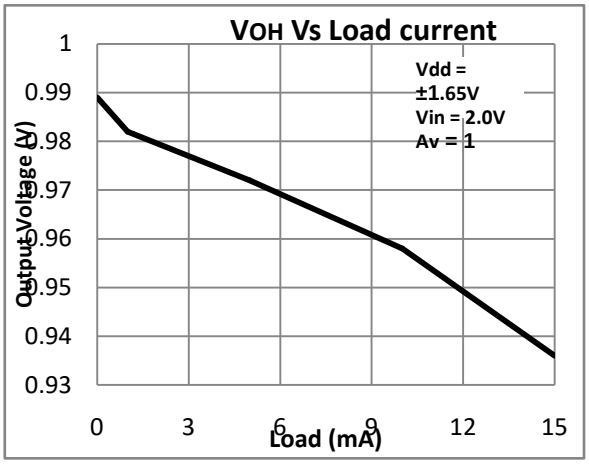


Figure 13

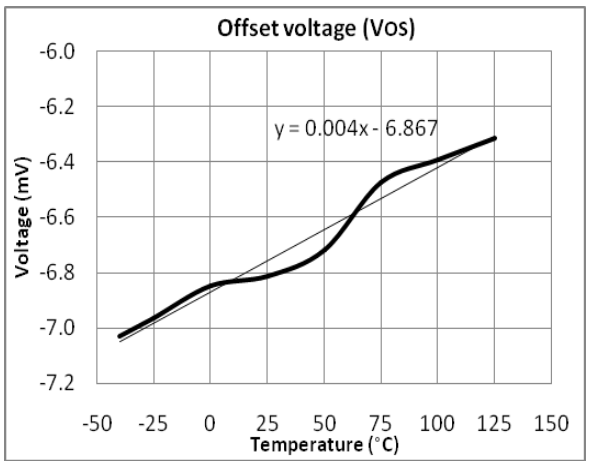


Figure 12

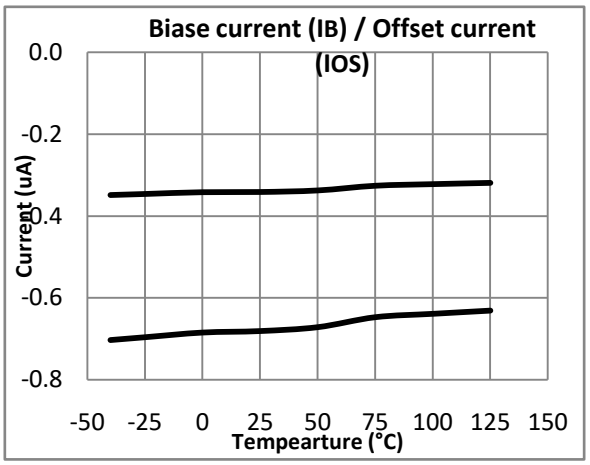


Figure 13

TEST METHOD:

S.N.	Test	Test method (MIL-STD-883E)	Test circuit
1	Input offset voltage (V_{IO})	Method 4001.1	Test circuit 1
2	Input offset current (I_{IO})	Method 4001.1	Test circuit 1
3	Input bias current (I_{IB})	Method 4001.1	Test circuit 1
4	CMMR	Method 4003.1	Test circuit 1
5	+PSRR/ -PSRR	Method 4003.1	Test circuit 1
6	Open Loop Gain	Method 4004.1	Test circuit 1
7	Slew Rate (S.R.)	Method 4002.1	Test circuit 2
8	Phase Margin	Method 4002.1	Test circuit 2
9	FPBW	Method 4002.1	Test circuit 2
10	UGB	Method 4004.1	Test circuit 3
12	Output Impedance	Method 4005.1	Test circuit 4
13	Power Dissipation	Method 4005.1	Test circuit 4
14	ICMR	----	Test circuit 2
15	VOH/VOL	----	Test circuit 2
16	$+I_{SC}$ / $-I_{SC}$	----	Test circuit 2

Table 5

TEST CIRCUITS:

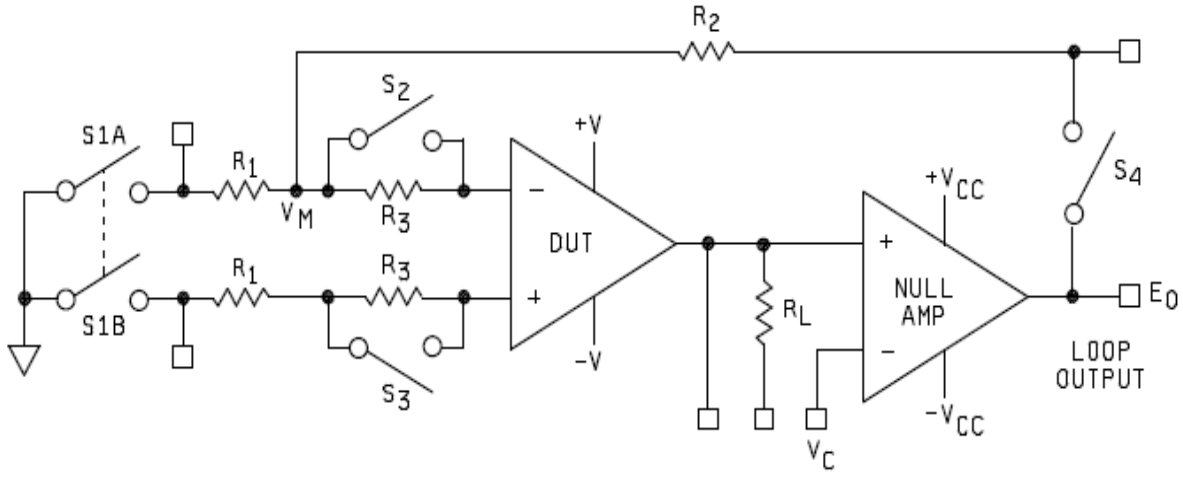


Figure 14: Test Circuit 1

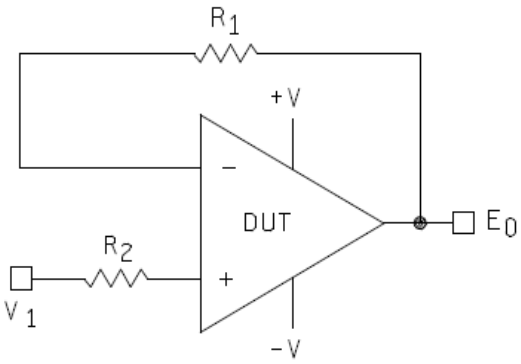


Figure 15: Test Circuit 2

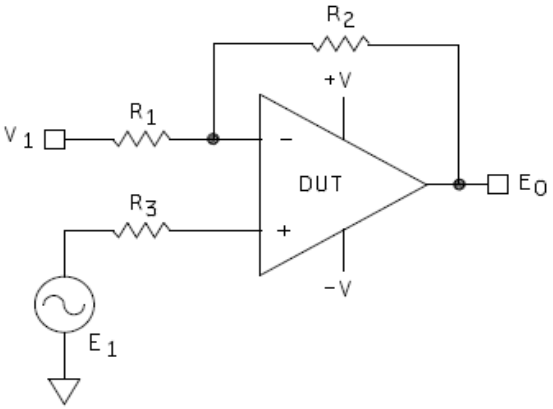


Figure 16: Test Circuit 3

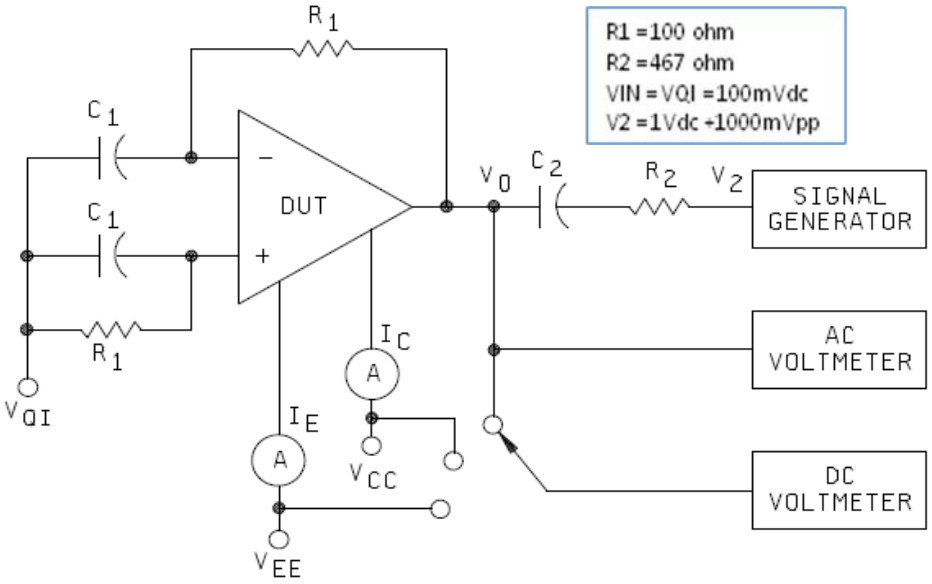
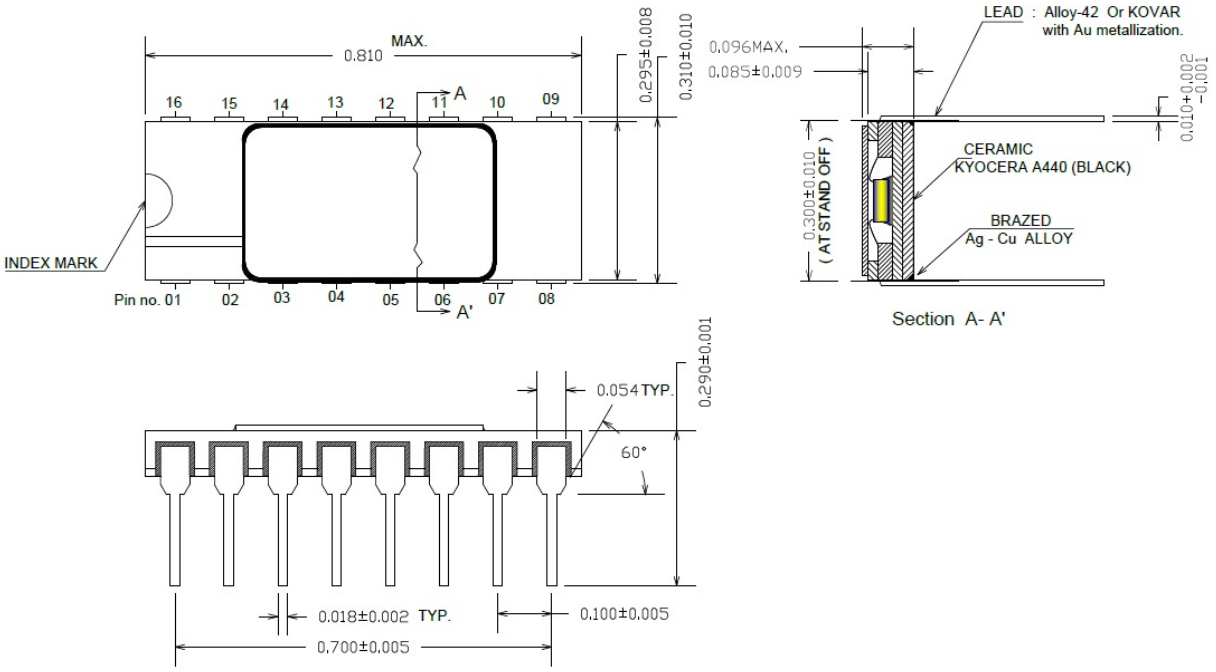


Figure 17: Test Circuit 4

MECHANICAL PACKAGE DRAWING:

16 PIN DIP PACKAGE



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