256Kbit CMOS (32K X 8) Static SRAM

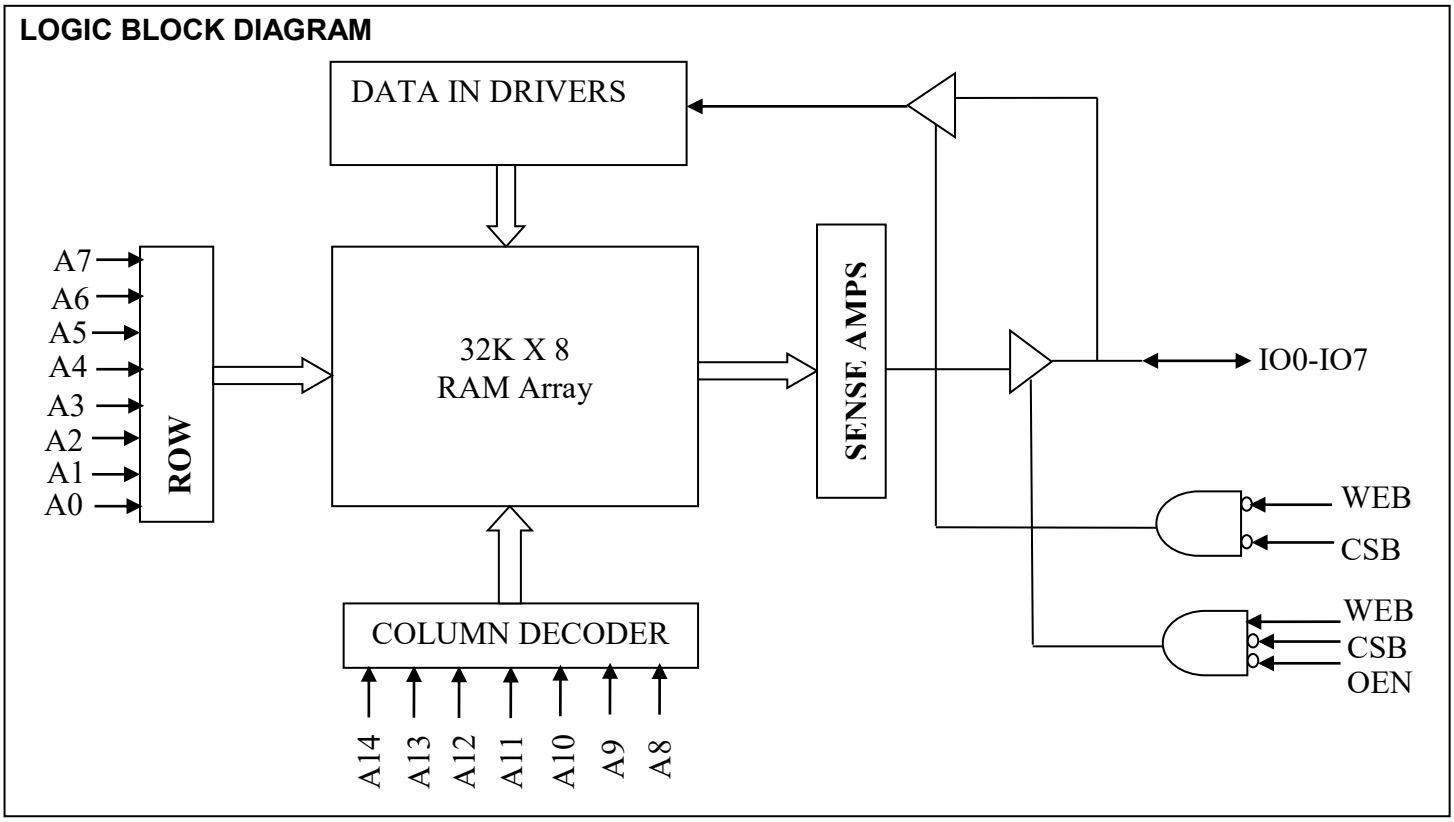
Features

- SCL's 180nm CMOS process
- I/O Power Supply 3.3V ± 10%
- Core Power Supply 1.8V ± 10%
- Operating Temperature -55ºC to 125ºC
- Asynchronous 32Kx8 bits SRAM
- Fully Static operation
- High speed operation
- Access Time t_{AA} = 18 ns
- 68 pin CQFP-J Package

Functional Description

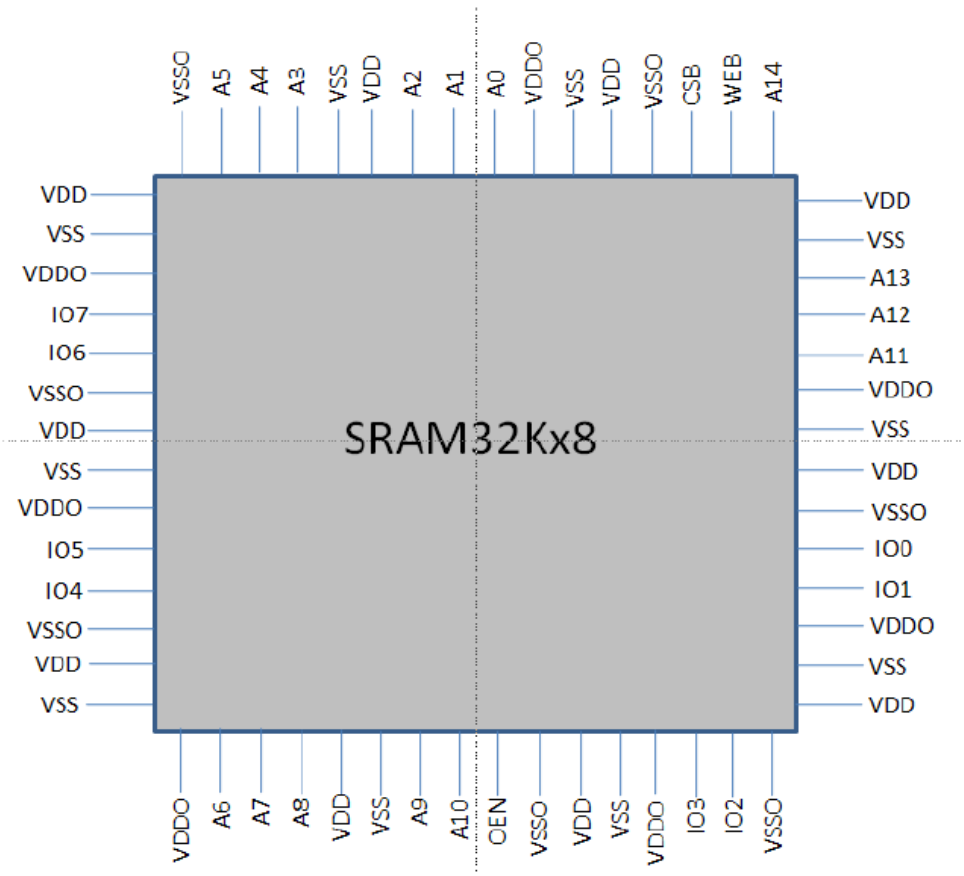
The SCL SC1301-1 is a high performance CMOS static RAM organized as 32,768 words by 8 bits. Writing to the device is accomplished by taking Chip Select (CSB) and Write Enable (WEB) inputs LOW. Reading from the device is accomplished by taking Chip Select (CSB) and Output Enable (OEN) LOW while forcing the Write Enable (WEB) HIGH. The complete description of Read and Write modes can be found in the truth table. The input/output pins (IO0 through IO7) are placed in a high-impedance state when the device is deselected (CSB HIGH), or OEN and WEB both are held HIGH with CSB Low.

LOGIC BLOCK DIAGRAM



Pin Configurations

Name	Pin Number	I/O Type	Description
A0-A14	68,1,2,5,6,7,28,29,30, 33,34,55,56,57,61	Input	Address inputs (A14 as MSB)
IO0-IO7	49,48,41,40,22,21,15, 14	Input / Output	Data Input / Output (IO7 as MSB)
CSB	63	Input	Chip Select (Active low)
WEB	62	Input	Write Enable (Active low)
OEN	35	Input	Output Enable (Active low)
VDDO	13,20,27,39,47,54,67	Power Supply	I/O supply (3.3 V)
VDD	3,11,17,24,31,37,45, 51,59,65	Power Supply	Core Supply (1.8 V)
VSSO	8,16,23,36,42,50,64	Ground	I/O Ground
VSS	4,12,19,25,32,38,46, 53,58,66	Ground	Core Ground



Absolute Maximum Ratings

Symbol	Rating	Value
V_{DDO}	IO supply Voltage relative to V_{SSO}	4.3 V
V_{DD}	Core supply Voltage relative to V_{SS}	2.2 V
T_J	Operating Temperature (Junction)	125 ºC

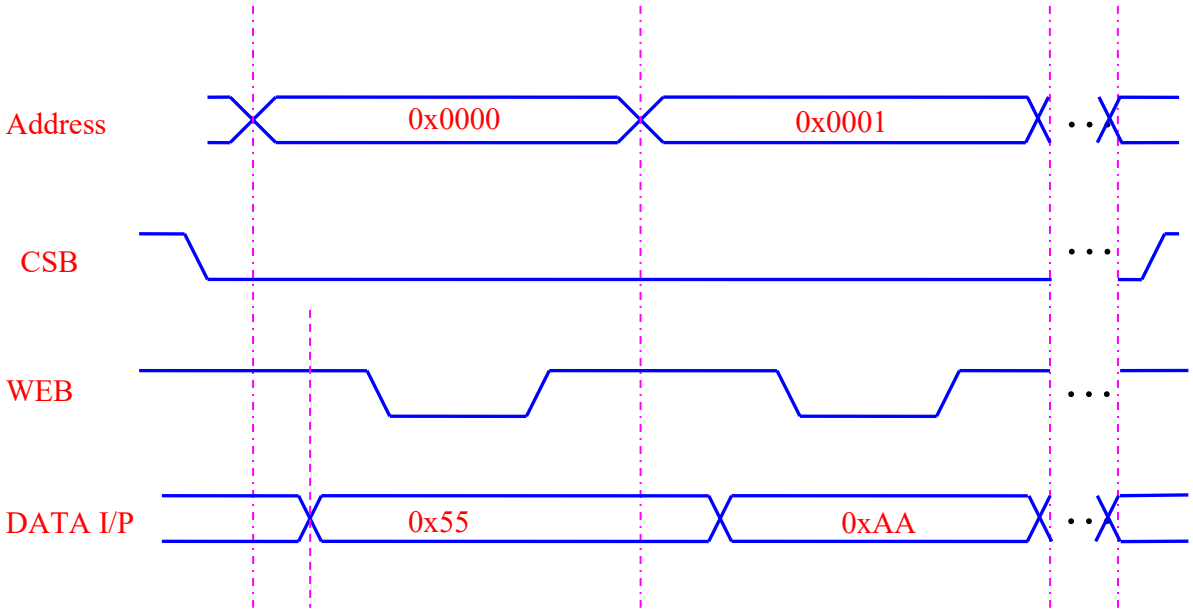
Truth Table

WEB	CSB	OEN	IO	Function
X	H	X	High-Z	Disabled
H	L	H	High-Z	Output Disable
H	L	L	Dout	Read
L	L	X	Din	Write

DC Electrical Characteristics over the Operating Range

Parameter	Conditions	Symbol	Typical Value	Unit
Dynamic Operating Current	CSB<VIL V_{DD}=max, f=f_{MAX}	I_{DD}	134	mA
		I_{DDO}	23	mA
Standby Power Supply Current	CSB=V_{IH} V_{DD}=max, f=f_{MAX}	I_{DDSB}	1.8	mA
		I_{DDOSB}	8	mA
Full Standby Power Supply Current	CSB=V_{IH} V_{DD}=max, f=0	I_{DDSB1}	1	μA
		I_{DDOSB1}	28	μA
Input Leakage Current	V_{DD}=max, V_{IN}=GND or V_{DD}	I_{IL}/I_{IH}	100	nA
Output Low Voltage	V_{DDO}=min; I_{OL} = - 8mA	V_{OL}	115.15	mV
Output High Voltage	V_{DDO}=min; I_{OH} = + 8mA	V_{OH}	3.12	mV

Switching Waveforms



OEN: As per truth table: OEN = X

Fig. 2 WEB dependent Write Cycle

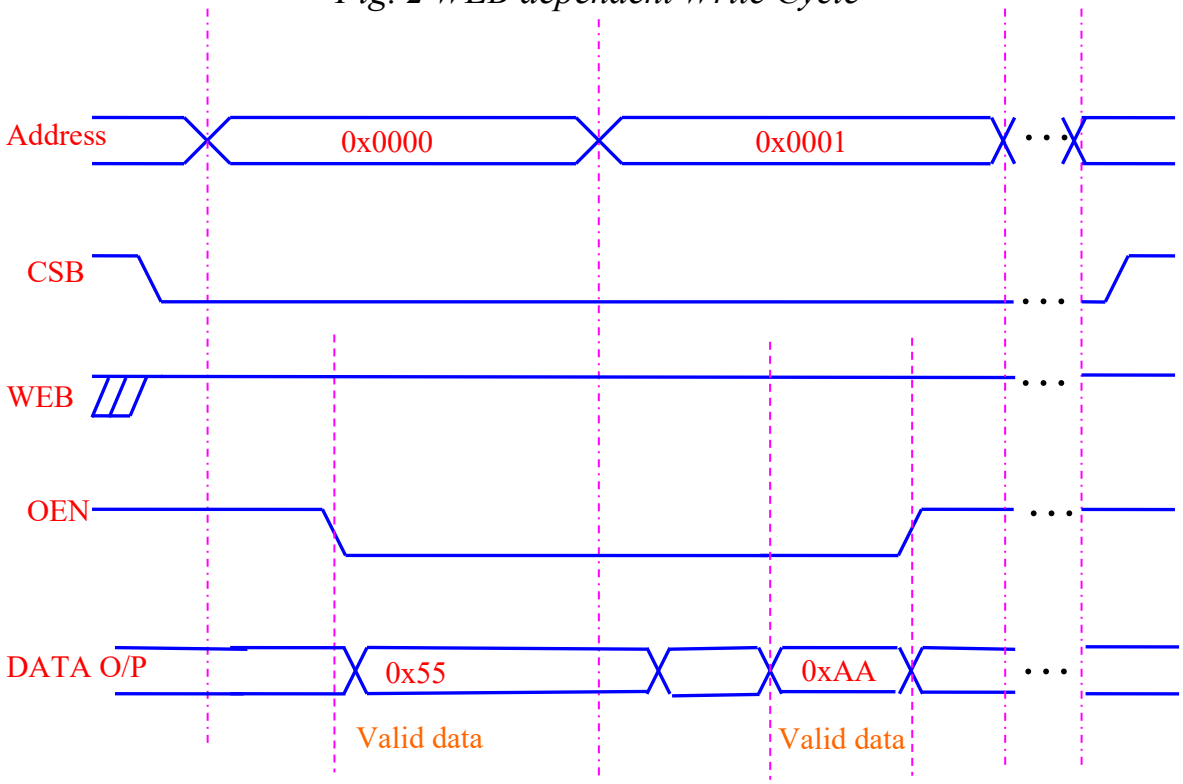
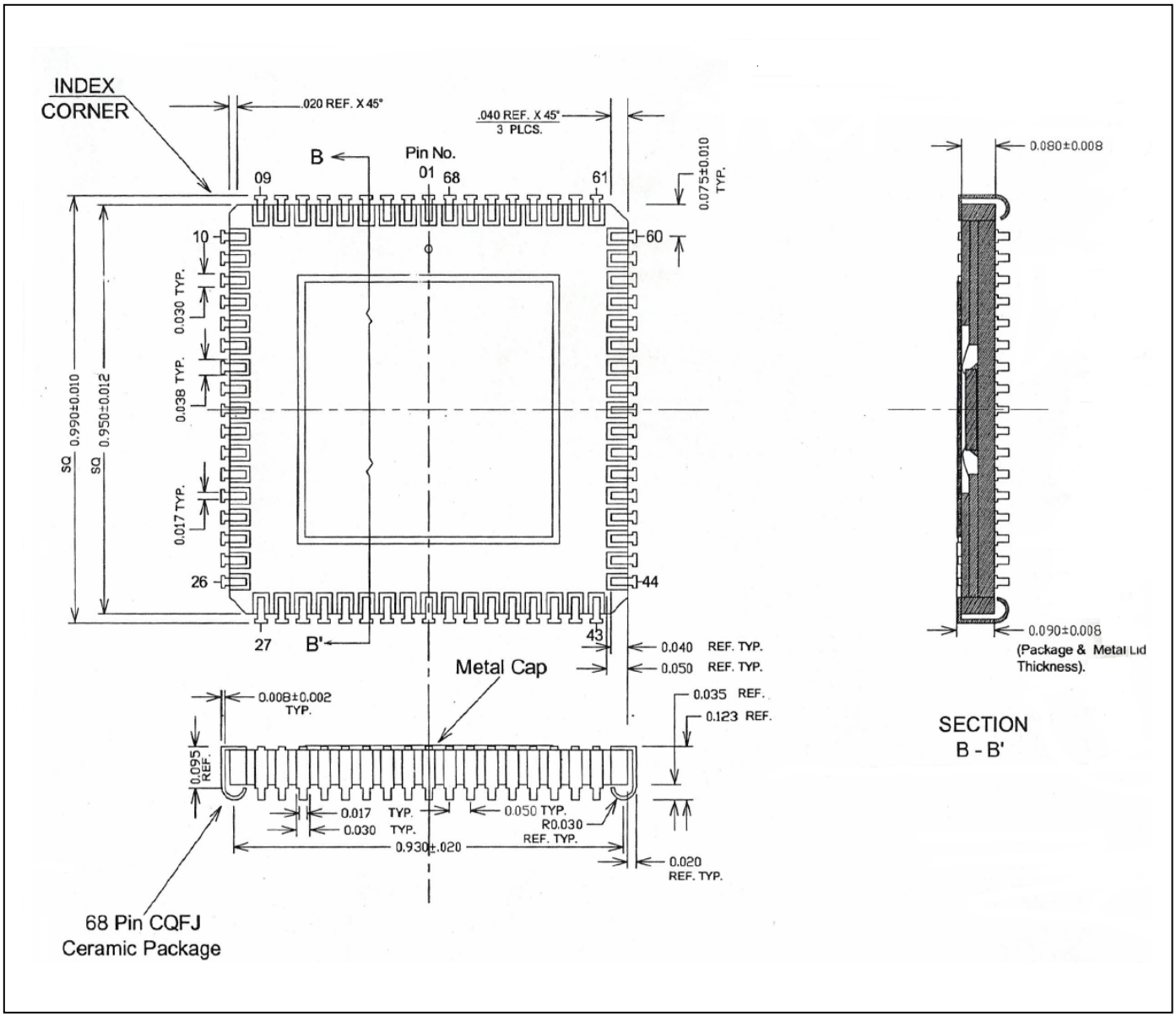


Fig. 3 OEN dependent Read Cycle

Package Details:

68 pin CQFP-J is being used to package the device. Package drawing is attached below.



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