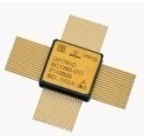

DATA SHEET

10-BIT,1.5MSPS, SUCCESSIVE-APPROXIMATION-REGSITER(SAR)
ANALOG TO DIGITAL CONVERTER
Differential

SC1260-0T1

Version 1.0, October 2022

Semi–Conductor Laboratory
Government of India
S.A.S. Nagar, Punjab-160071
www.scl.gov.in

PRODUCT DESCRIPTION:

The 10-bit SAR is a monolithic CMOS analog-to-digital converter capable of converting analog input signals into 10-bit digital word up to 1.5 Mega samples per second (MSPS) in serial and parallel mode. This converter uses a SAR architecture, operating on a single 3.3V power supply, device achieves 10-bits effective resolution and consumes <5mW power. The inputs provide a full scale input swing equal 0.65V to 2.65V. Full scale input range is recommended for optimum performance. The ASIC is fabricated in 180nm SCL CMOS Standard Logic Process.

FEATURES

- Operating Voltage: 3.3V
- Resolution: 10-Bit
- Data Rate: 1.5MSPS
- Input Range: 4Vp-p Differential Ended
- No missing code Guaranteed
- Output Data Format: Straight Binary (Serial and Parallel)
- Power Consumption < 5mW
- SCL's 180nm CMOS Technology
- Operating Temperature (TA): -55ºC to +125ºC
- Packaged in 64 Pins CQFP

APPLICATIONS:

- **Medical Imaging**
- **Industrial Process Control**

BLOCK DIAGRAM:

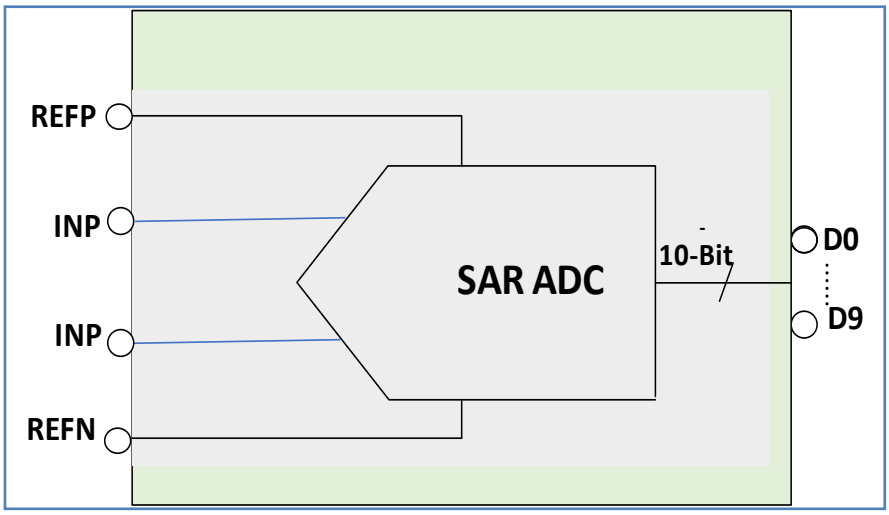

Figure-1: Device Block Diagram

DEVICE SUMMARY:

Table-1: Package Detail

Reference	Package	Pins	Lead Finish	Description	Junction Temp. range
SC1260-0T1	**CQFP**	**64**	**Gold**	Engineering Model	-55°C to +125°C

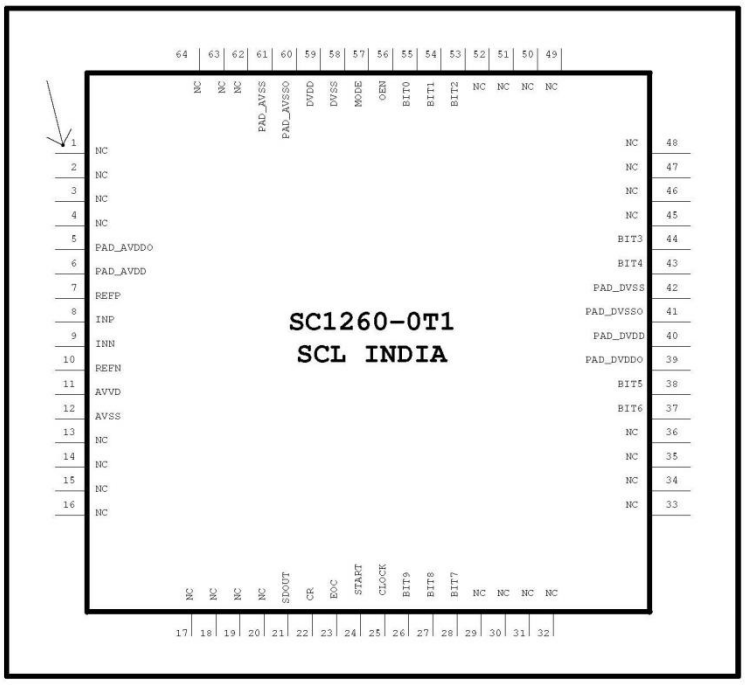

Figure-2: Pin Diagram

Table-2: Pin Configuration

Pin No.	Pin Name	Pin Type	Pin Description
12,60,61	AVSS	AP	Analog Negative Supply (0V)
41,42,58	DVSS	DP	Digital Negative Supply (0V)
5,6,11	AVDD	AP	Analog Positive Supply (+3.3V)
39,40,59	DVDD	DP	Digital positive Supply (3.3V)
7	REFP	AI	Positive reference voltage
10	REFN	AI	Negative reference voltage
21	SDOUT	DO	Serial Data Out
22	$\overline{CR}$	DI	Clear for internal registers (Active Low)
23	EOC	DO	ADC end of conversion
24	START		ADC Start pulse
25	CLOCK	DI	ADC Sampling Clock
56	$\overline{OEN}$	DI	Output enable (Active Low)
57	MODE	DI	One Shot or Continuous Conversion Mode Continuous Conversion: Mode=Logic1 One Shot Conversion: Mode=Logic0
8	INP	AI	ADC IN+
9	INN	AI	ADC IN-
26	BIT9	DO	ADC digital output Bit (MSB)
27	BIT8	DO	ADC digital output Bit
28	BIT7	DO	ADC digital output Bit
37	BIT6	DO	ADC digital output Bit
38	BIT5	DO	ADC digital output Bit
43	BIT4	DO	ADC digital output Bit
44	BIT3	DO	ADC digital output Bit
53	BIT2	DO	ADC digital output Bit
54	BIT1	DO	ADC digital output Bit
55	BIT0	DO	ADC digital output Bit (LSB)
1,2,3,4,13-20,29-36,45-52, 62-64	NC		Internally Not Connected

- # PIN TYPE: AI = Analog Input, AO = Analog Output, DI = Digital Input, DO = Digital Output, AP = Analog Power, DP = Digital Power.

ELECTRICAL SPECIFICATIONS:

All typical specifications are at T_A = 25°C, all power supply voltages = 3.3V and Conversion rate=1.5MSPS unless otherwise stated. All maximum specifications are assured across operating temperature and voltage ranges.

Table-3: Electrical Specifications

Parameters	Test Conditions	Min.	Typ.	Max.	Units
POWER SUPPLY					
AVDD Analog supply voltage		2.97	3.3	3.63	V
DVDD Digital supply voltage		2.97	3.3	3.63	V
AVDD Operating current		0.127	0.14	0.15	mA
DVDD Operating current		0.45	0.48	0.53	mA
Power Dissipation		1.97	2.08	2.23	mW
EXTERNALREFERENCE					
Positive reference voltage	REFP		2.65		V
Negative reference voltage	REFN		0.65		V
CURRENT REQUIREMENT					
Positive reference voltage	REFP		0.027		mA
Negative reference voltage	REFN		0.040		mA
JUNCTION TEMPERATURE		-55	25	125	°C
DIGITAL INPUT					
VIH : Logic-high input voltage		2.0		DVDD	V
VIL : Logic-low input voltage		0		0.8	V
IIH : Logic-high input current		-10	0.9	10	µA
IIL : Logic-low input current		-10	1	10	µA
Input capacitance			5		pF
DIGITAL OUTPUT					
VOH : Logic-high output voltage	@5mA I_{OH}	3.24	3.28	3.3	V
VOL : Logic-low output voltage	@5mA I_{OL}	0	.06	0.4	V
Output load capacitance	@1MHz		10		pF

ELECTRICAL SPECIFICATIONS (CONTINUED):

Parameters	Test Conditions	Min.	Typ.	Max.	Units
Resolution			10	10	Bits
Conversion rate				1.5	MSPS
Input Range				4	Vpp
No missing codes			Guaranteed		
Differential nonlinearity		-0.62		1.03	LSB
Integral nonlinearity		-0.44		1.17	LSB
Gain Error		2.41		2.53	% of FSR
Offset Error		-13.14		-11.39	LSB
Input referred noise			1		LSB
Effective resolution			10		Bit
AC LINEARITY					
Signal To Noise Ratio (SNR)	Clock =1MHz Test Frequency = 1004.733Hz	60.43		61.20	dB
Total Harmonics Distortion (THD)		-74.38		-71.48	dB
Spurious-Free Dynamic Range (SFDR)		73.68		76.32	dB
Signal To Noise And Distortion (SINAD)		60.06		60.85	dB
ENOB		9.74		9.87	Bit
Analog Input capacitance (IN+,IN-)			10		pF

Table-4: Typical Operating Conditions

Parameter	Value
AVDD	3.3V
DVDD	3.3V
REPF	2.65V
REFN	0.65V
Conversion rate	1.5MSPS
AVSS	0V
DVSS	0V

Table-5: Absolute Maximum Ratings*

Parameters	With respect To	Min.	Max.	Units
VIN	AVSS	-0.3	AVDD	V
DIGITAL INPUTS	AVSS	-0.3	AVDD	V
AVDD	AVSS	-0.3	3.9	V
DVDD	DVSS	-0.3	3.9	V
AVSS	DVSS	-0.3	0.3	V
DIGITAL OUTPUTS	DVSS	-0.3	DVDD	V
Storage Temperature		-65	150	ºC
Lead Temperature (10 Sec)			300	ºC
ESD Tolerance (HBM)**			> 1000	V
Latch Up Protection**			100	mA

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

**These are target value. Characterization for this is in progress.

SWITCHING SPECIFICATIONS

All typical specifications are at T_A = 25°C, all power supply voltages = 3.3 V, and conversion rate = 1.5MSPS, unless otherwise stated.

Table-6: **Typical timings for best performance with 1.5MSPS Data Rate**

Symbol	Parameter	Min	Typ	Max	Units
t_C	Conversion Rate		1.5		MSPS
t_{CLK}	CLOCK Period		666.66		ns
t_{on}	CLOCK Pulse Width High		333.33		ns
t_{off}	CLOCK Pulse Width Low		333.33		ns

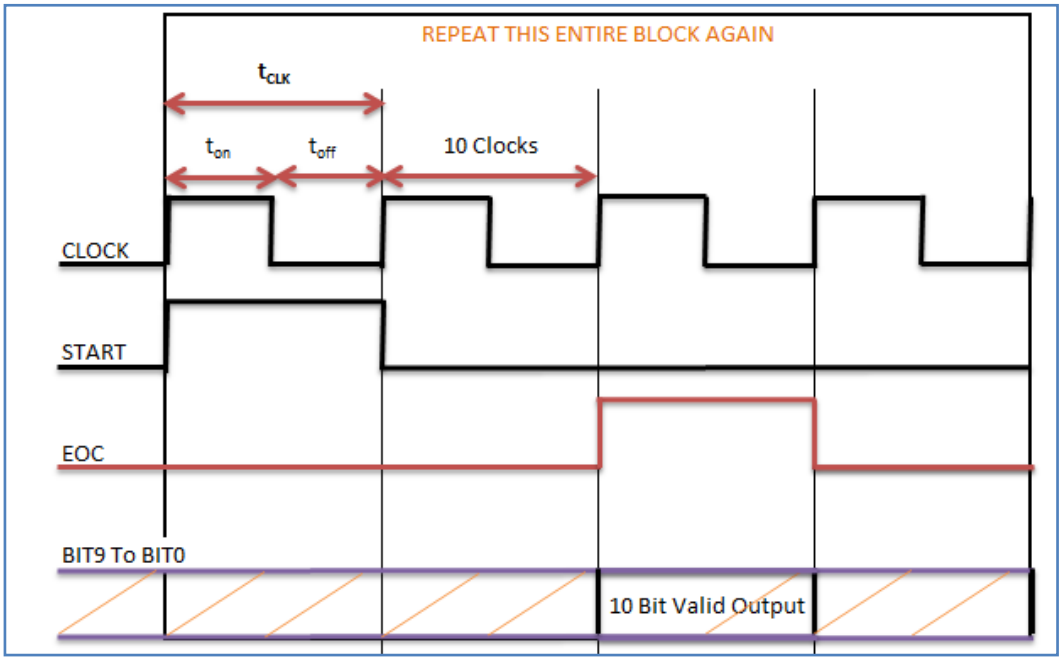

Figure-3: One Shot Mode Timing Diagram

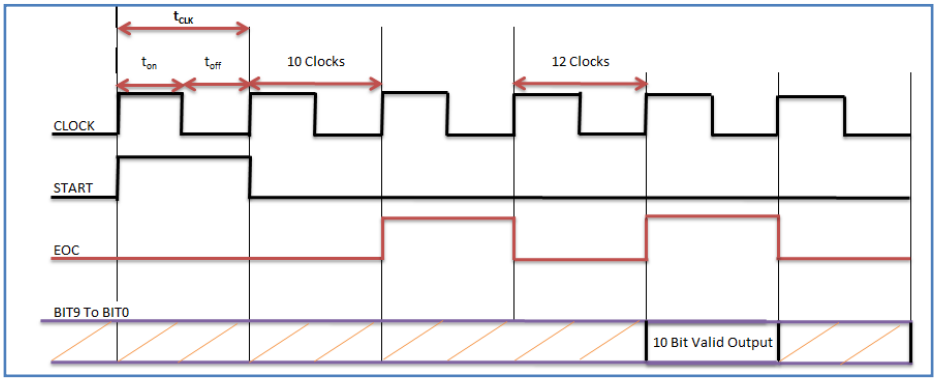

Figure-4: Continuous Conversion Mode Timing Diagram

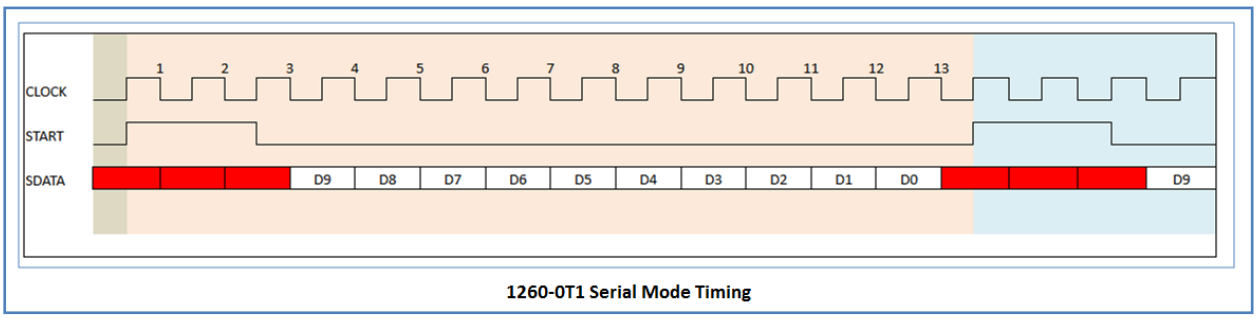

Figure-5: Serial Capture Mode Timing Diagram

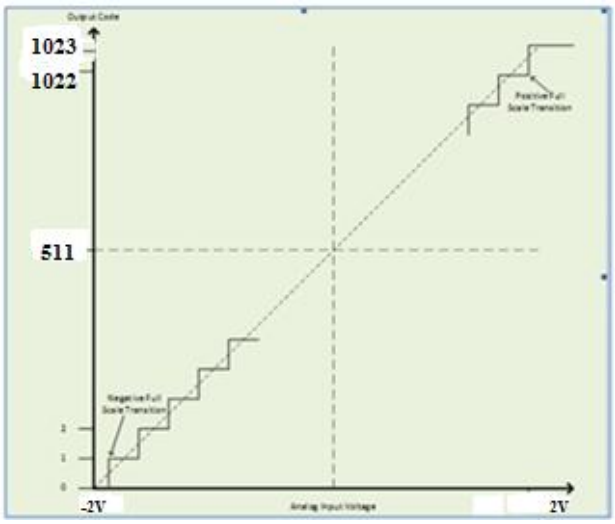

Figure-6: Transfer Characteristics of ADC

TYPICAL CHARACTERISTICS:

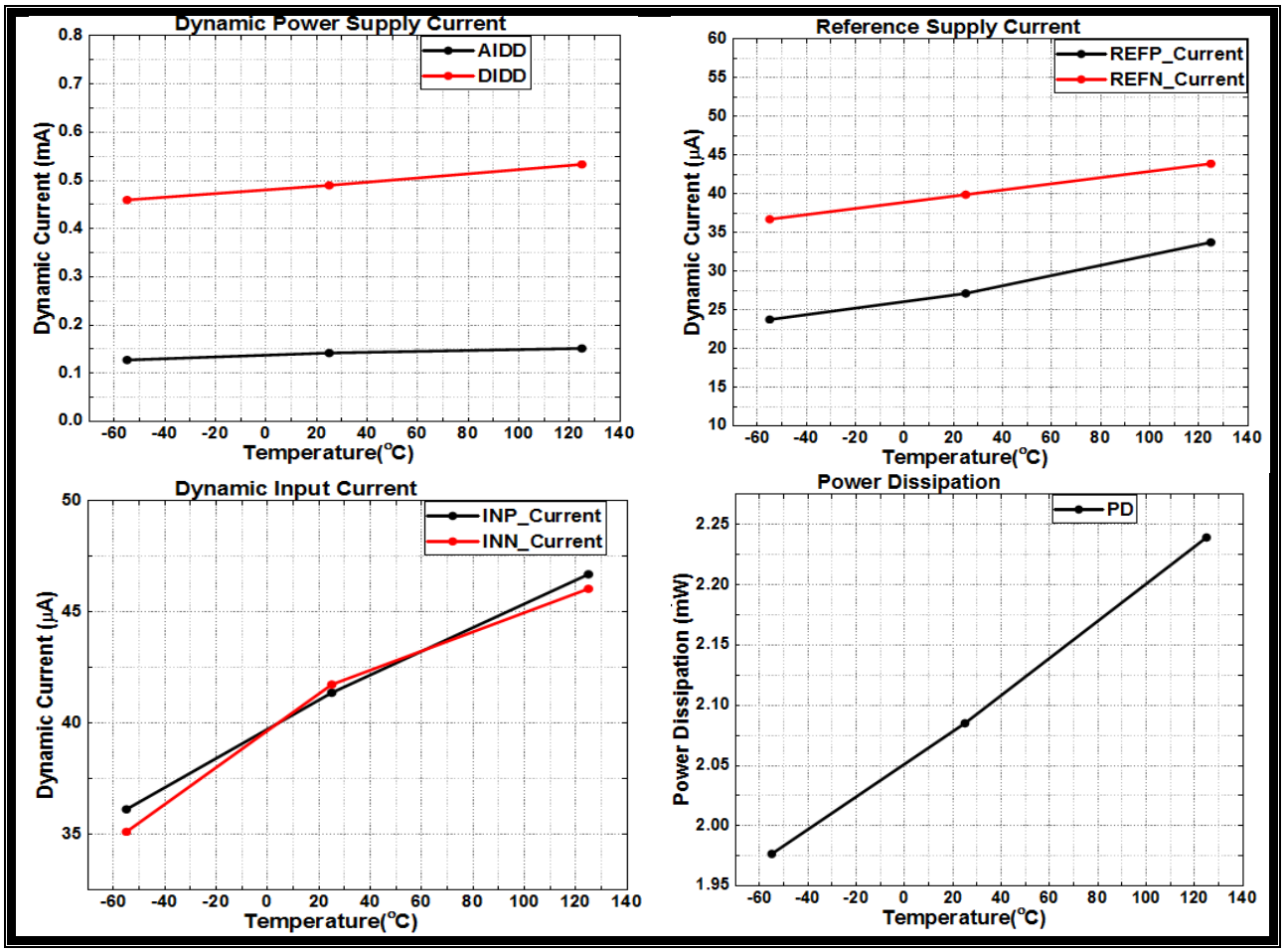

Figure 7: DC Characteristics

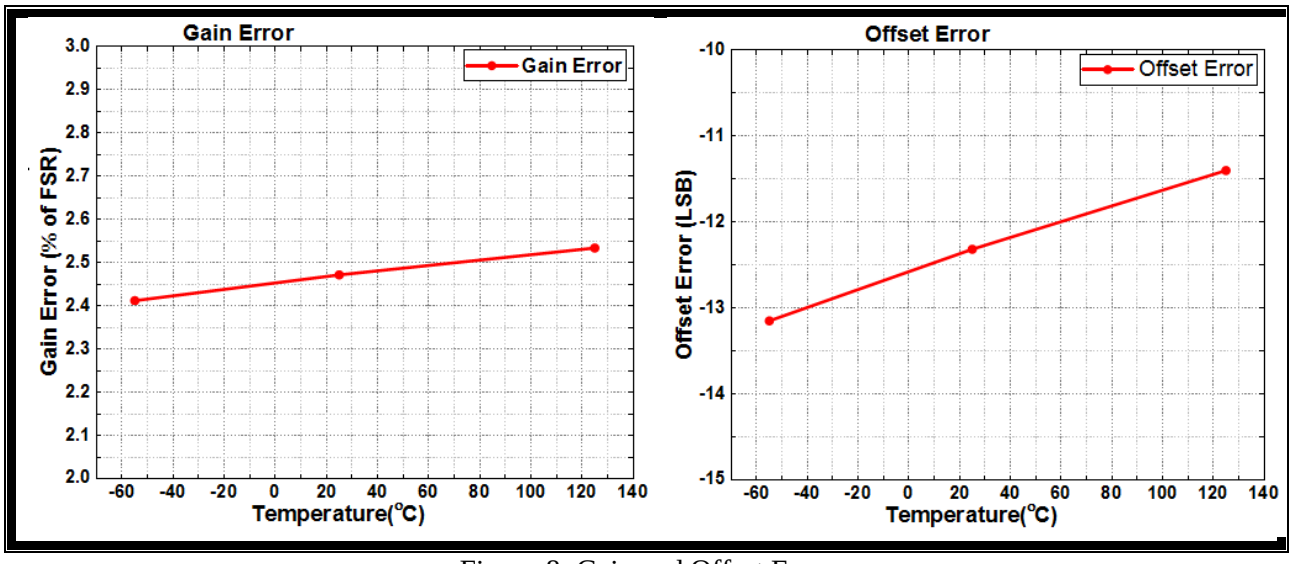

Figure-8: Gain and Offset Error

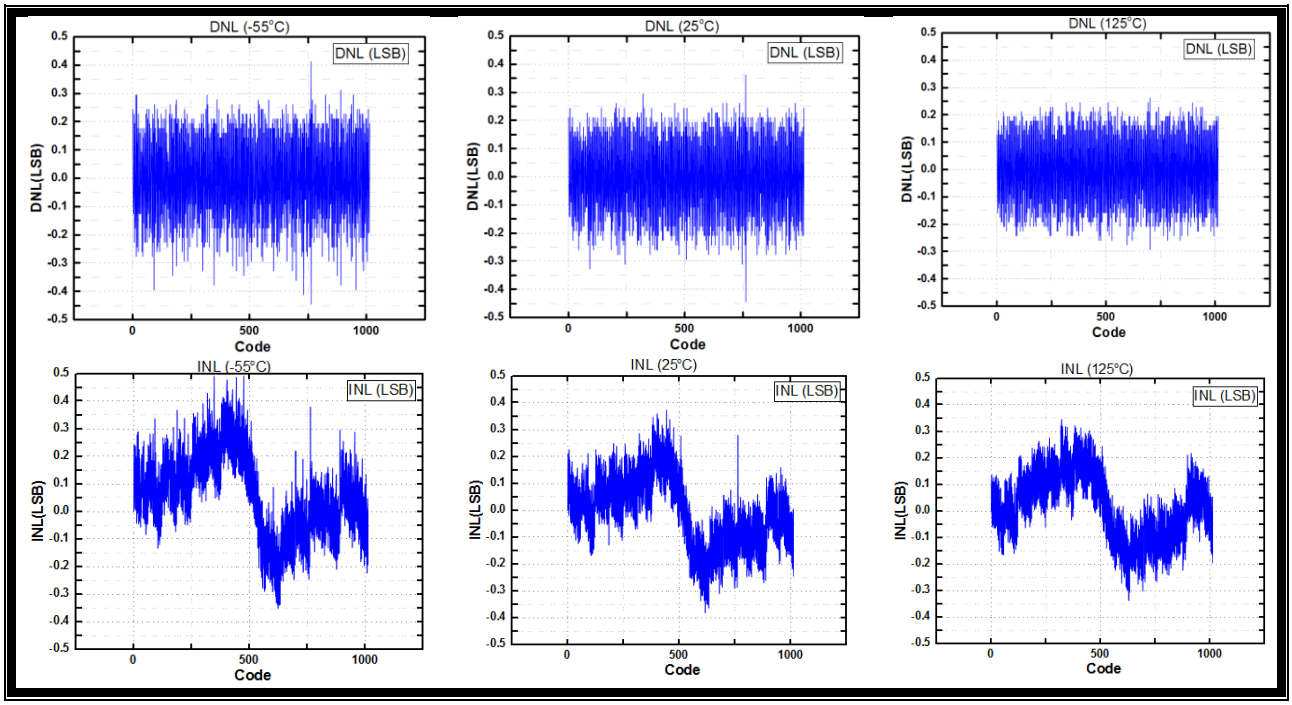

Figure-9: DNL/INL Plots

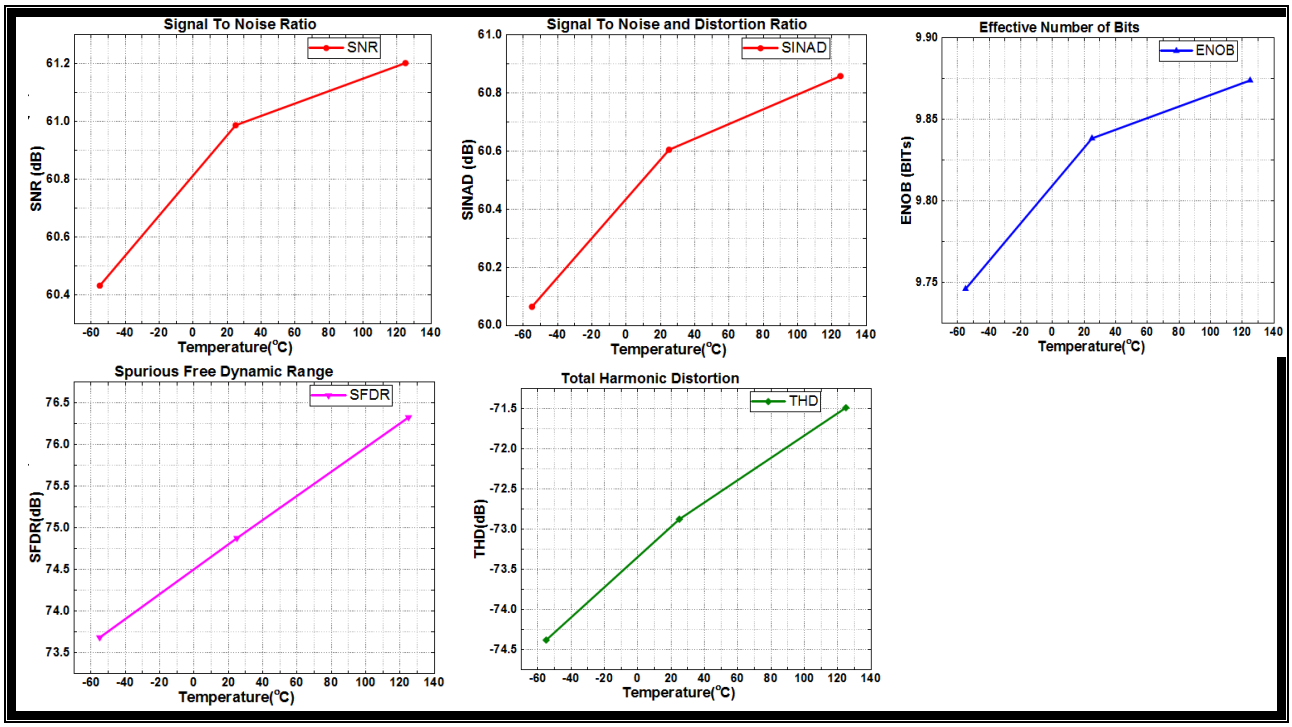

Figure-10: AC Plots

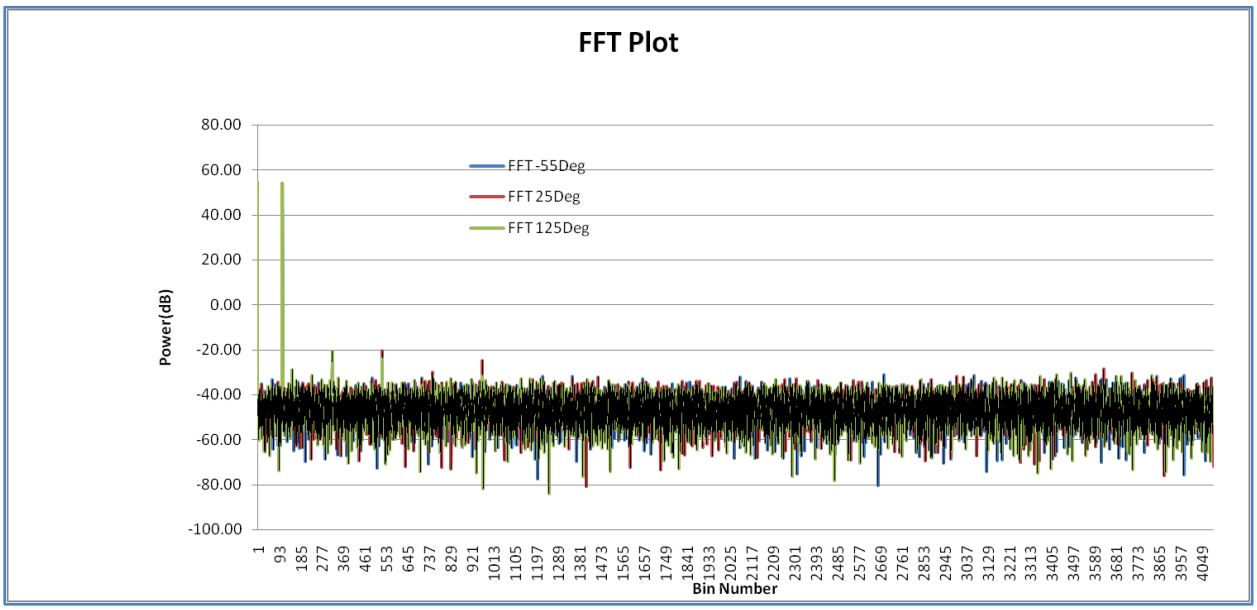

Figure-11: FFT Plots

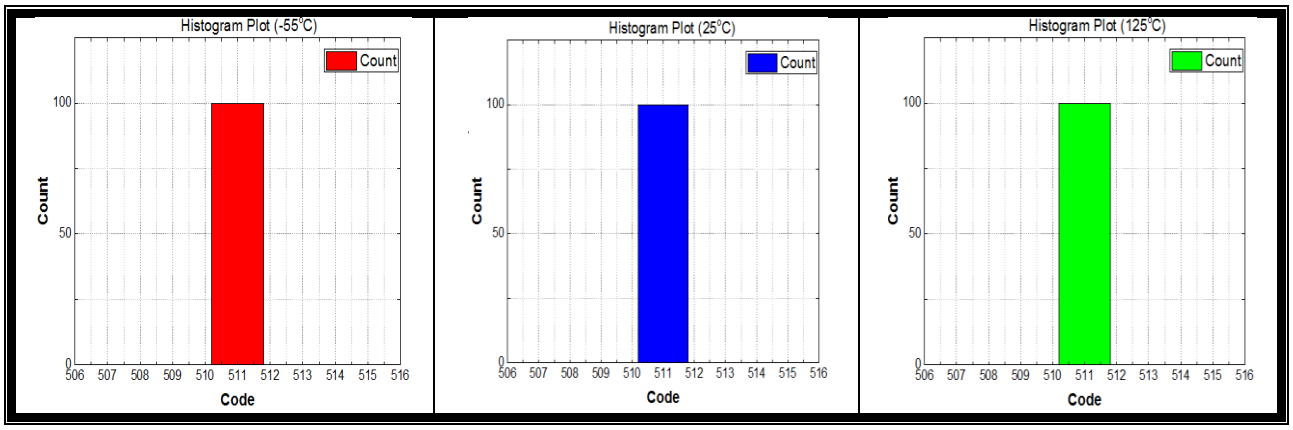

Figure-: 12 Histogram plot of output codes with analog grounded input (IN=1.65V)

OVERVIEW:

DEFINITIONSOF KEY SPECIFICATIONS:

• **Differential Nonlinearity (DNL):** An ideal ADC exhibits code transitions that are exactly 1LSB apart. DNL is the deviation from this ideal value. Therefore, every code must have a finite width. No missing codes guaranteed to 10-bit resolution indicate that all 1024 codes must be present overall operating conditions.

• **Input Referred Noise:** The noise is measured using histogram techniques. The standard deviation of the CSP output codes is calculated in LSB and represents the rms noise level of the total signal chain . The noise can be converted to an equivalent voltage, using the relationship

1 LSB = (ADC full scale / 2^N codes)

Where N is the bit resolution of the ADC.

1 LSB is approximately 3.90625mV.

• **Effective Resolution:** The ratio of the full-scale input range to the rms input noise (from grounded input histogram test) is called as effective resolution.

$$Effective\ resolution = \log_2\left(\frac{2^N}{rms\ input\ noise\ (LSBs)}\right)$$

RMS Input Noise = Standard deviation from Grounded input Histogram Curve

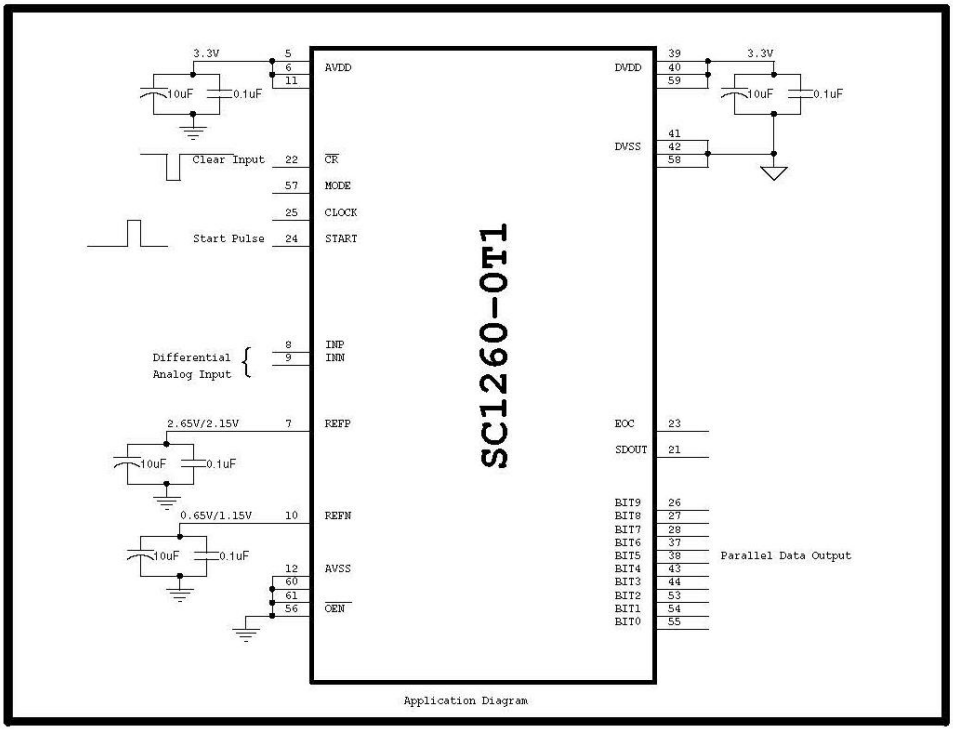

Figure-13: Application Diagram

PACKAGE DRAWING (100 Pin CQFJ):

Note7: All linear dimensions are in inches (mm.)

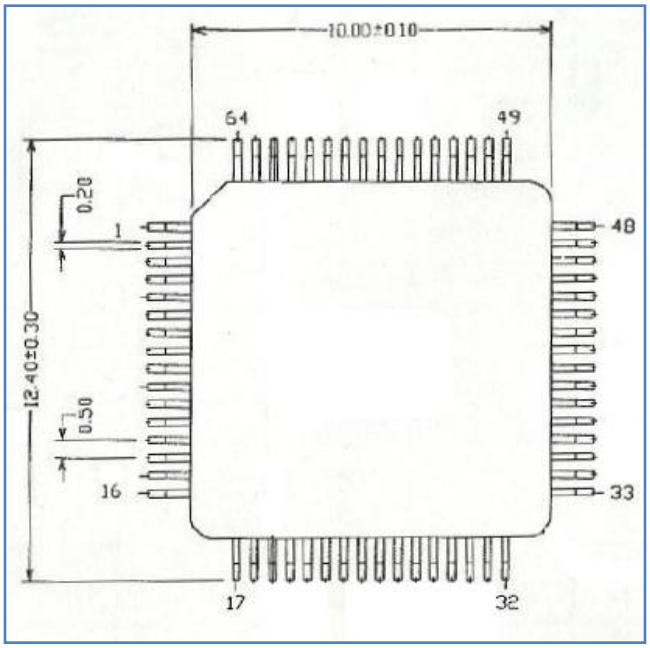

Figure-14: Package Drawing

Revision History			
S.No.	**Version**	**Date of release**	**Description**
1	1.0	October 20, 2022	
2			
3			
4			

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