SC1259-0

DATASHEET

Version 1.0 December 2021

SINGLE CHANNEL 24 BIT CAPACITANCE TO DIGITAL CONVERTER (ASC)

FEATURES:

- **24 BITS NO MISSING CODES**
- **FULL SCALE INPUT CAPACITANCE RANGE C_{FS} UP TO ±4pF**
- **NOMINAL CAPACITANCE RANGE C_0 UP TO 17.75pF**
- **0.04% INL**
- **18 BITS EFFECTIVE RESOLUTION**
- **PROGRAMMABLE DATA OUTPUT RATESUP TO 8KSPS**
- **ON CHIP TEMPERATURE SENSOR**
- **ON-CHIP OFFSET & GAIN CALIBRATION**
- **SPI COMPATIBLE**
- **3.0V TO 3.6V**
- **180nm SCL CMOS standard logic process**
- **ESD Protection upto ±3KV HBM**

DESCRIPTION:

Accelerometer Signal Conditioner (ASC) is a Sigma Delta Modulator based high resolution Capacitance-to-Digital Converter. It senses the change in the differential capacitance connected at the input and produces a 24 Bit digital code proportional to this change. This device is developed for sensing the capacitance change of *MEMS* based Accelerometer and can be used in other similar applications as well. The capacitance to be sensed can be directly connected at the input of this device.

ASC incorporates a Second Order Sigma Delta (ΣΔ) Modulator. The ΣΔ Modulator converts the difference in the input differential capacitors into a digital 1 bit pulse train whose average duty cycle represents the digitized signal information. The pulse train is then processed by a digital *sinc*^{3} filter to produce a digital output.

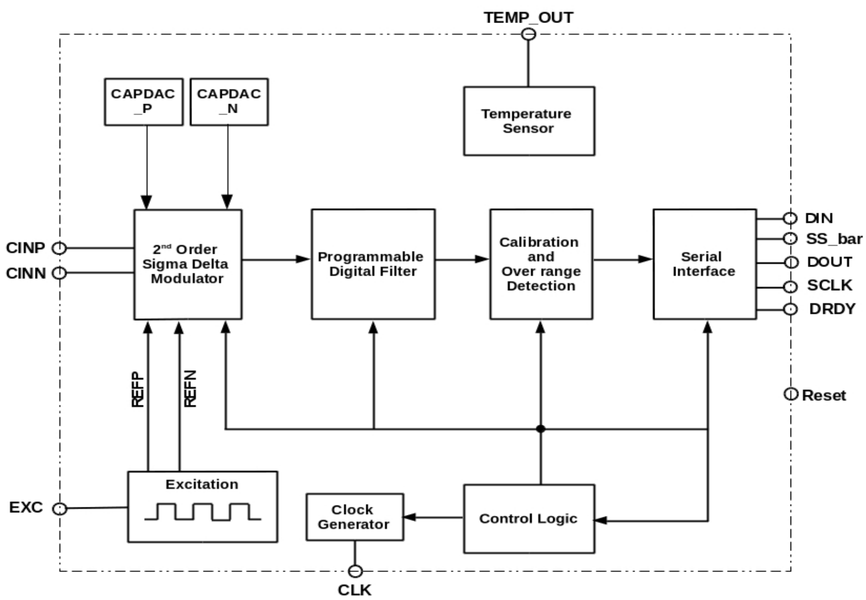


Figure 1: Block Diagram

PIN CONFIGURATION:

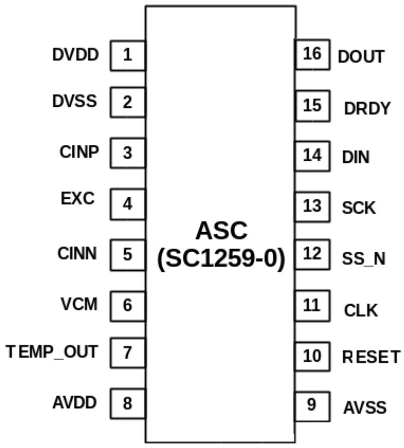


Figure 2: Pin Configuration

PIN DESCRIPTIONS:

PIN NO.	NAME	Pin Type	DESCRIPTION
1	DVDD	Digital Supply	3.3 V – Digital Supply
2	DVSS	Digital Ground	0 V – Digital Ground
3	CINP	Analog Input	CDC Positive Capacitive Input. The positive side capacitor in differential capacitance to be connected between CINP and EXC.
4	CINN	Analog Input	CDC Negative Capacitive Input. The Negative side capacitor in differential capacitance to be connected between CINN and EXC.
5	EXC	Analog Output	CDC Excitation Voltage. This pin should be connected to common terminal of the differential capacitance to be measure.
6	VCM	Analog Output	Common Mode Output (VDD/2). User has to connect a decoupling capacitor of 0.1μF and 1μF at this pin)
7	TEMP_OUT	Analog Output	Output of Temperature Sensor
8	AVDD	Analog Supply	3.3 V – Analog Supply
9	AVSS	Analog Ground	0 V – Analog Ground
10	RESET	Digital Input: Active Low	Reset Signal: Reset the entire Chip
11	CLK	Digital Input	Master Clock
12	SS_N	Digital Input: Active Low	Chip Select
13	SCK	Digital Input	Serial Clock Input
14	DIN	Digital Input	Serial Data Input
15	DOUT	Digital Output	Serial Data Output
16	DRDY	Digital Output: Active Low	Data Ready Signal

Table 1: Pin Descriptions

TIMING SPECIFICATIONS:

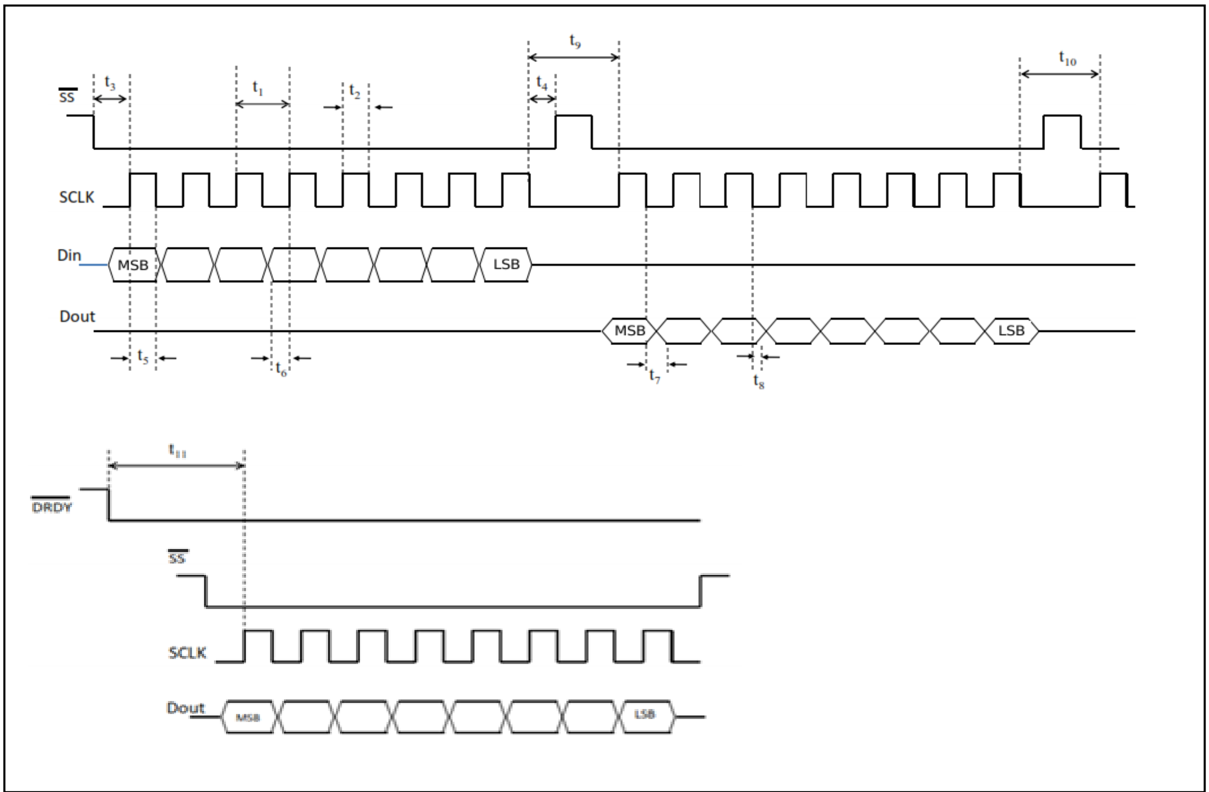


Figure3: Timing Waveform

TIMING SPECIFICATION TABLE:

SPEC	DESCRIPTION	MIN	MAX	UNIT
t_1	SCLK period	4 cycle		t_{CLK} Period
t_2	SCLK pulse width (High and Low)	2 cycle		t_{CLK} Period
t_3	SS low to first SCLK edge	100		ns
t_4	Last SCLK falling edge to SS HIGH	100		ns
t_5	SCK rising edge to DIN valid (Hold time)	50		ns
t_6	DIN valid to SCLK rising edge (Setup time)	50		ns
t_7	SCLK falling Edge to valid new DOUT		50	ns
t_8	SCLK falling Edge to DOUT, Hold Time	0		ns[2]
t_9	Delay between last SCLK edge of 1st byte transfer and first SCLK edge for subsequent 2nd byte transfer : RDATA, RDATAC, RREG, WREG Command	50		t_{CLK} Period
t_{10}	Final SCLK edge of one command until first edge SCLK of next command	4		t_{CLK} Period
t_{11}	DRDY LOW to first SCLK edge of first byte transfer for RDATAC command	15		t_{CLK} Period
t_{11}	DRDY LOW to first SCLK edge of first byte transfer for RDATA command	0		t_{CLK} Period

Table 2: Timing Specification

Notes: (1) DOUT goes immediately into tri-state whenever SS is high

(2) DOUT should be sampled externally on rising edge of SCLK. DOUT will remain valid till next falling edge.

ELECTRICAL CHARACTERISTICS

All Specifications AVDD, DVDD = +3.3V, Temp. = 25^{0}C, OSR = 2048, f_{EXC} = 250 KHz, f_{CLK} = 4 MHz, f_{DATA} = 122 Hz, full scale input capacitance range = ±4pF, unless otherwise specified.

PARAMETER	TEST CONDITIONS/ COMMENT	SC1259-0			UNITS
		MIN	TYP	MAX	
CAPACITIVE INPUT					
Nominal Capacitance C_0				17.75	pF
Full Scale Input Range C_{FS}	User Selectable	±0.5		±4.0	pF
Resolution p-p			24		Bits
No Missing Code			24		Bits
Effective Resolution	Based on 100 samples			18	Bits
Integral Non-Linearity	Best Fit Method			±0.04	% of FSR
Offset Error[1]	Before Calibration			0.2	% of FSR
Gain Error[1]	Before Calibration			0.1	% of FSR
Common-Mode Rejection	At DC	60			dB
CAPDAC_P and CAPDAC_N					
Full Range				15.75	pF
Resolution	6-Bit DAC		±0.25		pF
EXCITATION					
Frequency Range	Programmable	32.5		250	KHz
Voltage			±VDD/4		V
			±3VDD/4		V
			±VDD/2		V
			±VDD		V
TEMP SENSOR					
Temperature Rage		-10		85	°C
Scale Factor			12		mV/°C
Non Linearity				0.85	°C
CLOCK INPUT**** f_{CLK}			5	20	MHz
POWER SUPPLY					
Supply Voltage	AVDD, DVDD	3.0	3.3	3.6	V
Analog Current	IAVDD			6	mA
Digital Current	IDVDD			2	mA
TEMPERATURE RANGE					
Operating		-55		125	ºC

Table3: Electrical Specifications

Note 1. System Calibration can minimize this error.

ELECTRICAL CHARACTERISTICS

All Specifications AVDD, DVDD = +3.3V, Temp. = 25^{0}C, OSR = 2048, f_{EXC} = 250 KHz, f_{CLK} = 4 MHz, f_{DATA} = 122 Hz, full scale input capacitance range = ±4pF, unless otherwise specified.

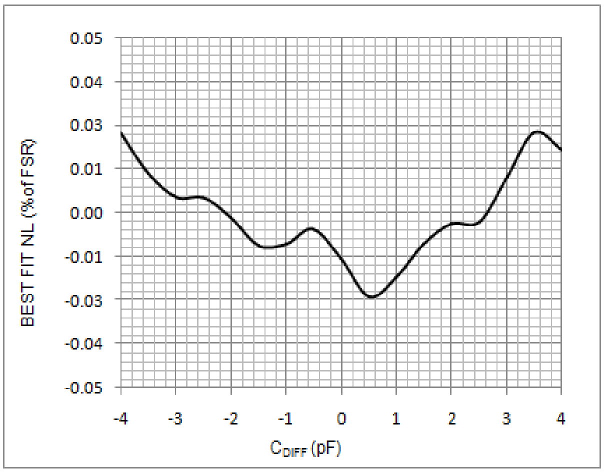


Figure 3: Non linearity versus C_{DIFF}

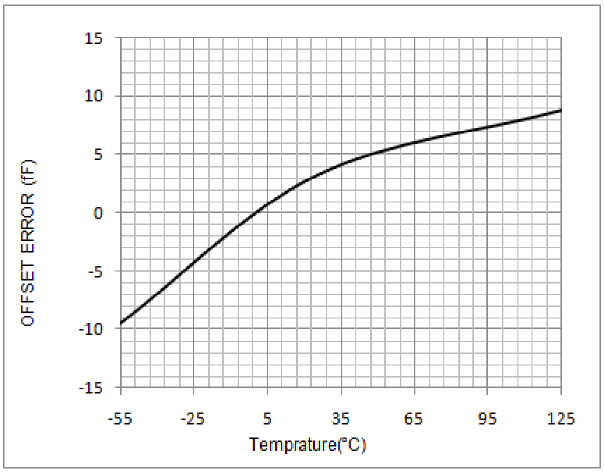


Figure 5: Offset Error versus Temperature

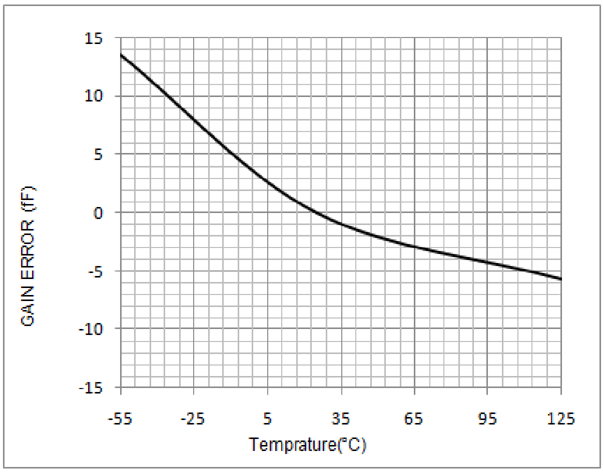


Figure6: Gain Error versus Temperature

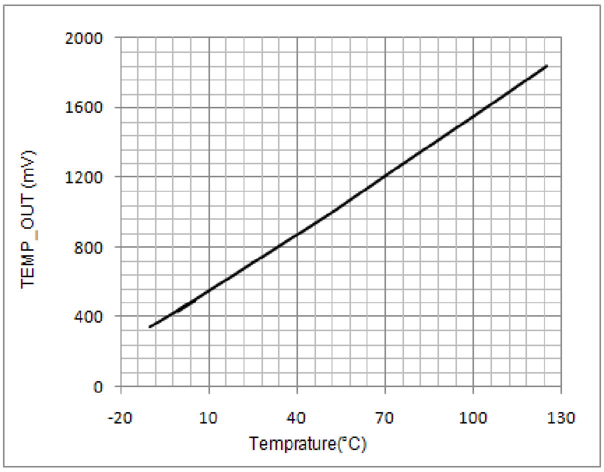


Figure7: TEMP_OUT versus Temperature

DIGITAL CHARACTERISTICS

DVDDO= 3.0V to 3.6V

PARAMETER	TESTS CONDITIONS	SC1259-0			UNITS
		MIN	TYP	MAX	
Logic Family			CMOS		
Logic Level: V_{IH}		2		DVDD	V
V_{IL}		DVSS		0.8	V
V_{OH}	I_{OH}=8mA	3.0			V
V_{OL}	I_{OL}=8mA	DVSS		0.4	V
Input Leakage: I_{IH}	V_I=DVDD			1	μA
I_{IL}	V_I=DVSS	-1			μA

Table 4: Digital Specification

ABSOLUTE MAXIMUM RATING

PARAMETER	SC1259-0		UNITS
	MIN	MAX	
AVDD to AVSS	-0.3	4.3	V
DVDD to DVSS	-0.3	4.3	V
Digital Input Voltage to DGND	-0.3	DVDD+0.3	V
Digital Output Voltage to DVSS	-0.3	DVDD+0.3	V
Digital Output Current		8	mA
Maximum Ambient Temperature		125	°C

Table 5: Absolute Ratings

OVERVIEW

SIGMA DELTA MODULATOR

A second order single loop ∑Δ modulator is used in the ASC. The ∑Δ Modulator converts the change in the input differential capacitance into a digital pulse train whose average duty cycle represents the digitized signal information. As mentioned above the, the full scale input capacitance range C_{FS} of ASC is programmable. Depending on the $C_{DiffMax}$ of any sensor, user can set any value of C_{FS} between 0.5pF and 4pF in steps of 0.5pF. The C_{FS} must be selected in such a way so that $C_{DiffMax}$ should not be more than C_{FS} under full scale input conditions. The CFS can be programmed using *CF2*: *CF0* bits of control register *CR1* as given in the following table:

FS2:FS1:FS0	**C_{FS} (pF)**
000	±4.0
001	±3.5
010	±3.0
011	±2.5
100	±2.0
101	±1.5
110	±1.0
111	±0.5

Table 6: Full Scale Input Range Setting

The values mentioned in the Table 6 are the typical values of C_{FS}. There may be 20% change in these values.
The modulator runs at clock frequency f_{MOD}, which is same as the excitation source frequency f_{EXC}. f_{EXC} and f_{MOD} can be adjusted by setting the appropriate value of *PRE1: PRE0* of *CR2* control register as shown in the following table:

PRE1:PRE0	**f_{EXC} and f_{MOD}**
00	f_{CLK}/16
01	f_{CLK} /32
10	f_{CLK} /64
11	f_{CLK} /128

Table 7: Pre scalar Values

Where, f_{CLK} is external clock frequency. The modulator is designed to work at a maximum sampling frequency of 250 KHz.

PROGRAMMABLE DIGITAL FILTER

The ∑Δ Modulators is followed by an integrated digital filter unit. It comprises of $sinc^3$ digital filter and internal registers. The Decimation Ratio or Oversampling Ratio (OSR) of filter module can be programmed. The on-chip digital filter processes the single bit data stream coming from the corresponding modulator unit using a $sinc^3$ filter. The output Data Rate (DR) of digital filter is given as:

$$Data\ Rate = f_{MOD} / OSR$$

The *3dB* cut off frequency of the filter is *0.262 * DR*. For example, if f_{MOD} is 250 KHz and OSR is 256, then the Data Rate comes out to be 976Hz and maximum input frequency will be 0.262*244 i.e. 255Hz.

The *OSR* of filter can vary from 20 to 2047 and its value is represented by 8 Bits of *DECIM* Register and first 3 LSBs of *CR2* Register. Although, *OSR* can have any of the value between 20 and 2047 but there are fixed numbers of OSRs which are implemented internally. A range of the OSR belongs to a particular fixed internal OSR.

Depending on the selected OSR value from a particular range, filter will provide a gain. The gain of the filter will be:

$$FilterGain = \left(\frac{OSR}{Internal\ OSR}\right)^3$$

A table is given below shows the Filter Gain on a various decimation ratio:

S. No.	Internal OSR	OSR Range		Filter Gain	
		MAX	MIN	MAX	MIN
1	2048	2047	1836	0.99	0.72
2	1626	1835	1458	1.44	0.72
3	1260	1457	1157	1.44	0.72
4	1024	1156	919	1.44	0.72
5	813	918	729	1.44	0.72
7	645	728	579	1.44	0.72
8	512	578	459	1.44	0.72
9	406	458	365	1.43	0.72
10	323	364	290	1.43	0.72
11	256	289	230	1.44	0.72
12	203	229	182	1.43	0.72
13	161	181	145	1.41	0.73
14	128	144	115	1.42	0.72
15	102	114	92	1.41	0.74
16	81	91	73	1.44	0.74
17	64	72	58	1.42	0.74
18	51	57	46	1.41	0.74
19	40	45	36	1.39	0.71
20	32	35	29	1.31	0.74
21	25	28	23	1.34	0.74
22	20	20	22	1.3	1

Table 8: Oversampling Ratio

Depending on the value on OSR, user can calculate Filter Gain. The output code of the filter data will be scaled by the corresponding Filter Gain. For e.g., If OSR = 1350, the Corresponding Internal OSR of the filter is 1260 (S. No. 3), then the filter gain is given as:

$$FilterGain = \left(\frac{1350}{1260}\right)^3 = 1.23$$

The filter gain can be corrected using Gain Calibration.

The ∑Δ modulator along with the programmable digital filter forms the Capacitance-to-Digital (CDC) Converter.

EXCITATION SOURCE

It provides excitation to the differential input capacitance. The capacitance to be measured should be connected between EXC and ASC input (CINP and CINN) as shown in below Figure. ASC outputs a square wave on ECX pin. The amplitude V_{EXC} and frequency f_{EXC} of this square wave are programmable. The voltage appears across the input capacitors C_P and C_N will be half of V_{EXC}. For e.g. if V_{EXC} is VDD, then ±VDD/2 will appear across the input capacitors C_P and C_N. f_{EXC} can be programmed using *PRE1:PRE0* bits of *CR2* control register as mentioned in Table 6. V_{EXC} can be programmed using *EXC1*:*EXC0* control bits of control register CR1.

EXC1:EXC0	V_{EXC}
00	*VDD*
01	±3VDD/4
10	±VDD/2
11	±VDD/4

Table 9: Excitation Source Amplitude

The common mode voltage of V_{EXC} is VDD/2.

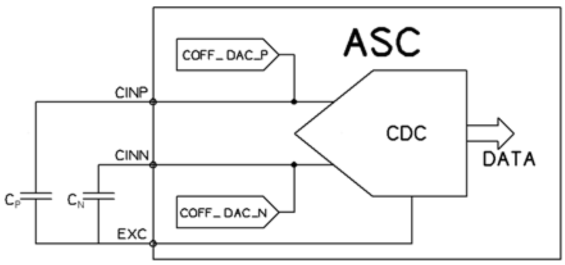


Figure 8: Differential Mode

CAPDAC

The input capacitance full scale range C_{FS} of the ASC is programmable. Depending on full scale capacitance of the Sensor, user can program the value of CFS from 0.5pF to 4pF in steps of 0.5pF.

ASC can accept higher nominal capacitance C_0 of differential sensor. The nominal capacitance of the sensor can be balanced using *CAPDAC*. *CAPDAC* is the negative capacitance connected at the input pin.

ASC consists of two independent *CAPDACs*; *CAPDAC_P* to balance the capacitance on *CINP* and *CAPDAC_N* to balance the capacitance on *CINN*. The effective capacitance of *CINP* C_{INPeff} will be the difference of C_P and CAPDAC_P. Similarly effective capacitance of *CINN* C_{INNeff} will be the difference of C_N and CAPDAC_N. The differential capacitance which will be sensed by the ASC is given as:

$$C_{DIFF} = C_{INPeff} - C_{INNeff=} = (C_P - CAPDAC\_P) - (C_N - CAPDAC\_N)$$

The maximum possible value of *CAPDAC_P* and *CAPDAC_N* is 15.75pF and its resolution is 0.25pF. The values of *CAPDAC_P* and *CAPDAC_N* can be set independently using the *CAPDAC_P5:CAPDAC_P0* control bits of *CAPDAC_P* register and *CAPDAC_N5:CAPDAC_N0* control bits of *CAPDAC_N* register respectively. Typically, the total value of each CAPDAC is given as:

$$C_{CAPDAC\_P} = 0.25\,pF * (CAPDAC\_P5{:}\,CAPDAC\_5P0)_{10}$$

$$C_{CAPDAC\_N} = 0.25\,pF * (CAPDAC\_N5{:}\,CAPDAC\_5N0)_{10}$$

For e.g. if decimal equivalent of *CAPDAC_P5:CAPDAC_P0* is 17, then C_{CAPDAC_P} will be 4.25pF. If decimal equivalent of *CAPDAC_N5:CAPDAC_N0* is 63, then C_{CAPDAC_N} will be 15.75pF.

The *CAPDACs* should be used if value of C_P or C_N is more than C_{FS}. When C_P or C_N is more than C_{FS}, then user should set the *CAPDAC_P* and *CAPDAC_P* in such a way so that under full scale input conditions, C_{INPeff} and C_{INNeff} should not be more than C_{FS}.

Few cases of selecting appropriate value of C_{FS} and both the *CAPDACs* as well as the corresponding ideal digital code (assuming 2's Compliment Data Format) are tabulated in Table 9.

As, it can be seen from above table that in any case, C_{INPeff} and C_{INNeff} is not more than C_{FS}. For the same value of C_0 and C_{FS}, user can used different combinations of *COFFDAC* as shown in Case2 and 3. It is recommended that USER should not use *COFFDAC* unless it is not required.

S. No.	Input	C_0 (pF)	$C_{Diffmax}$ (pF)	C_P (pF)	C_N (pF)	C_{FS} (pF)	CAPDAC_P (pF)	CAPDAC_N (pF)	C_{INPeff} (pF)	C_{INNeff} (pF)	C_{Diff} (pF)	Ideal Digital Code
1.0	0	2	4	2	2	4	0	0	2	2	0	000000
	+ F.S.	2	4	4	0	4	0	0	4	0	4	7FFFFF
	- F.S.	2	4	0	4	4	0	0	0	4	-4	800000
2.1	0	6	2	6	6	2	5	5	1	1	0	000000
	+ F.S.	6	2	7	5	2	5	5	2	0	2	7FFFFF
	- F.S.	6	2	5	7	2	5	5	0	2	-2	800000
2.2	0	6	2	6	6	2	7	5	-1	-1	0	000000
	+ F.S.	6	2	7	5	2	7	5	0	-2	2	7FFFFF
	- F.S.	6	2	5	7	2	7	5	-2	0	-2	800000
3.1	0	10	3	10	10	3	8.5	8.5	1.5	1.5	0	000000
	+ F.S.	10	3	11.5	8.5	3	8.5	8.5	3	0	3	7FFFFF
	- F.S.	10	3	8.5	11.5	3	8.5	8.5	0	-3	-3	800000
3.2	0	10	3	10	10	3	11.5	11.5	-1.5	-1.5	0	000000
	+ F.S.	10	3	11.5	8.5	3	11.5	11.5	0	-3	3	7FFFFF
	- F.S.	10	3	8.5	11.5	3	11.5	11.5	-3	0	-3	800000
4.0	0	17.75	4	17.75	17.75	4	15.75	15.75	2	2	0	000000
	+ F.S.	17.75	4	19.75	15.75	4	15.75	15.75	4	0	4	7FFFFF
	- F.S.	17.75	4	15.75	19.75	4	15.75	15.75	0	-4	-4	800000

Table 10: Selection of C_{FS} and CAPDACs in Differential Mode

Single Ended Measurement Mode

ASC is developed for the differential mode capacitance measurements. But the device can also be used for Single Ended Capacitance Measurement as well. The Single Ended Sensor C_{IN} can be connected between *EXC* and C_{INP} and C_{INN} can be left open as shown in Fig. 7.

As explained in the ∑Δ Modulator section previously, USER should select C_{FS} range depending on the maximum capacitance change (C_{inFS}) possible in sensor capacitance. The C_{FS} should be selected in such a way so that C_{inFS} must always be less than or equal to C_{FS}.

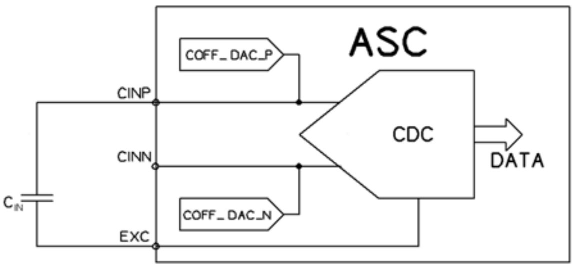


Figure 9: Single Ended Mode

The nominal capacitance C_0 (Not Changing) of input sensor must be balanced using CAPDAC. ASC will produce the digital code corresponding to the capacitance C_{SINGLE}.

$$C_{SINGLE} = \left(C_{IN} - (CAPDAC\_P - CAPDAC\_N)\right)$$

The value of both the CAPDACs must be set equal to nominal value C_0 of input sensor. Because of limited resolution of CAPDAC, if it is not possible to set CAPDACs equal C0, then it must be set nearest to C0 and the initial difference between CAPDAC and C0 can be taken care of System Offset Calibration, if the difference is within the calibration range. In single ended case, ASC can handle the Nominal capacitance up to 15.75pF.

In case of Single Ended case, if the 2's compliment data format is selected, then output code will vary from 000000 to 7FFFFF and if unipolar data format mode is selected then output code will vary from 000000 to FFFFFF. Assuming Unipolar Data Format is selected, a table is given below for selection of C_{FS} and CAPDACs:

S. No.	Input	C_0 (pF)	C_{inFS} (pF)	C_{IN} (pF)	C_{FS} (pF)	CAPDAC_P (pF)	CAPDAC_N (pF)	C_{Single} (pF)	Ideal Digital Code
1	0	0	4	0	4	0	0	0	000000
	+F.S.	0	4	4	4	0	0	4	FFFFFF
2	0	4	2	4	2	4	4	0	000000
	+F.S.	4	2	6	2	4	4	2	FFFFFF
3	0	10	1	10	1	10	10	0	000000
	+F.S.	10	1	11	1	10	10	1	FFFFFF
4	0	15.75	4	15.75	4	15.75	4	0	000000
	+F.S..	15.75	4	19.75	4	15.75	4	4	FFFFFF

Table 11: Selection of C_{FS} and CAPDACs in Single Ended Mode

SERIAL INTERFACE

The serial interface is standard four-wire SPI compatible (DIN, DOUT, SCK and SS_N). USER can communicate to ASC using serial interface. The SPI works in mode 00 i.e. clock phase is 0 and clock polarity is also 0. SPI serial interface signals are described below:

SS_N (Serial Interface Enable)

The SS_N input must be externally asserted before a master device can exchange data with the ADC. SS_N must be low for the duration of the transaction. DOUT pin will become tri-state when SS_N goes high. After data read operation, it should be made high.

SCK (serial clock)

SCK function as a clock for serial communication. The device will sample serial data on positive edge of SCK. Data from ASC will be launched on negative edge of SCK.

DIN (Data input)

DIN is the serial data input port. DIN is internally sampled at positive edge of SCK by SPI.

DOUT (Data Output)

DOUT is the serial data output port. DOUT is internally launched by SPI at negative edge of SCK by SPI. DOUT immediately goes into tri-state when SS_N is high.

DRDY (DATA READY)

The DRDY pin is used as a status signal to indicate when new digital code is ready to be read from the ASC. DRDY goes low when new data is available. It goes high in the mid of the second byte read during read operation from the data register. In case, in response to the DRDY assertion no read operation is performed, DRDY will remain low till next Data cycle. It is mandatory for the user to read at least two bytes, otherwise the DRDY will remains low till next Data cycle.

CALIBRATION

The offset and gain errors in the ASC or the complete system, can be reduced with calibration. User can carry out system calibration to reduce offset and gain errors. For system calibration, the appropriate capacitor must be connected to the inputs. The system offset calibration command requires a “zero” differential capacitor C_{DIFF}. It then computes an offset that will nullify offset in the system. The system gain calibration command requires a positive full scale C_{DIFF} i.e. $C_{DIFF} = C_{FS}$. It then computes a value to nullify gain errors in the system. At the completion of calibration, the DRDY signal will go LOW to indicate that calibration is complete and valid data is available.

(Note: To read internal Offset Correction Register (OCR) and Full Scale Register (FSR) value, RREG command should be used with appropriate register address.)

SYSTEMOCAL commands will only update the Offset Calibration Register of the ASC with appropriate offset value. However, to enable the offset correction, OCEN bit of CR1 control register has to be set separately. Similarly to enable the Gain Calibration set GCALEN bit of CR1. The offset and gain calibration module can correct up to 50% of Full Scale Range. Calibration of ASC must be performed after system reset, a change in decimation ratio, a change in CFS, a change in the COFFDEC value, or a change in Excitation source frequency or Amplitude.

Apart from above commands, OSR and FSR of the selected ADC core can be accessed externally through RREG (Read Register) and WREG (Write Register) commands. This will provide flexibility to manually set the OCR and FSR. When FSR is externally loaded, follow the procedure as below:

- Perform System gain calibration as sated above and read the FSR register and note down the value.
- Divide FFFFFC00000 by noted value of FSR register and take its integer portion.
- This calculated value has to be written into FSR register at next power ON in order to perform gain calibration without command.

For example:
Let us assume noted value of FSR register is 3ee259.
The value to be written in the FSR reg. after power off and on will be:
FFFFFC00000/3ee259 = 4122B7.

OVER-LOAD & OVER-RANGE DETECTION MODULE:

These Modules prevents rollover of digital output code when differential capacitance of sensor C_{DIFF} exceeds the full scale capacitance range C_{FS} .Digital output code will be clipped at $(7FFFFF)_H$ and $(800000)_H$ when C_{DIFF} exceeds positive and negative full scale respectively. In case the ADC input is more than 50 % of full scale range, the Over Load detection module will clipped the digital output at $(7FFFFF)_H$ or $(800000)_H$, accordingly.

Over-Range Detection Module also keeps into consideration of digital calibration. i.e. Any rollover of digital output due to calibration will also be detected by Over Range Detection Module and will be clipped appropriately to $(7FFFFF)_H$ and $(800000)_H$. To ensure the proper functioning of the Over Range Detection Module, following constraint on OCR & FSR register value must be followed:

1. Maximum value of OCR register should not exceed $3FFFFF_H$ for negative offset correction and $C00000_H$ for positive offset correction.

2. FSR value must be positive.

By default Over-Load and Over-Range Detection Modules are enabled.

1. Over-Load Detection module (OLDD)

- In the scenario where digital code without calibration is such that it cannot be corrected after calibration then Over-Load detection module detects over-load and clip digital output appropriately to $(7FFFFF)_H$ and $(800000)_H$.

- Over-load detection can be disabled by setting OLDD bit of *CR2* control register.

2. **Over-Range Detection module (ORDD)**

- Over-range module checks for the digital code after digital offset and gain calibration. If digital code after gain and offset calibration is out of the acceptable code range then digital over-range module detects over-range and clip digital output appropriately to $(7FFFFF)_H$ and $(800000)_H$.

- Over-range detection can be disabled by setting ORDD bit of CR2 control register.

Over-Load Detection and Over-Range Detection can be disabled by setting OLDD and ORDD bits of CR2 register respectively. ORDD bit also affects digital output range. Setting ORDD bit will half the digital output range as shown in Table-12. In case of Over-Load or Over-Range detection, the primary output pin ORD will become high. This ORD pin will be correspond to the selected ADC core.

ORDD bit	C_{DIFF}	**DIGITAL OUTPUT CODE**
ORDD = 0	$+C_{FS}$	$7FFFFF_H$
	0	000000_H
	$-C_{FS}$	800000_H
ORDD = 1	$+C_{FS}$	$3FFFFF_H$
	0	000000_H
	$-C_{FS}$	$C00000_H$

Table 12: Full scale code range correspond to different ORDD flag value

OUTPUT CODE FORMAT

Two options of the output data format are available in SC1259: Two's Compliment and Unipolar. Any of the data format may be chosen based on the Data_format bit CR2.

C_{Diff}	**Unipolar**	**Two's Compliment**
$-C_{FS}$	000000	800000
0	000000	000000
$+C_{FS}$	FFFFFF	7FFFFF

Table 13: Output Data Format

TEMPERATURE SENSOR

An on chip temperature sensor is provided whose output is independently available in analog form. In case user wants to digitize the output of the temperature sensor, its output should be shorted externally with the input of one of the ADC. The temperature sensor is PTAT based temperature sensor.

COMMAND DEFINITIONS

The commands listed below control the operation of SC1259-0 Device. Some commands are stand-alone commands (e.g. STOPC) while others require additional bytes (e.g., WREG requires command and the data bytes).
Operands:
rrrr represents the register address.

nnnnnnnn represents the data.

xxxx: these bits will be ignored while instruction decoding.

COMMANDS	DESCRIPTION	COMMAND BYTE	2ND COMMAND BYTE
RDATA	Read Data	0001 xxxx ($1x_H$)	-N.A.-
RDATAC	Read Data Continuously	0011 xxxx ($3x_H$)	-N.A.-
STOPC	Stop Read Data Continuously	1111 xxxx (Fx_H)	-N.A.-
RREG	Read from Register rrrr	0100 r r r r ($4r_H$)	-N.A.-
WREG	Write to Register rrrr	0101 r r r r ($5r_H$)	nnnn_nnnn (value of reg–rrrr)
SYSOCAL	System Offset Calibration	0111 xxxx ($7x_H$)	-N.A.-
SYSGAIN	System Gain Calibration	1001 xxxx ($9x_H$)	-N.A.-

Table 14: Commands

RDATA (Read Data):
This command reads a single 24-bit ADC conversion result. In response to RDATA command ADC transmit 24-bit digital code. Digital code is available at DOUT pin in 8-bit format with most significant byte first. RDATA command must be followed by 3-byte read operation. On completion of read operation, DRDY goes high.

Operands: None
Bytes: 1
Encoding: 0001 xxxx

RDATAC (Read Data Continuous)
RDATAC (Read Data Continuous) command enables the continuous output of new data on each DRDY. This command eliminates the need to send the Read Data Command on each DRDY. In case of read data continuous command user can directly perform 3 read operation to read 24-bit digital code. DRDY will go high in response to 3-byte read operation. This mode will be terminated by the STOPC (Stop Read data Continuous) command.

RDATAC command must be followed by STOPC command before issuing any other command.

Operands: None
Bytes: 1
Encoding: 0011 xxxx

STOPC (Stop Read Data Continuous)
Description: Ends the continuous data output mode. After this command DRDY will also go high.
Operands: None
Bytes: 1
Encoding: 1111 xxxx
Data Transfer Sequence:

RREG (Read Register)

RREG (Read Register) command reads content of the specified register. The address of the register to be read is specified in the LSB nibble of the instruction.

Operands: None
Bytes: 2
Encoding: 0100 rrrr

rrrr: Defines register address as mentioned in the Table 8.

WREG (Write Register)

WREG (Write Register) command writes the data to specified register. The address of the register to be written is specified in the LSB nibble of the instruction. Second byte represents the data to be written.

Operands: r, n
Bytes: 2
Encoding: 0101 rrrr nnnn nnnn

rrrr: Defines register address as mentioned in the Table 8.
nnnn nnnn : value of reg–rrrr

SYSOCAL (System Offset Calibration):

SYSTEMOCAL command performs system offset calibration. In case of system offset calibration ADC computes the offset value based on the available differential input signal on selected analog channel to nullify offset in the system.

At the end of the calibration process, offset value will be stored in 24-bit internal Offset Calibration Register (OCR). The offset value stored in Offset Calibration Register (OCR) is in 2's complement format.

DRDY will be asserted to indicate completion of the command.

Operands: none
Bytes: 1
Encoding: 0111 xxxx

SYSGAIN (System Gain Calibration):

This command performs System gain Calibration. In case of system offset calibration, the value of the gain calibration coefficient is calculated based on the available input differential signal. At the end of the calibration process, gain calibration coefficient value will be stored in 24-bit internal FSR.

DRDY will be asserted to indicate completion of the command.

Operands: none
Bytes: 1
Encoding: 1001 xxx

CONTROL / STATUS REGISTERS

The operation of the device is set up through following control / status registers.

Address	Register	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0_H	digital_code_B1 (R)	DC23	DC22	DC21	DC20	DC19	DC18	DC17	DC16
1_H	digital_code_B2 (R)	DC15	DC14	DC13	DC12	DC11	DC10	DC9	DC8
2_H	digital_code_B3 (R)	DC7	DC6	DC5	DC4	DC3	DC2	DC1	DC0
3_H	CR1 (RW)	FS2	FS1	FS0	OCEN	GCALEN	--	EXC1	EXC0
4_H	CR2(RW)	Data_ format	OLDD	ORDD	PRE1	PRE0	OSR10	OSR9	OSR8
7_H	DECIM_reg	OSR7	OSR6	OSR5	OSR4	OSR3	OSR2	OSR1	OSR0
8H	OCR1 (RW)	OCR7	OCR6	OCR5	OCR4	OCR3	OCR2	OCR1	OCR0
9_H	OCR2 (RW)	OCR15	OCR14	OCR13	OCR12	OCR11	OCR10	OCR9	OCR8
A_H	OCR3 (RW)	OCR23	OCR22	OCR21	OCR20	OCR19	OCR18	OCR17	OCR16
B_H	FSR1 (RW)	FSR7	FSR6	FSR5	FSR4	FSR3	FSR2	FSR1	FSR0
C_H	FSR2 (RW)	FSR15	FSR14	FSR13	FSR12	FSR11	FSR10	FSR9	FSR8
D_H	FSR3 (RW)	FSR23	FSR22	FSR21	FSR20	FSR19	FSR18	FSR17	FSR16
E_H	CAPDAC_N (RW)	-	-	CAPDAC_N5	CAPDAC_N4	CAPDAC_N3	CAPDAC_N2	CAPDAC_N1	CAPDAC_N0
F_H	CAPDAC_P (RW)	-	-	CAPDAC_P5	CAPDAC_P4	CAPDAC_P3	CAPDAC_P2	CAPDAC_P1	CAPDAC_P0

Table 15: Control / Status Registers

R: Read only registers
RW: Read/Write registers
Note: At reset all registers are initialized to 00_H on reset.

CR1 (ADD: 03_H) CONTROLREGISTER-1

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FS2	FS1	FS0	OCEN	GCALEN	-	EXC1	EXC00

Bit 7-5 : FS2:FS1:FS0: Full Scale Input Capacitance C_{FS} Range Selection Bits.
Refer to Table 5 for more details

Bit 4: OCEN: Offset Calibration Enable bit
OCE = 1: Enable offset calibration
OCE = 0: Disable offset calibration

Bit 3: GCALEN: Gain calibration Enable bit
GCALEN = 1: Enable Gain calibration
GCALEN = 0: Disable Gain calibration

Bit 4: Not Used

Bit 1-0: EXC1:EXC0: Excitation Source Amplitude Selection Bits.
Refer to table 8 for more details

CR2 (ADD: 04_H) CONTROL REGISTER- 2

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Data_ format	OLDD	ORDD	PRE1	PRE0	OSR10	OSR9	OSR8

Bit 7: Data_format: format of the output code
Data_format = 1: Uni-polar Output
Data_format = 0: 2's complement output

Bit 6: OLDD: Over-Load Detection Disable
OLDD = 0: Enable over-load detection.
OLDD = 1: Disable over-load detection.

Bit 5: ORDD: Over-Range Detection Disable
ORDD = 0: Enable over-range detection.
ORDD = 1: Disable over-range detection.

Bit 4-3: PRE1:PRE0: Prescaler Bits.
Refer to Table 7 for more details.
Bit 2-0: OSR10: OSR9: OSR8: OSR control bits.
Three Most Significant Bits of 11 bits of decimation ratio.

DECIM_reg (ADD: 07_H) Control Register - 3 (Read/Write)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
OCR07	OCR06	OCR05	OCR04	OCR03	OCR02	OCR01	OCR00

Bit 7-0: OSR7:OSR0

8 Least Significant Bits of 11 bit decimation ratio.

OCR1 (ADD: 08_H) OFFSET CALIBRATION REGISTER-1
(Least Significant Byte)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
OCR07	OCR06	OCR05	OCR04	OCR03	OCR02	OCR01	OCR00

OCR2 (ADD: 09_H) OFFSET CALIBRATION REGISTER-2
(Middle Byte)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
OCR15	OCR14	OCR13	OCR12	OCR11	OCR10	OCR09	OCR08

OCR3 (ADD: $0A_H$) OFFSET CALIBRATION REGISTER-3
(Most Significant Byte)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
OCR23	OCR22	OCR21	OCR20	OCR19	OCR18	OCR17	OCR16

Note: 24-bit OCR (OCR3:OCR2:OCR1) register holds the value in 2's Complement format. Its value can be positive and Negative.

FSR1 (ADD: $0B_H$) FULL SCAEE REGISTER-1
(Least Significant Byte)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FSR07	FSR06	FSR05	FSR04	FSR03	FSR02	FSR01	FSR00

FSR2 (ADD: $0C_H$) FULL SCAEE REGISTER-2
(Middle Byte)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FSR15	FSR14	FSR13	FSR12	FSR11	FSR10	FSR09	FSR08

FSR3 (ADD: $0D_H$) FULL SCAEE REGISTER-3
(Most Significant Byte)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FSR23	FSR22	FSR21	FSR20	FSR19	FSR18	FSR17	FSR16

Note: 24-bit FSR (FSR3:FSR2:FSR1) holds the value in 2's Complement format. The value of FSR must always be positive.

CAPDAC_N (ADD: $0E_H$) (Read/Write)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
DC23	DC22	DC21	DC20	DC19	DC18	DC17	DC16

The CAPDAC_N registers bits control the capacitance of CAPDAC_N. The total capacitance of CAPDAC_N is given as:

C_{CAPDAC_N} = 0.25 pF*(Decimal Equivalent of *CAPDAC_N5:CAPDAC_N0*)

CAPDAC_P (ADD: $0F_H$) (Read/Write)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
DC23	DC22	DC21	DC20	DC19	DC18	DC17	DC16

The CAPDAC_N registers bits control the capacitance of CAPDAC_N. The total capacitance of CAPDAC_N is given as:

C_{CAPDAC_N} = 0.25 pF*(Decimal Equivalent of CAPDAC_*N5:CAPDAC_N0*)

DIGITAL_CODE_B3 (ADD: 00_H) DIGITAL OUTPUT CODE (MOST SIGNIFICANT BYTE)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
DC23	DC22	DC21	DC20	DC19	DC18	DC17	DC16

DIGITAL_CODE_B2 (ADD: 01_H) DIGITAL OUTPUT CODE (MIDDLE BYTE)

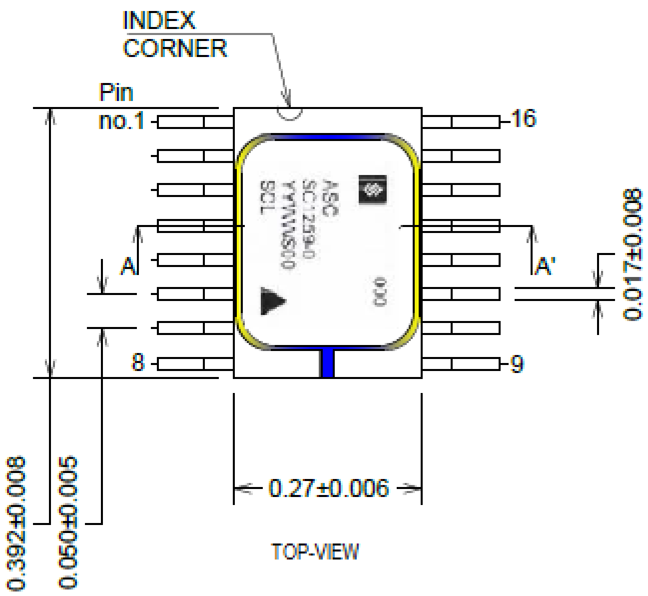
BIT7	BIT6	BIT5	BIT4		BIT3	BIT2	BIT1	BIT0
DC15	DC14	DC13	DC12		DC11	DC10	DC09	DC08

DIGITAL_CODE_B1 (ADD: 02_H) DIGITAL OUTPUT CODE (LEAST SIGNIFICANT BYTE)

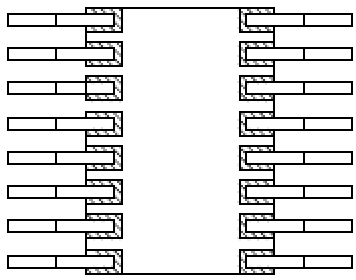
BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
DC07	DC06	DC05	DC04	DC03	DC02	DC01	DC00

PACKAGE INFORMATION

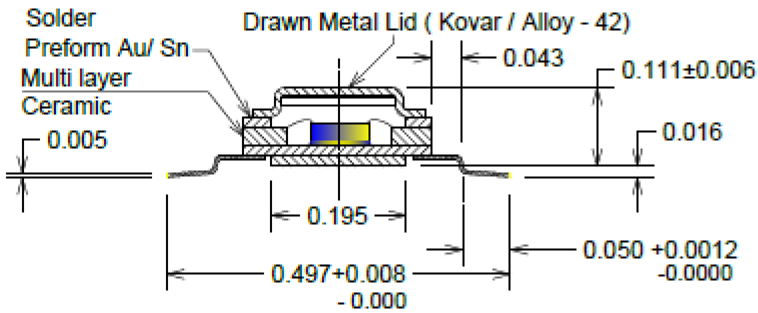
Package: 16 Pin CFP



TOP-VIEW



BOTTOM -VIEW



Section - A-A'

NOTE: ALL DIMENSIONS ARE IN INCH UNLESS UNTIL SPECIFIED