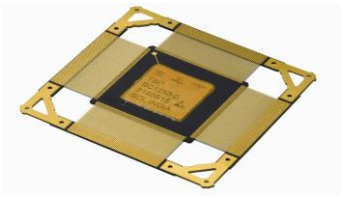
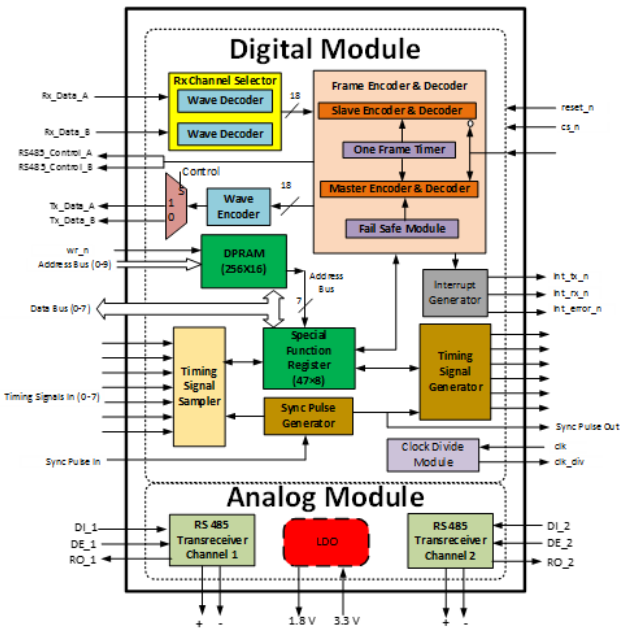
	TILE SERIAL PROTOCOL (TSP) ASIC	
SCL Part No.	**SCL1253-0**	

FEATURES:

- Microcontroller: DW8051
- Clock frequency:48 MHz
- Power Supply: 3.3V
- Memory:DPRAM : 256 X 16 bits
- Power Dissipation:< 1 W
- Temperature Range:-55°C to 125°C
- Number of I/O:62
- RS-485 Transceiver: 2Nos.
- On chip 1.8V LDO
- Package: CQFP-256
- Rad Hardened (TID) upto 300krad
- SEL/SEU Immune upto70 MeV-cm2/mg
- 180nm SCL CMOS standard logic process
- ESD Protection upto ±2KV HBM



Block Diagram

DESCRIPTION:

Tile Serial Protocol (TSP) is a custom protocol used for distributed control sub-systems of phased array radar. This protocol will be useful for communication of tele-command/telemetry data as well as communication of timing signals from central Payload Controller (PLC) to distributed T/R Controllers (TRC). The advantage of proposed protocol is huge reduction in tile harness, ease of debug and standardization of tile control management. TSP ASIC is a mixed signal ASIC consist of

Digital Modules:

- Sync Pulse Generator
- Timing Signal Sampler
- Timing Signal Generator
- Frame Encoder and Decoder
- One Frame Timer
- Fail Safe Module
- Wave Encoder & Decoder
- Received Channel Selector
- Special Function Register Module
- Interrupt Generation Module
- Clock Divide Module
- Memory Wrapper
- DPRM

Analog Modules:

- Two RS-485 Differential Transceiver
- LDO