2 CHANNELS SIMULTANEOUS SAMPLING 24 BIT Σ-Δ ADC (PSSC)

## FEATURES:

- **Two ΣΔ ADCs**
  - **24 Bits resolution**
  - **PGA from 1 to 128 in binary steps**
  - **Programmable Data Rate**
  - **0.003% INL**
  - **19 Bits ENOB (PGA = 1, OSR=2047)**
  - **On-chip Offset and Gain Calibrations**
  - **Over Range Detection**
  - **Data Format Selection**
  - **Fully Differential Reference Inputs**
- **Two Offset DACs (ODACs)**
  - **8 Bits resolution**
  - **Programmable up to half of full scale range at each PGA.**
- **Two Current DACs (IDACs)**
  - **8 Bits resolution**
  - **Programmable Full Scale Ranges of 0.5mA, 1mA and 2mA.**
- **Precision on-chip 2.5V Reference Accuracy: ±1%, Drift: ±36ppm/ºC**
- **On Chip Temperature Sensor**
- **Program and Flight Mode Operation**
- **SPI Compatible**
- **3.0V To 3.6V**

DESCRIPTION:

Pressure Sensor Signal Conditioner (PSSC) is developed for signal conditioning and digital conversion of the Pressure Sensor output data. It incorporates 2 Numbers of high resolution Sigma Delta (ΣΔ) ADCs, 2 Numbers of Eight Bits IDACs along with the calibration and over-range detection unit for each ΣΔ ADC. User can communicate with any of the ADC through SPI interface using one bit channel address. There are two modes of operation: Program mode and Flight mode. User can select any of the modes through a primary input pin.

Each ΣΔ ADC uses a second order modulator with a Programmable Gain Amplifier (PGA) and on-chip offset and gain calibration. It converts the analog input signal into a digital pulse train whose average duty cycle represents the digitized signal information. The pulse train is then processed by a digital sinc3 filter to produce a digital output. The output data rate of ΣΔ ADC is programmable.

Each 8-bits current DAC is available with three different ranges: 0.5mA, 1mA and 2mA. The device interface is SPI Compatible.
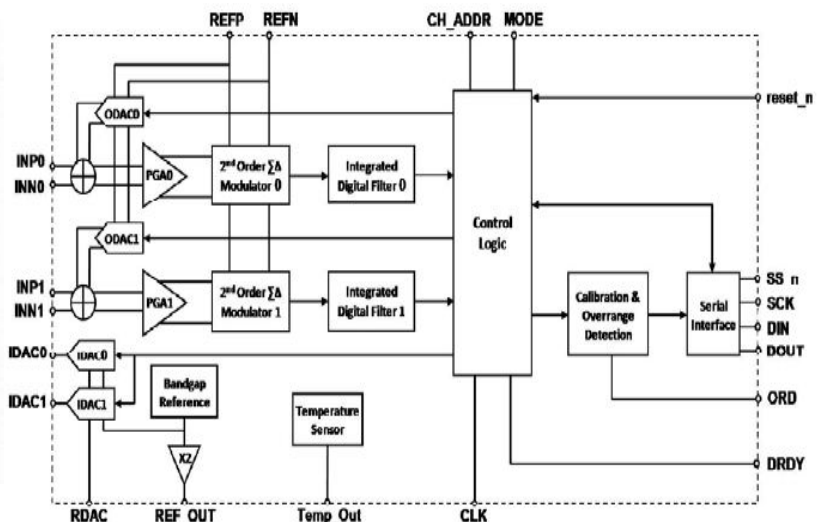
PIN CONFIGURATION:
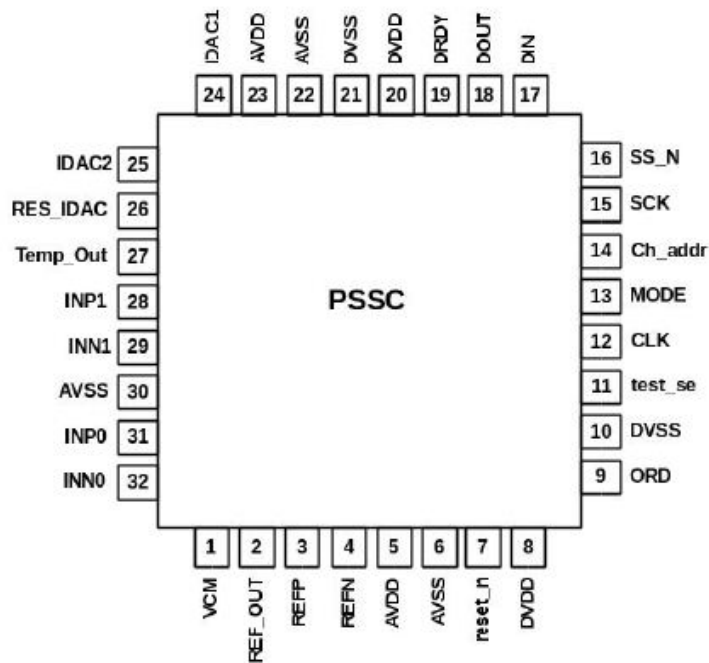
PIN DESCRIPTION:

Pin No.	Name	Analog/Digital	Description
1	VCM	Analog Output	Common Mode Output (VDD/2). User has to connect a decoupling capacitor of 0.1µF and 1 µF at this pin.
2	REF_OUT	Analog Output	Reference Output (2.5V). User has to connect a decoupling capacitor of 0.1µF and 1 µF at this pin.
3	REFP	Analog Input	Positive Reference Input Pin for ADC
4	REFN	Analog Input	Negative Reference Input Pin for ADC
5	AVDD	Analog Supply	3.3 V – Analog Supply
6	AVSS	Analog Ground	0 V – Analog Ground
7	reset_n	Digital Input: Active Low	Reset Signal: Reset the entire chip
8	DVDD	Digital Supply	3.3 V – Digital Supply
9	ORD	Digital Output	Over Range Detection
10	DVSS	Digital Ground	0 V – Digital Ground
11	test_se	Digital Input	Test Pin – Must to connected to DVSS
12	CLK	Digital Input	ADC Master Clock
13	MODE	Digital Input	Mode Selection to select Program mode or Flight mode
14	Ch_addr	Digital Input	Channel Address to select any of 2 ADCs
15	SCK	Digital Input	Serial Clock Input

16	SS_N	Digital Input: Active Low	Chip Select
17	DIN	Digital Input	Serial Data Input
18	DOUT	Digital Output	Serial Data Output
19	DRDY	Digital Input: Active Low	Data Ready Signal
20	DVDD	Digital Supply	3.3 V – Digital Supply
21	DVSS	Digital Ground	0 V – Digital Ground
22	AVSS	Analog Ground	0 V – Analog Ground
23	AVDD	Analog Supply	3.3 V – Analog Supply
24	IDAC1	Analog Output	Current DAC 1st Output
25	IDAC2	Analog Output	Current DAC 2nd Output
26	RES_IDAC	Analog	Current DAC Resistor
27	Temp_Out	Analog Output	Output of Temperature Sensor
28	INP1	Analog Input	ADC 1 Positive Input
29	INN1	Analog Input	ADC 1 Negative Input
30	AVSS	Analog Ground	0 V – Analog Ground
31	INP0	Analog Input	ADC 0 Positive Input
32	INN0	Analog Input	ADC 0 Negative Input

SPI TIMING SPECIFICATIONS DURING PROGRAM MODE:
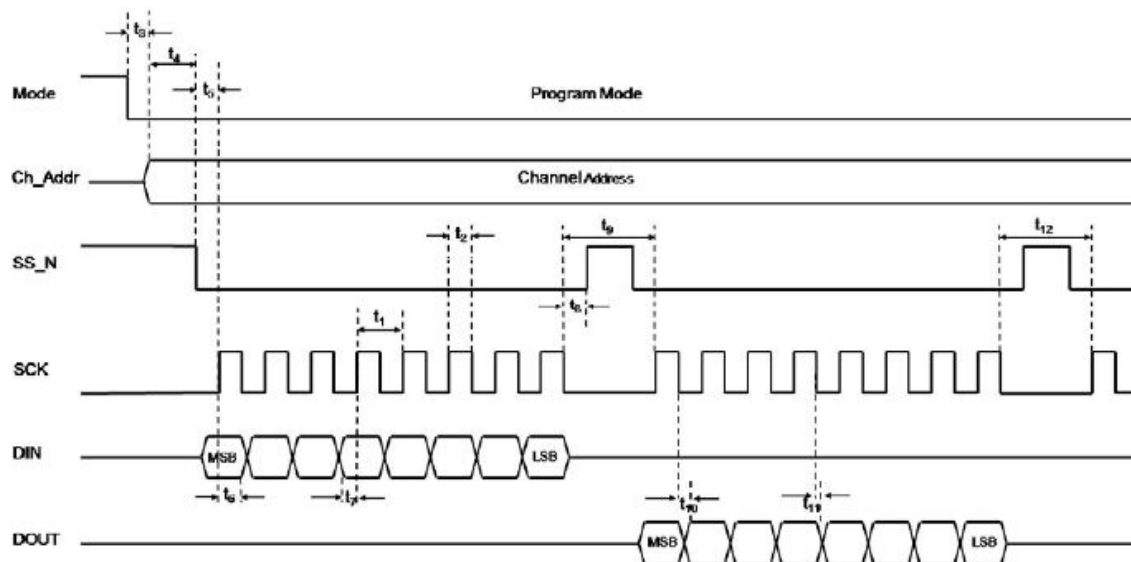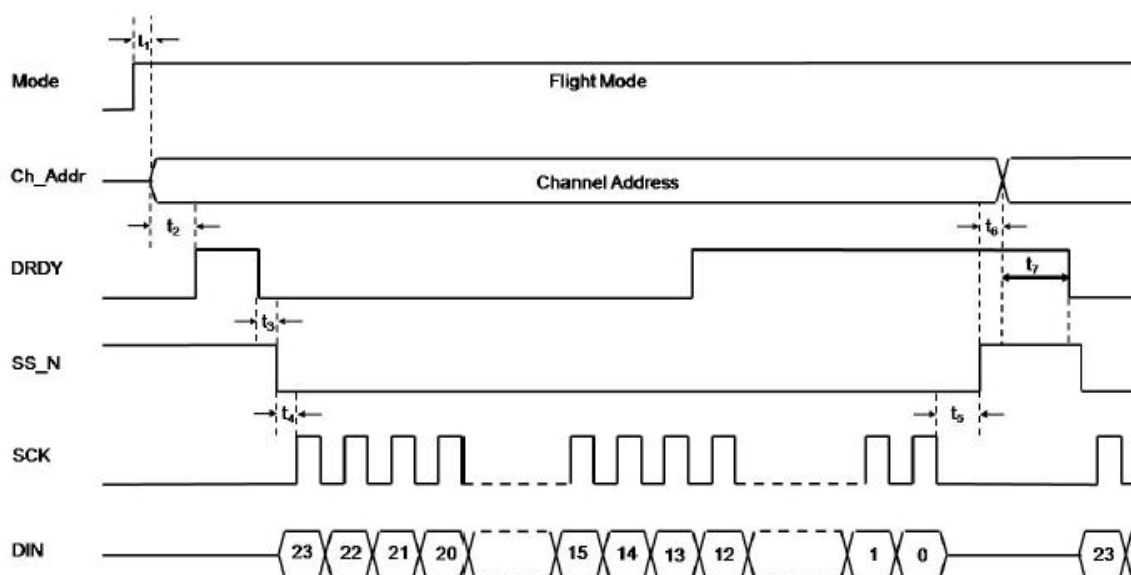

TIMING DIAGRAM

TIMING SPECIFICATION TABLE

SPEC	DESCRIPTION	MIN	MAX	UNIT
t_1	SCK period	4 cycle		t_{CLK} Period
t_2	SCK pulse width (High and Low)	2 cycle		t_{CLK} Period
t_3	Mode change to channel change	1 cycle		t_{CLK} Period
t_4	Channel change to SS_N low	4 cycle		t_{CLK} Period
t_5	SS_N low to first SCK edge	1 cycle		t_{CLK} Period
t_6	SCK rising edge to DIN valid (Hold time)	50		ns
t_7	DIN valid to SCLK rising edge (Setup time)	50		ns
t_8	Last SCK falling edge to SS_N HIGH	100		ns
t_9	Delay between last SCK edge of 1st byte transfer and first SCK edge for subsequent 2nd byte transfer : RREG, WREG Command	10		t_{CLK} Period
t_{10}	SCK falling edge to valid new DOUT		50^2	ns
t_{11}	SCK falling edge to DOUT, Hold time	0^3		ns
t_{12}	Final SCK edge of command until first edge SCK of next command	4		t_{CLK} Period

Notes: (1) DOUT goes immediately into tri-state whenever SS_N is high
     (2) DOUT pin output load should be less than 20pF
     (3) DOUT should be sampled externally on rising edge of SCK. DOUT will remain valid till next falling edge.

FLIGHT MODE TIMING SPECIFICATIONS:

TIMING DIAGRAM

TIMING SPECIFICATION TABLE

SPEC	DESCRIPTION	MIN	MAX	UNIT
t_1	Mode change to channel change	1		t_{CLK} Period
t_2	Channel Change to DRDY High (Note:1)	4		t_{CLK} Period
t_3	DRDY low to SS_N low (Note:2)		1	t_{CLK} Period
t_4	SS_N low to 1st edge of SCK	4		t_{CLK} Period
t_5	SCK low to SS_N High	5		t_{CLK} Period
t_6	SS_N High to channel change	1		t_{CLK} Period
t_7	Channel change to DRDY low	20	40	t_{CLK} Period

Notes: (1) In case the DRDY of the previous channel is turns low before changing the channel
 (2) Once DRDY goes low, user has to makes SS_N low within one master clock.
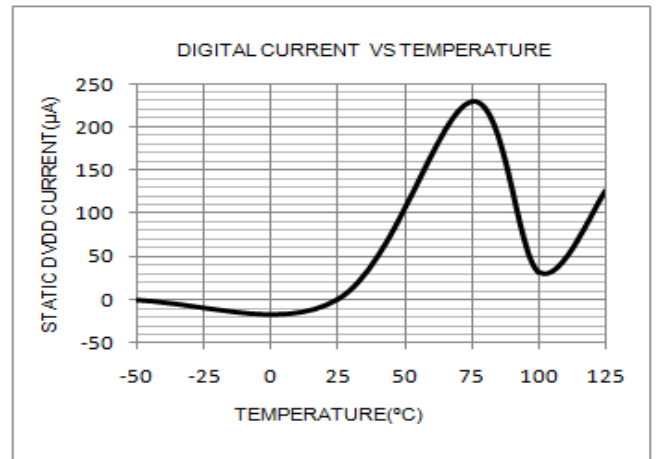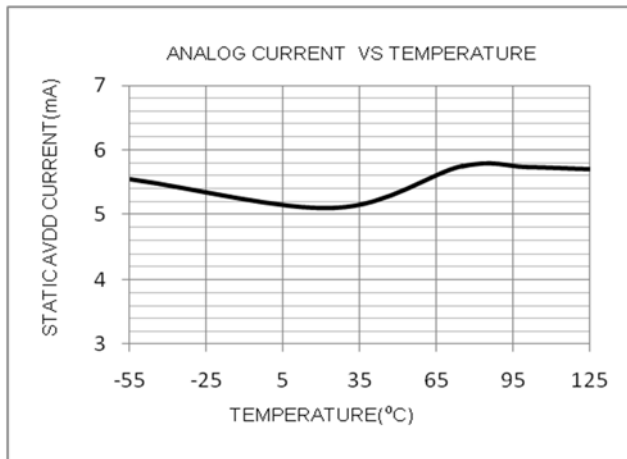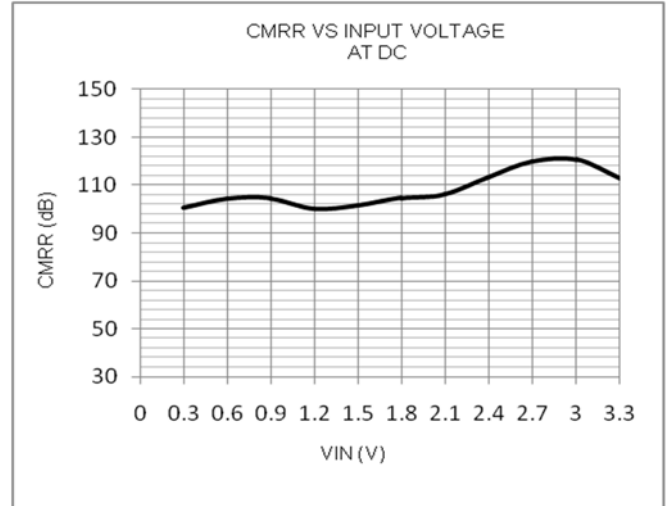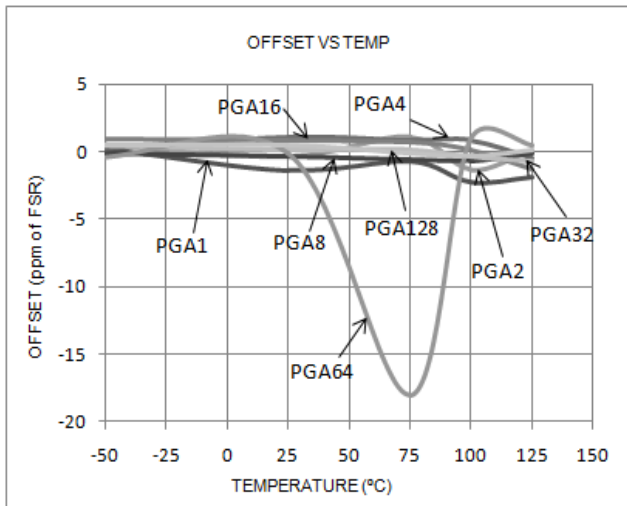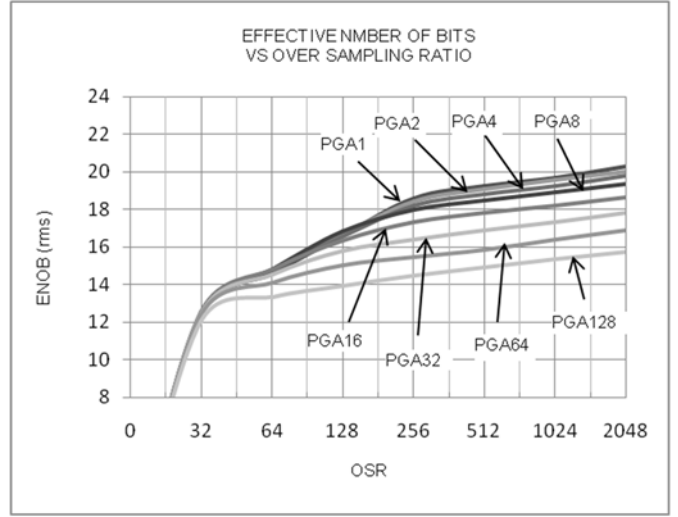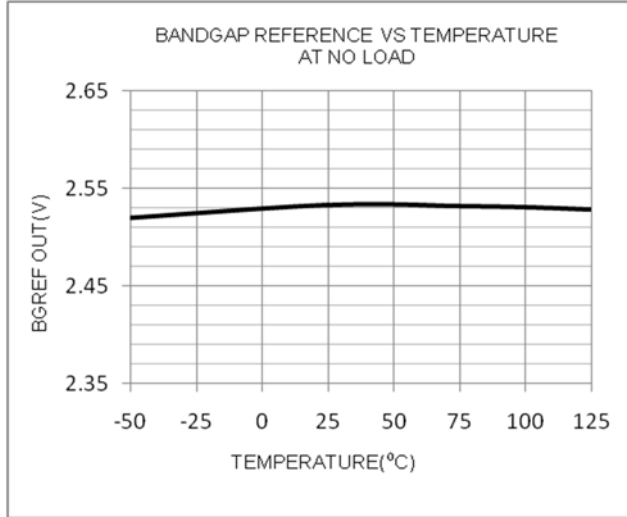
ELECTRICAL CHARACTERISTICS

All specifications are at AVDD, DVDD = +3.3V, Temp. = 25ºC, OSR=2047, f_{MOD} = 78.125 KHz, f_{CLK} = 2.5MHz, f_{Data} = 38.165 Hz, PGA=1, REFP =2.5V, REFN =0V, R_{DAC}=75K unless otherwise specified.

| PARAMETER | TESTS CONDITIONS | SC1247-0 | | | UNITS |
		MIN	TYP	MAX	
ADC					
Analog Input Range		0		AVDD	V
Full Scale Input Range	V_{INP}-V_{INN}	-V_{REF}/PGA		+V_{REF}/PGA	V
Programmable Gain Amplifier	User Selectable	1		128	
Input Current (Dynamic)*				25	µA
Input Capacitance*			32		pF
Bandwidth					
Sinc³ Filter*	-3dB		0.262*f_{Data}		Hz
Input Impedance*			100		KΩ
Resolution		24			Bits
Integral Non-Linearity	Best Fit Method			±0.003	% of FSR
Offset Error	After Calibration			8.2	ppm of FSR
Offset Drift	-55ºC to +125ºC			0.1	ppm/ºC
Gain Error	After Calibration			50	% of FSR
Gain Drift	-55ºC to +125ºC			0.13	ppm/ºC
Effective Number of Bits (ENOB)	Based on 100 samples			20	Bits
Common-Mode Rejection	At DC = 1.65		104		dB
Master Clock Rate	f_{CLK}			20	MHz
ON CHIP VOLTAGE REFERENCE					
Output Voltage	Load Current = 1µA	2.52	2.53	2.54	V
Load Regulation	Full Load =2.5mA	-1		1	%
Drift	-55ºC to +125ºC			36	ppm/ºC
Start up Time*				240	µS
VOLTAGE REFERENCE INPUT					
External Reference	(REFP)-(REFN)			2.5	V
POWER SUPPLY REQUIREMENT					
Supply Voltage	AVDD	3.0	3.3	3.6	V
	DVDD	1.62	1.8	1.98	V
Analog Current			5.5	8	mA
Digital Current	Static		0.24	2	mA
Digital Current	Dynamic @ F_{CLK}=10MHz		2.1	5	mA
Temperature Sensor					
Output Voltage	Temp_Out	555	650	747	mV
IDAC					
Full Scale Output Current	R_{DAC} =75K, Range1		0.5		mA
	R_{DAC} =75K, Range2		1.0		mA
	R_{DAC} =75K, Range3		2.0		mA
Monotonocity		8			Bits
Nonlinearity				1	%FSR
ODAC					
Full Scale Output Voltage	At Code 127		1.25		V
	At Code 255		-1.25		V
TEMPERATURE RANGE					
Operating		-55		125	ºC

* Simulated Result

ELECTRICAL CHARACTERISTICS

All specifications are at AVDD, DVDD = +3.3V, Temp. = 25ºC, OSR=2047, f_{MOD} = 78.125 KHz, f_{CLK} = 2.5MHz, f_{Data} = 38.165 Hz, PGA=1, REFP =2.5V, REFN =0V, R_{DAC}=75K unless otherwise specified.

DIGITAL CHARACTERISTICS

DVDD= 3.0V to 3.6V

PARAMETER	TESTS CONDITIONS	SC1247-0			UNITS
		MIN	TYP	MAX	
Logic Family			CMOS		
Logic Level: V_{IH}	DVDD = 3.3V	2		0.3 + DVDD	V
V_{IL}	DVDD = 3.3V	DVSS		0.8	V
V_{OH}	I_{OH}=-8Ma, DVDD = 3.3V	2.4			V
V_{OL}	I_{OL}=8mA, DVDD = 3.3V			0.4	V
Input Leakage: I_{IH}	V_I=DVDD			1	µA
I_{IL}	V_I=DVSS	-1			µA

ABSOLUTE MAXIMUM RATING

PARAMETER	SC1247-0		UNITS
	MIN	MAX	
AVDD to AVSS	-0.3	4.3	V
DVDD to DVSS	-0.3	4.3	V
INP, INN	-0.3	AVDD+0.3	V
Digital Input Voltage to DGND	-0.3	DVDDO+0.3	V
Digital Output Voltage to DVSS	-0.3	DVDDO+0.3	V
Maximum Junction Temperature		125	°C

OVERVIEW

PROGRAMMABLE GAIN AMPLIFIER

The Programmable Gain Amplifier (PGA) can be set to gains of 1, 2, 4, 8, 16, 32, 64, or 128. Adjusting the internal gain of a sigma delta modulator is a technique, which can be used to get an appropriate LSB size for the transducers application. It will improve the resolution of the ADC. The PGA is combined with the $\Sigma\Delta$ modulator.

$\Sigma\Delta$ MODULATOR

A second order single loop sigma delta modulator is used in the PSSC. The sigma delta modulator converts the input signal into a digital pulse train whose average duty cycle represents the digitized signal information. The integrators used in the modulator are switched capacitor based.

There are two different $\Sigma\Delta$ Modulator units in PSSC. Each of the modulator units can be programmed independently.

The modulator runs at clock frequency f_{MOD} that can be adjusted by setting the appropriate value of PRE1: PRE0 of CR2 control register as shown in the following table:

PRE1:PRE0	f_{MOD}
00	$f_{CLK}/32$
01	$f_{CLK}/64$
10	$f_{CLK}/128$
11	$f_{CLK}/256$

Where f_{CLK} is external clock frequency

The modulator is designed to work at a maximum sampling frequency of *625 KHz.* Both the modulator units run at the same modulator frequency. It is recommended that user must set the same PRE1:PRE0 value in both the modulator cores. If different values of PRE1:PRE0 are used then, the last core PRE1:PRE0 values will be used for both the modulator cores.

INTEGRATED DIGITAL FILTER

Each of $\Sigma\Delta$ Modulator is followed by an independent integrated digital filter unit. It comprises of sinc[3] filter and internal registers. The decimation ratio of each unit of filter module can be programmed independently.

The on-chip digital filter processes the single bit data stream coming from the corresponding modulator unit using a sinc[3] filter. The sinc filters are conceptually simple, efficient and flexible, especially where variable resolution and data rates are required. The output data rate of digital filter is given as:

$$\text{Data Rate} = f_{MOD} / DR$$

The Decimation Ratio (DR) of filter can vary from 20 to 2047 and its value is represented by 8 Bits of DECIM Register and first 3 LSBs of CR2 Register. Although, DR can have any of the value between 20 and 2047 but there are fixed numbers of decimation ratios which are implemented internally.

Both the ADC cores have its own registers bank which comprise of CR1, CR2, DECIM, ODAC, IDAC, OCR and FSR registers. The user can read/write these registers during program mode and any of the ADC core can be selected by applying appropriate channel address at the CH_ADDR pin.

IDAC

There are two numbers of 8 bit IDACs. Both the IDACs can be programmed independently. The output current of a particular IDAC pair is set with RDAC, the range select bits in CR1 register of CORE0 and 8 Bit digital value in IDAC register. The output current of IDAC is given as:

$$IDAC\ Current = \frac{V_{REF\_OUT}}{8*R_{DAC}}(2^{RANGE-1})(IDAC\ CODE)$$

RDAC resistor is an external register to be connected at the RDAC pin. It is common to both the IDACs. V_{REF_OUT} is the output voltage of on chip bandgap reference. Range is the decimal equivalent of range select bits in CR1 register. IDAC code is decimal equivalent of 8 bits binary value in IDAC register. In case, IDAC is not used then set the value of range in CR1of CORE0 as 00. The reference of the IDAC is internally shorted the internal bandgap reference voltage of 1.22V.

ODAC

The input to the PGA can be shifted by half the full-scale range of the PGA by using the ODAC register. The ODAC (Offset DAC) register is an 8-bit value; the MSB is the sign and the seven LSBs provide the magnitude and the offset.

REFERENCES

PSSC has a differential voltage reference input. The ADC measure the input signal against the differential voltage V_{REF}, Where V_{REF} is the difference between positive reference input (REFP) and negative reference input (REFN). An external bandgap reference can be between REFP and REFN primary input pins of ADC.

An internal bandgap reference of 2.5V is also provided. User can select between the internal and external bandgap reference using the control pin REF_CON. When REF_CON is 0, the internal positive reference of ADC will be sorted REF_OUT and internal negative reference will be sorted to AVSS. When REF_CON is 1, the internal reference of ADC will be sorted REFP and internal negative reference will be sorted to REFN.

CONTROL LOGIC

Any of the 2 ADC core for communication can be selected by applying appropriate one bit channel address on input primary pin CH_ADDR. All the operations like instruction decoding, command execution, SPI control, DRDY generation, calibration & over range management, etc are governed by this unit.

PSSC has two modes of operation i.e. flight mode and program mode. The chip can be made to operate in any mode based on the logic high/low of Mode Pin.

Program Mode: During this mode (Mode Pin at Logic Low) user can program the control registers for different settings like decimation ratio, PGA, pre-scaler value, ODAC register, IDAC register and self/system calibration registers. All the commands will be recognized only in Program Mode.

Steps to be follow in program mode.

1. Set the mode of device in Program mode.
2. Set the address lines corresponding to a particular ADC core.
3. Enable the SS_N signal.
4. Set the control registers and perform the calibration.
5. Follow steps 2 and 4 for both the ADC cores.

Flight Mode: During this mode, data from selected ADC core sends out from the device. Whenever Master wants to fetch data of a particular ADC core; place the address of ADC core on the address lines, CH_ADDR and then asserts chip select enable signal. Thereafter, three dummy bytes are written on SPI bus and 24 bit data is received through DOUT. Valid data from device will be available at the falling edge of DRDY. During this mode no commands will be recognized by the device.

Steps to be follow in flight mode.
1. Set the mode of the device in Flight mode
2. Set the address lines corresponding to a particular ADC core.
3. Wait for negative edge of DRDY signal.
4. Enable the SS_N signal.
5. Read the data of selected ADC through DOUT.
6. Disable the SS_N Signal.
7. To read data from other ADC core, repeat steps 2 to 6.

SERIAL INTERFACE

The serial interface is standard four-wire SPI compatible (DIN, DOUT, SCK and SS_N). Any of the two ADC cores can communicate serially through single SPI. The user has to select a particular ADC core for data transaction by placing a one bit address on address line CH_ADDR.

SS_N (Serial Interface Enable): The SS_N input must be externally asserted before a master device can exchange data with the ADC. SS_N must be Low for the duration of the transaction. DOUT pin will become tri-state when SS_N pin goes high. When SS_N is Low, the output data register will never be updated even if new data comes. After data read operation, it should be made high.

SCK (Serial clock): SCK function as a clock for serial communication. The device will sample serial data on positive edge of SCK. Data from PSSC will be launched on negative edge of SCK.

DIN (Data input): DIN is the serial data input port. It is internally sampled at positive edge of SCLK by SPI.

DOUT (Data output): DOUT is the serial data output port. It is internally launched by SPI at negative edge of SCK. DOUT immediately goes into tri-state when SS_N is high.

DRDY (DATA READY)

The DRDY pin is used as a status signal to indicate when new digital code is ready to be read from the selected ADC core of PSSC. DRDY goes low when new data is available. It becomes high in the mid of second byte read during read operation from the data register in flight mode. In case, in response to the DRDY assertion no read operation is performed, DRDY will remain low till next filter clock cycle or till next channel change. It is mandatory for the user to read at least two bytes, otherwise the DRDY will remains low till next filter clock or channel change.

OFFSET AND GAIN CALIBRATION

Both the self offset error and complete system offset error in selected ADC

core can be reduced with offset calibration. This is handled with two offset commands SEFOCAL and SYSOCAL. There is also a gain calibration module to compensate self gain and system gain error with SELFGAIN and SYSGAIN command respectively. ***Please refer calibration procedure section.*** Each calibration process takes five conversion cycles to complete. Therefore it takes 10 conversion cycles to complete both an offset and gain calibration. Calibration must be performed after system reset, a change in decimation ratio or a change of the PGA.

Calibration commands will only update the Offset Calibration Register (OCR) with appropriate offset value. However, to enable the offset correction, OCEN bit of CR1 control register has to be set separately. Similarly to apply gain correction, GCALEN bit has to be set.

SELFGAIN command is only possible at PGA1.

OVER-LOAD DETECTION MODULE

Where digital code without calibration is such that it cannot be corrected after calibration then Over-Load detection module detects over-load and clip digital output appropriately to $7FFFFF_H$ and 800000_H.

Status of over-load detection module is available at ORD Pin. This pin will become high in case of over-load condition.

Over-load detection can be disabled by setting OLDD flag of CR2 control register. By default it is enabled.

OVER-RANGE DETECTION MODULE

If digital code after gain and offset calibration is out of the acceptable code range then digital over-range module detects over-range and clip digital output appropriately to $7FFFFF_H$ and 800000_H. To ensure the proper functioning of the Over Range Detection Module, following constraint on OCR & FSR register value must be followed:

Maximum value of OCR register should not exceed $3FFFFF_H$ for negative offset correction and $C00000_H$ for positive offset correction.

FSR value must be positive.

When device is in the over-range condition, the ORD pin will become high.

Over-range detection can be disabled by setting ORDD flag of CR2 control register. By default it is enabled.

ORDD bit also affects digital output range. Setting ORDD bit will half the digital output range as shown below.

ORDD BIT	ANALOG INPUT	DIGITAL OUTPUT CODE
0	$+V_{REF}$	$7FFFFF_H$
	0	000000_H
	$-V_{REF}$	800000_H
1	$+V_{REF}$	$3FFFFF_H$
	0	000000_H
	$-V_{REF}$	$C00000_H$

CALIBRATION PROCEDURE

The Multi-Core RDAS has two commands namely SEFOCAL and SYSOCAL to compensate offset errors. Internal calibration of device is called self calibration. By executing SELFOCAL command, the device shorts the ADC input and stores the offset value into OCR register in 2's complement form.

For system calibration, the user must apply appropriate 'zero signal' to the selected input channel and then execute SYSOCAL command. In this case ADC computes the offset value based on the available differential input signal and stores it into OCR register in 2's complement form. The System gain calibration requires appositive "full scale differential input signal. On executing system gain command, ADC computes a value to nullify gain error. At the completion of calibration, the DRDY signal will go Low to indicate that calibration is complete and valid data is available.

Calibration commands will only update the Offset Calibration Register (OCR) with appropriate offset value. However, to enable the offset correction, OCEN bit of CR1 control register has to be set separately. Similarly to enable gain calibration set GCALEN bit of CR1 register. Each calibration process takes five conversion cycles to complete. DRDY will be asserted to indicate completion of the calibration process.
Apart from above commands, OSR and FSR can be accessed externally through RREG (Read Register) and WREG (Write Register) commands. This will provide flexibility to manually set the OCR and FSR.

COMMAND DEFINITIONS

The commands listed below control the operation of PSSC Device. Some commands are stand-alone commands (e.g. SELFOCAL) while others require additional bytes (e.g., WREG requires command and the data bytes).

Operands:
rrrr represents the register address.
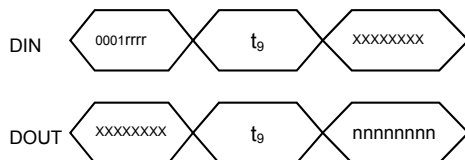
nnnnnnnn represents the data.

xxxx: these bits will be ignored while instruction decoding.

COMMANDS	DESCRIPTION	COMMAND BYTE	2ND COMMAND BYTE
RREG	Read from Register rrrr	0100 rrrr (4r$_H$)	-N.A.-
WREG	Write to Register rrrr	0101 rrrr (5r$_H$)	nnnnnnnn
SELFOCAL	Self Offset Calibration	0110 xxxx (6x$_H$)	-N.A.-
SYSOCAL	System Offset Calibration	0111 xxxx (7x$_H$)	-N.A.-
SELFGAIN	Self Gain Calibration	1000 xxxx (8x$_H$)	-N.A.-
SYSGAIN	System Gain Calibration	1001 xxxx (9x$_H$)	-N.A.-

RREG (READ REGISTER)

RREG (Read Register) command reads content of the specified register. The address of the register to be read is specified in the LSB nibble of the instruction.

Operands: r, n
Bytes: 2
Encoding: 0100 rrrr

DIN: 0001rrrr t$_9$ xxxxxxxx

DOUT: xxxxxxxx t$_9$ nnnnnnnn

WREG (WRITE REGISTER)

WREG (Write Register) command writes the data to specified register. The address of the register to be written is specified in the LSB nibble of the first byte. Second byte represents the data to be written.

Operands: r, n
Bytes: 2
Encoding: 0101rrrr nnnnnnnn

DIN: 0001rrrr t$_9$ nnnnnnnn
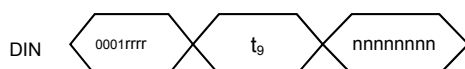
SELFOCAL (SELF OFFSET CALIBRATION)

This command performs Self Offset Calibration. At the end of the calibration process, offset value will be stored in 24-bit internal Offset Calibration Register (OCR) is in 2's complement format. DRDY will be asserted low to indicate completion of the command.

Operands: x
Bytes: 1
Encoding: 0110 xxxx

DIN: 0110XXXX
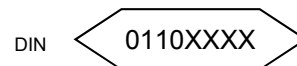
SYSOCAL (SYSTEM OFFSET CALIBRATION)

With this command ADC computes the offset value based on the available differential input signal on ADC input to nullify offset in the system. The offset value will be stored in 24-bit internal Offset Calibration Register (OCR) in 2's complement format. DRDY will be asserted low to indicate completion of the command.

Operands: x
Bytes: 1
Encoding: 0111xxxx

DIN ⟨ 0111XXXX ⟩

DIN ⟨ 1001XXXX ⟩

SELFGIAN (SELF GIAN CALIBRATION)

This command performs Self Gain Calibration. At the end of the calibration process, gain calibration coefficient value will be stored in 24-bit internal FSR Register. DRDY will be asserted low to indicate completion of the command.

Operands: x
Bytes: 1
Encoding: 1000 xxxx

DIN ⟨ 1000XXXX ⟩

SYSGAIN (SYSTEM GAIN CALIBRATION)

With this command ADC computes the gain value based on the available differential input signal on ADC input to nullify gain error in the system. The gain value will be stored in 24-bit internal FSR Register. DRDY will be asserted low to indicate completion of the command.

Operands: x
Bytes: 1
Encoding: 1001xxxx

CONTROL / STATUS REGISTERS

The operation of the device is set up through following control / status registers.

Address	Register	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0$_H$	DIGITAL_CODE_B 1 (R)	DC23	DC22	DC21	DC20	DC19	DC18	DC17	DC16
1$_H$	DIGITAL_CODE_B 2 (R)	DC15	DC14	DC13	DC12	DC11	DC10	DC9	DC8
2$_H$	DIGITAL_CODE_B 3 (R)	DC7	DC6	DC5	DC4	DC3	DC2	DC1	DC0
3$_H$	CR1 (RW)	PGA2	PGA1	PGA0	OCEN	GCALEN	REFCON	IDACR1	IDACR0
4$_H$	CR2 (RW)	Data Format	OLDD	ORDD	PRE1	PRE0	OSR10	OSR9	OSR8
5$_H$	DECIM_reg (RW)	OSR7	OSR6	OSR5	OSR4	OSR3	OSR2	OSR1	OSR0
7$_H$	OCR1 (RW)	OCR07	OCR06	OCR05	OCR04	OCR03	OCR02	OCR01	OCR00
8$_H$	OCR2 (RW)	OCR15	OCR14	OCR13	OCR12	OCR11	OCR10	OCR09	OCR08
9$_H$	OCR3 (RW)	OCR23	OCR22	OCR21	OCR20	OCR19	OCR18	OCR17	OCR16
A$_H$	FSR1 (RW)	FSR07	FSR06	FSR05	FSR04	FSR03	FSR02	FSR01	FSR00
B$_H$	FSR2 (RW)	FSR15	FSR14	FSR13	FSR12	FSR11	FSR10	FSR09	FSR08
C$_H$	FSR3 (RW)	FSR23	FSR22	FSR21	FSR20	FSR19	FSR18	FSR17	FSR16
D$_H$	IDAC (RW)	IDAC7	IDAC6	IDAC5	IDAC4	IDAC3	IDAC2	IDAC1	IDAC0
E$_H$	ODAC (RW)	SIGN	ODAC6	ODAC5	ODAC4	ODAC3	ODAC2	ODAC1	ODAC0

R: Read only registers
RW: Read/Write registers
Note: At reset all registers are initialized to 00$_H$ on reset.

CR1 (ADD: 03$_H$) CONTROL REGISTER-1

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
PGA2	PGA1	PGA0	OCEN	GCALEN	REFCON	IDACR1	IDACR0

BIT 7-5:PGA2:PGA1:PGA0: Programmable
    Gain Amplifier selection
    000 = 1   100 = 16
    001 = 2   101 = 32
    010 = 4   110 = 64
    011 = 8   111 = 128

Bit4: OCEN: Offset Calibration Enable bit
OCE = 1: Enable offset calibration
OCE = 0: Disable offset calibration

Bit3: GCALEN: Gain calibration Enable bit
GCALEN = 1: Enable Gain calibration
GCALEN = 0: Disable Gain calibration

Bit2: REFCON: Reference Control Bit
REFCON = 0: Internal positive reference will be sorted to REF_OUT and internal negative reference will be sorted to AVSS.

REFCON = 1: Internal positive reference will be sorted to REFP and internal negative reference will be sorted to REFN.

Bit1-0: IDACR1: IDACR0: Range Selection for current in IDAC
00 = off   10 = 1 mA
01 = 0.5 mA   11 = 2 Ma

CR2 (ADD: 04$_H$) CONTROL REGISTER- 2

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Data Format	OLDD	ORDD	PRE1	PRE0	OSR10	OSR9	OSR8

Bit7: Data Format of the output code
1 = Offset Binary output data
0 = 2's complement output data

Bit6: OLDD: Analog over range detection
0 = Enable over-load detection.
1 = Disable over-load detection.

Bit5: ORDD: Digital over range detection
0 = Enable over-range detection.
1 = Disable over-range detection.

Bit4-3: PRE1:PRE0: Prescaler bits

PRE1:PRE0	f_{MOD}
00	f_{CLK} /32
01	f_{CLK} /64
10	f_{CLK} /128
11	f_{CLK} /256

Bit2-0:OSR10:OSR9: OSR8 control bits.
Three MSBs of 11bits of decimation ratio
Note: Any update in CR1 or CR2 control register will reset modulator and digital filter. DRDY will also go high.

DECIM (ADD: 05H) CONTROL REGISTER-3

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
OSR7	OSR6	OSR5	OSR4	OSR3	OSR2	OSR1	OSR0

BIT 7-0: OSR7:OSR0
These bits are 8 LSB bits of 11 bit decimation ratio

OCR1 (ADD: 07H) OFFSET CALIBRATION REGISTER-1
(Least Significant Byte)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
OCR07	OCR06	OCR05	OCR04	OCR03	OCR02	OCR01	OCR00

OCR2 (ADD: 08H) OFFSET CALIBRATION REGISTER-2
(Middle Byte)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
OCR15	OCR14	OCR13	OCR12	OCR11	OCR10	OCR09	OCR08

OCR3 (ADD: 09H) OFFSET CALIBRATION REGISTER-3
(Most Significant Byte)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
OCR23	OCR22	OCR21	OCR20	OCR19	OCR18	OCR17	OCR16

FSR1 (ADD: 0AH) FULL SCAEE REGISTER-1
(Least Significant Byte)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FSR07	FSR06	FSR05	FSR04	FSR03	FSR02	FSR01	FSR00

FSR2 (ADD: 0BH) FULL SCAEE REGISTER-2
(Middle Byte)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FSR15	FSR14	FSR13	FSR12	FSR11	FSR10	FSR09	FSR08

FSR3 (ADD: 0CH) FULL SCAEE REGISTER-3
(Most Significant Byte)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FSR23	FSR22	FSR21	FSR20	FSR19	FSR18	FSR17	FSR16

IDAC (ADD: 0DH) CURRENT DAC

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
IDAC7	IDAC6	IDAC5	IDAC4	IDAC3	IDAC2	IDAC1	IDAC0

The DAC code bits set the output of DAC from 0 to full scale. The value of the full-scale current is set by this Byte, V_{REF}, RDAC and the IDAC range bits in the CR1 register of Core0.

ODAC (ADD: 0EH) Offset DAC

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
SIGN	ODAC6	ODAC5	ODAC4	ODAC3	ODAC2	ODAC1	ODAC0

BIT7: Offset Sign
    0: Positive
    1: Negative

BIT6 – 0: Code

$$Offset = \frac{VREF}{2*PGA}\left(\frac{Code}{127}\right)$$

Note: the offset DAC register must be written after the calibration otherwise the effects of the ODAC setting will be reflected in the calibration.

DIGITAL_CODE_B1 (ADD: 00H) DIGITAL OUTPUT CODE
(MOST SIGNIFICANT BYTE)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
DC23	DC22	DC21	DC20	DC19	DC18	DC17	DC16

DIGITAL_CODE_B2 (ADD: 01$_H$) DIGITAL OUTPUT CODE
(MIDDLE BYTE)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
DC15	DC14	DC13	DC12	DC11	DC10	DC09	DC08

DIGITAL_CODE_B3 (ADD: 02$_H$) DIGITAL OUTPUT CODE
(LEAST SIGNIFICANT BYTE)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
DC07	DC06	DC05	DC04	DC03	DC02	DC01	DC00