SC1239-0

PRELIMINARY DATASHEET

Version 1.0 Jan 2021

8 Channels Simultaneous Sampling 24 Bit Sigma-Delta ADC (OC HF RDAS)

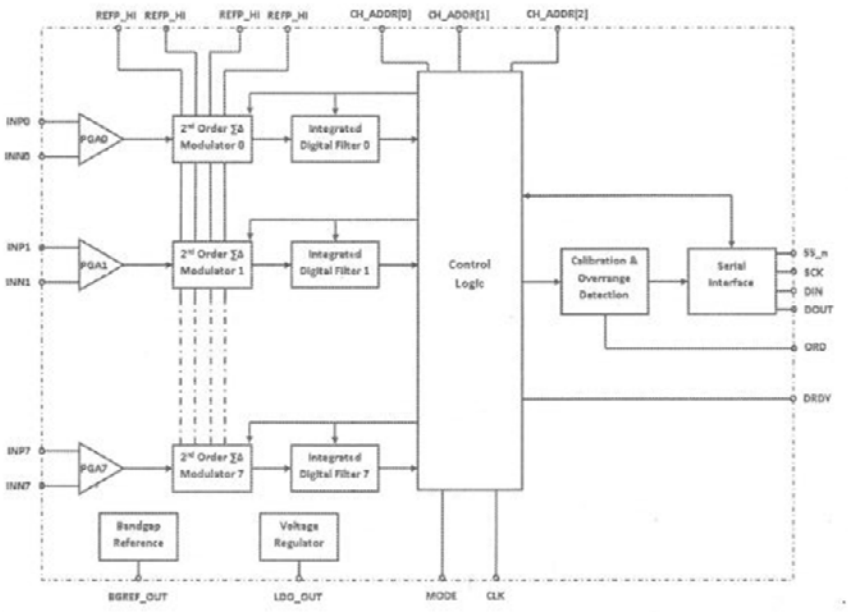
FEATURES:

- **Eight ΣΔ ADCs**
  - **24 Bits resolution**
  - **PGA from 1 to 128 (Binary Steps)**
  - **Programmable Data Rate**
  - **0.05% INL**
  - **19 Bits ENOB (PGA = 1, OSR=2047)**
  - **On-chip Offset and Gain Calibrations**
  - **Over Range Detection**
  - **Data Format Selection**
- **Precision on-chip 1.22V Reference Accuracy: ±1%, Drift: ±31ppm/ºC**
- **On Chip 1.8V Voltage Regulator**
- **Program and Flight Mode Operation**
- **SPI Compatible**
- **3.0V TO 3.6V**

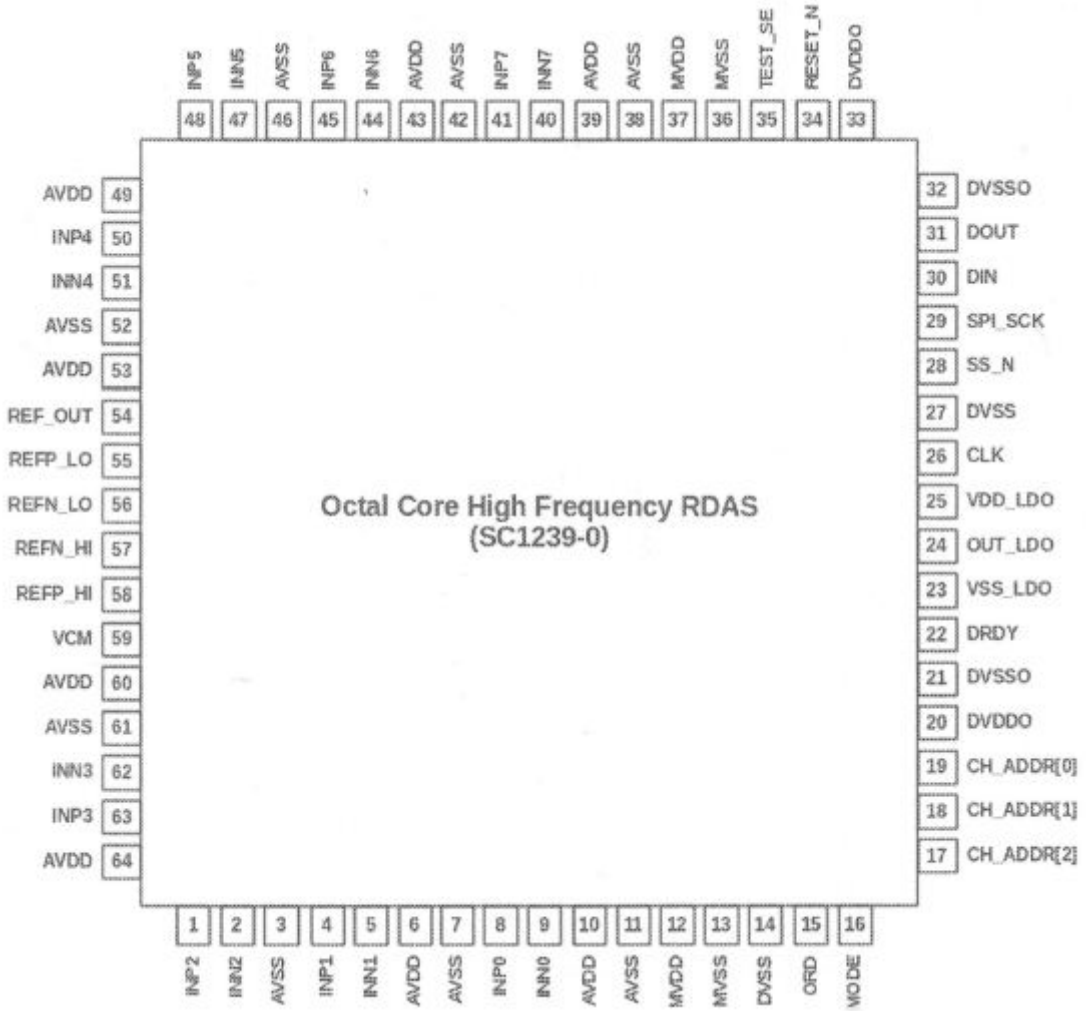
DESCRIPTION:

Octal-Core High frequency Reconfigurable Data Acquisition System (OC HF RDAS) is a fully integrated data acquisition system. It incorporates 8 high resolution Sigma Delta (ΣΔ) ADCs along with the calibration and over-range detection unit for each ΣΔ ADC. User can communicate with any of the ADC through SPI interface using three bits channel address. There are two modes of operation: Program mode and Flight mode. User can select any of the modes through a primary input pin.

Each ΣΔ ADC uses a second order modulator with a Programmable Gain Amplifier (PGA). The ΣΔ modulator converts the analog input signal into a digital pulse train whose average duty cycle represents the digitized signal information. The pulse train is then processed by a digital sinc^5 filter to produce a digital output. The output data rate of ΣΔ ADC is programmable.



PIN CONFIGURATION:

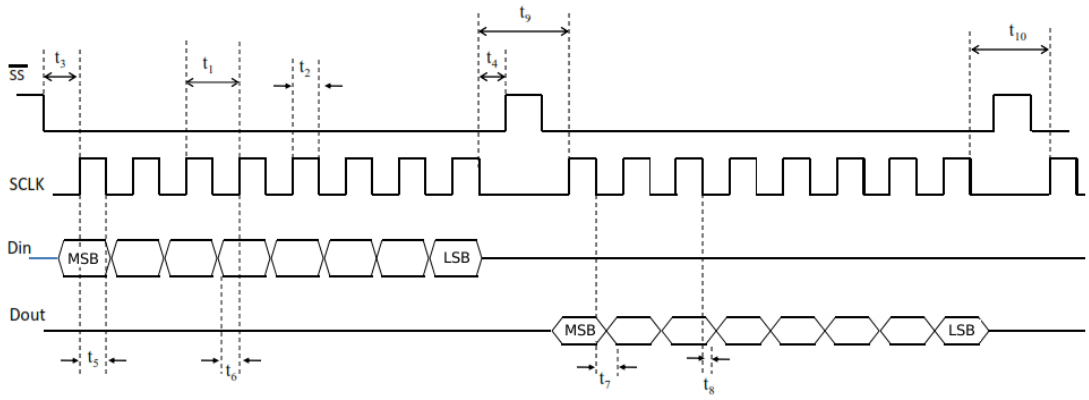


PIN DESCRIPTIONS:

PIN NO.	NAME	DESCRIPTION
1	INP2	Positive Analog Input 2
2	INN2	Negative Analog Input 2
3	AVSS	Analog Ground
4	INP1	Positive Analog Input 1
5	INN1	Negative Analog Input 1
6	AVDD	Analog Power Supply (3.3 V)
7	AVSS	Analog Ground
8	INP0	Positive Analog Input 0
9	INN0	Negative Analog Input 0
10	AVDD	Analog Power Supply (3.3 V)
11	AVSS	Analog Ground
12	MVDD	Mixed Signal Supply (3.3V, can be connected to AVDD)
13	MVSS	Mixed Signal Ground (can be connected to AVSS)
14	DVSSO	Digital Ground

15	ORD	Over Range Detection
16	MODE	Mode Selection
17	CH_ADDR[2]	Channel Address bit 2
18	CH_ADDR[1]	Channel Address bit 1
19	CH_ADDR[0]	Channel Address bit 0
20	DVDDO	Digital Power Supply (3.3 V)
21	DVSSO	Digital Ground
22	DRDY	Data Ready, Active Low
23	VSS_LDO	LDO Ground (can be connected to DVSS)
24	OUT_LDO	Voltage Regulator Output(1.8 V)
25	DVDD_LDO	Digital I/O Power Supply (3.3 V, can be connected to DVDD)
26	CLK	Master Clock
27	DVSSO	Digital Ground
28	SS_N	Serial Interface Enable, Active Low
29	SPI_SCK	Serial Clock
30	DIN	Serial Data Input
31	DOUT	Serial Data Output
32	DVSSO	Digital Ground
33	DVDDO	Digital Power Supply (3.3 V)
34	reset_n	Reset, Active Low
35	test_se	Scan Enable This pin is used for ATPG testing In normal operation, it will be connected to DVSS
36	MVSS	Mixed Signal Ground (can be connected to AVSS)
37	MVDD	Mixed Signal Supply (3.3V, can be connected to AVDD)
38	AVSS	Analog Ground
39	AVDD	Analog Power Supply (3.3 V)
40	INN7	Negative Analog Input 7
41	INP7	Positive Analog Input 7
42	AVSS	Analog Ground
43	AVDD	Analog Power Supply (3.3 V)
44	INN6	Negative Analog Input 6
45	INP6	Positive Analog Input 6
46	AVSS	Analog Ground
47	INN5	Negative Analog Input 5
48	INP5	Positive Analog Input 5
49	AVDD	Analog Power Supply (3.3 V)
50	INP4	Positive Analog Input 4
51	INN4	Negative Analog Input 4
52	AVSS	Analog Ground
53	AVDD	Analog Power Supply (3.3 V)
54	REF_OUT	Output of Band Gap Reference
55	REFP_LO	Positive Differential Reference Input Low
56	REFN_LO	Negative Differential Reference Input Low
57	REFN_HI	Negative Differential Reference Input High
58	REFP_HI	Positive Differential Reference Input High
59	VCM	Common Mode Voltage
60	AVDD	Analog Power Supply (3.3 V)
61	AVSS	Analog Ground
62	INN3	Negative Analog Input 3
63	INP3	Positive Analog Input 3
64	AVDD	Analog Power Supply (3.3 V)

SPI TIMING SPECIFICATIONS:



TIMING DIAGRAM

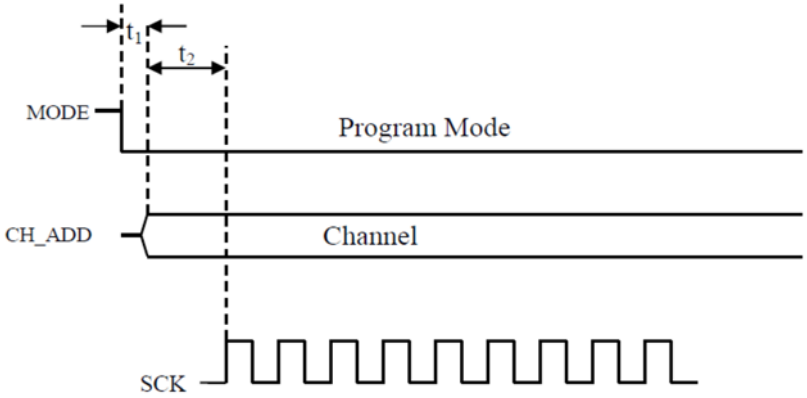
TIMING SPECIFICATION TABLE

SPEC	DESCRIPTION	MIN	MAX	UNIT
t_1	SCLK period	4 cycle		t_{CLK}
t_2	SCLK pulse width (High and Low)	2 cycle		t_{CLK}
t_3	SS low to first SCLK edge	100		ns
t_4	Last SCLK falling edge to SS HIGH	100		ns
t_5	SCK rising edge to DIN valid (Hold time)	50		ns
t_6	DIN valid to SCLK rising edge (Setup time)	50		ns
t_7	SCLK falling Edge to valid new DOUT		50[2]	ns
t_8	SCLK falling Edge to DOUT, Hold Time	0[3]		ns
t_9	Delay between last SCLK edge of 1st byte transfer and first SCLK edge for subsequent 2nd byte transfer : RREG, WREG Command	10		t_{CLK}
t_{10}	Final SCLK edge of one command until first edge SCLK of next command	4		t_{CLK}

Notes: (1) DOUT goes immediately into tri-state whenever SS is high,
(2) DOUT pin output load should be less than 20pF
(3) DOUT should be sampled externally on rising edge of SCLK. DOUT will remain valid till next falling edge.

tclk: Master Clock Period

PROGRAMING MODE TIMING SPECIFICATIONS:



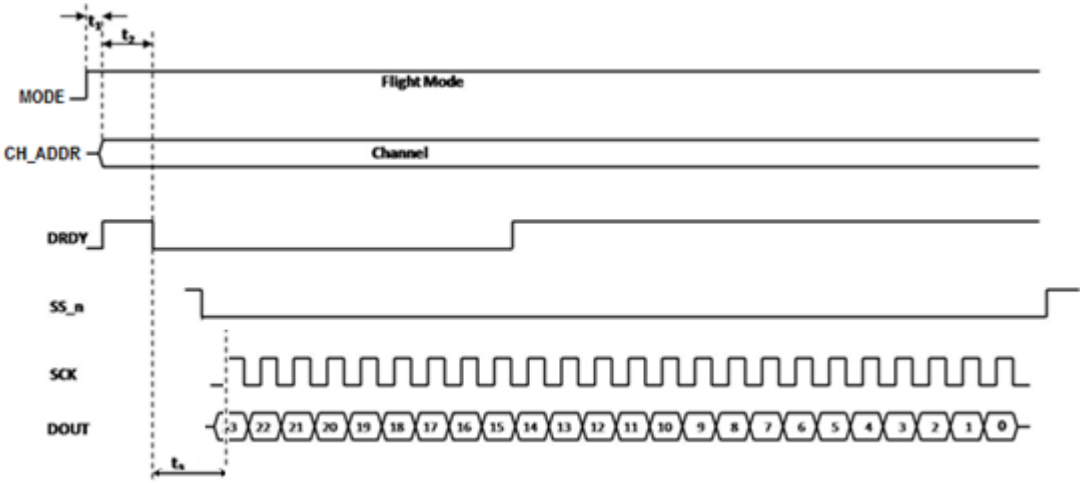
TIMING DIAGRAM

TIMING SPECIFICATION TABLE

SPEC	DESCRIPTION	MIN	MAX	UNIT
t_1	Mode change to channel change	1		t_{CLK}
t_2	Channel Change to First Edge of SCLK	4		t_{CLK}

tclk: Master Clock Period

FLIGHT MODE TIMING SPECIFICATIONS:



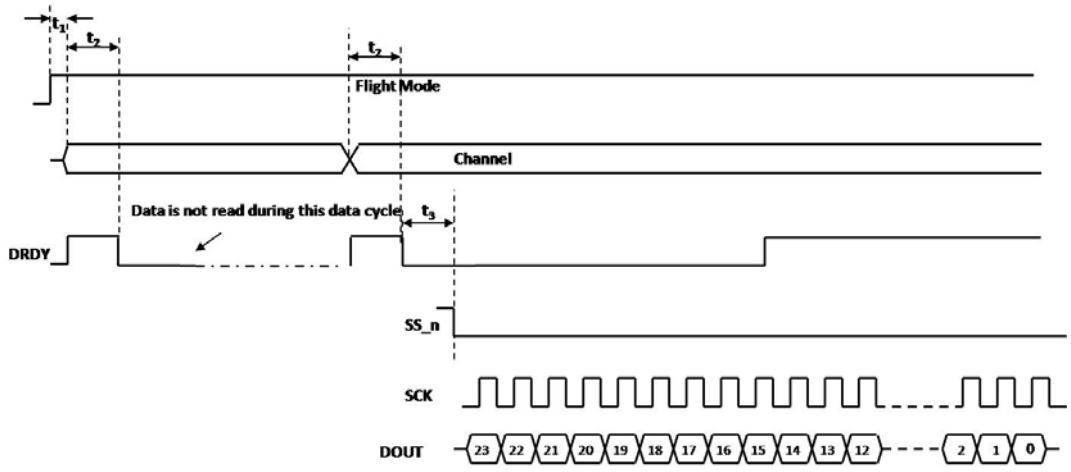
TIMING DIAGRAM

TIMING SPECIFICATION TABLE

SPEC	DESCRIPTION	MIN	MAX	UNIT
t_1	Mode change to channel change	1		t_{CLK}
t_2	Channel Change to DRDY Low	20		t_{CLK}
t_3	DRDY Low to First Edge of SCK	1		t_{CLK}

Notes: (1) It is mandatory to read at least two bytes of output data, otherwise DRDY will remain low till next filter clock or till next Channel change.
(2) In case filter clock comes during reading of output data, the data will not be updated until SS_N goes high.

FLIGHT MODE TIMING SPECIFICATIONS:



TIMING DIAGRAM

TIMING SPECIFICATION TABLE

SPEC	DESCRIPTION	MIN	MAX	UNIT
t_1	Mode change to channel change	1		t_{CLK}
t_2	Channel Change to DRDY Low	20		t_{CLK}
t_3	DRDY Low to SS_N LOW	1		t_{CLK}

Notes: In case a channel is selected and no read operation is performed, then DRDY will go high at the change of the channel and remain high for 20 master clock cycles.

tclk: Master Clock Period

ELECTRICAL CHARACTERISTICS

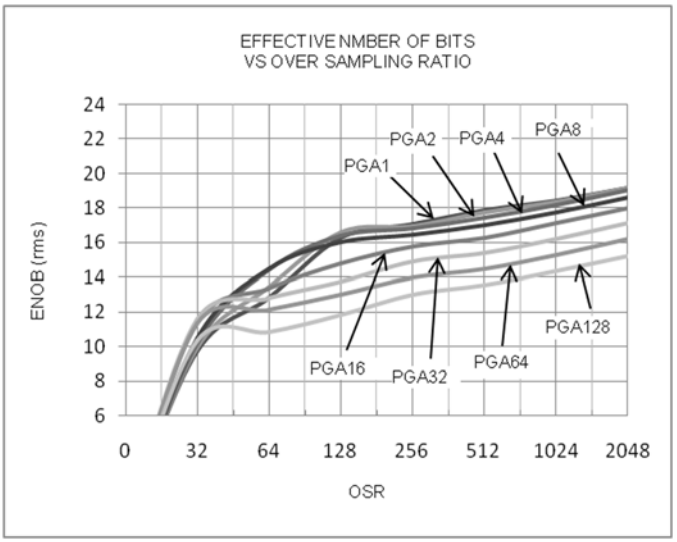
All specifications are at AVDD, DVDDO = +3.3V, Temp. = 25ºC, OSR = 2047, f_{MOD} = 2 MHz, f_{CLK} = 4MHz, f_{Data} = 976.5625 Hz, PGA=1, REFP_HI = 2.5V, REFN_HI = 0V unless otherwise specified.

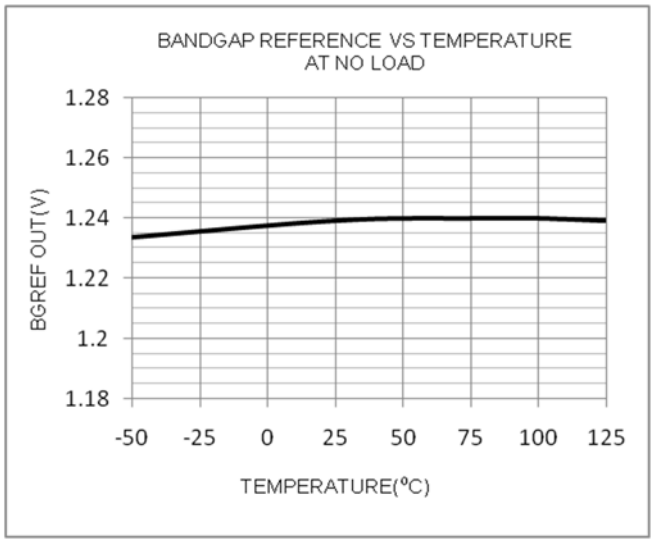
PARAMETER	TEST CONDITION	SC1239-0			UNIT
		MIN	TYP	MAX	
ADC PERFORMANCE					
Analog Input Range		0		AVDD	V
Full Scale Input Range	V_{INP}-V_{INN}	-V_{REF}/PGA		+V_{REF}/PGA	V
Programmable Gain Amplifier	User Selectable	1		128	
Input Current*			641		µA
Input Capacitance*			32		pF
Bandwidth					
Sinc^5 Filter*	-3dB		0.2*f_{Data}		Hz
Differential Input Impedance			3.9		KΩ
Resolution		24			Bits
Integral Non-Linearity	Best Fit Method			±0.05	% of FSR
Offset Error	After Calibration			0.5	ppm of FSR
Offset Drift	-55ºC to +125ºC			0.03	ppm/ºC
Gain Error	After Calibration			50	% of FSR
Gain Drift	-55ºC to +125ºC			1.67	ppm/ºC
Effective Number of Bits (ENOB)	Based on 100 samples			20	Bits
Common-Mode Rejection	At DC = 1.65		99		dB
Master Clock Rate	f_{CLK}			20	MHz
ON CHIP VOLTAGE REFERENCE					
Output Voltage	Load Current = 1µA	1.237	1.239	1.241	V
Load Regulation	Full Load =2.5mA			1	%
Drift	-55ºC to +125ºC			31	ppm/ºC
VOLTAGE REFERENCE INPUT					
External High Reference	(REFP_HI)-(REFN_HI)			2.5	V
External Low Reference	(REFP_LO)-(REFN_LO)			1.25	V
POWER SUPPLY REQUIREMENT					
Supply Voltage	AVDD, DVDDO, MVDD	3.0	3.3	3.6	V
Analog Current	STATIC		17	17.8	mA
Digital Current	STATIC		0.12	0.27	mA
AVDD Current	DYNAMIC @ F_{CLK}=20MHz		40.4		mA
ON CHIP LDO					
Supply Voltage	VDD_LDO	3.0	3.3	3.6	V
Output Voltage	OUT_LDO	1.81	1.82s	1.83	V
Line Regulation				1	%
TEMPERATURE RANGE					
Operating		-55		125	ºC

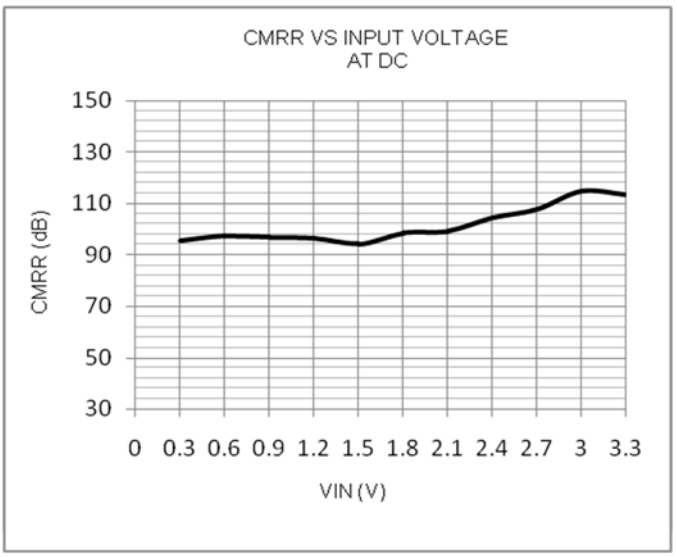
* Simulated Result

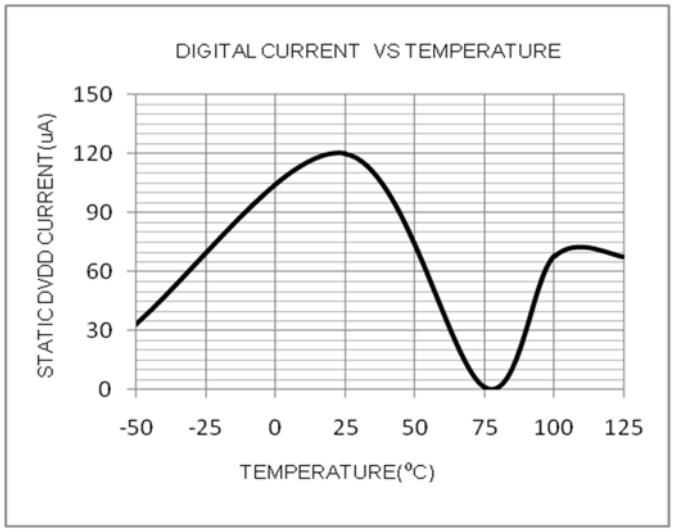
ELECTRICAL CHARACTERISTICS

All specifications are at AVDD, DVDDO = +3.3V, Temp. = 25ºC, OSR = 2047, f_{MOD} = 2 MHz, f_{CLK} = 4MHz, f_{Data} = 976.5625 Hz, PGA=1, REFP_HI = 2.5V, REFN_HI = 0V unless otherwise specified.









DIGITAL CHARACTERISTICS

DVDDO= 3.0V to 3.6V

PARAMETER	TESTS CONDITIONS	SC1239-0			UNITS
		MIN	TYP	MAX	
Logic Family			CMOS		
Logic Level: V_{IH}		2		DVDDO	V
V_{IL}		DVSSO		0.8	V
V_{OH}	I_{OH}=8mA	3.0			V
V_{OL}	I_{OL}=8mA	DVSSO		0.4	V
Input Leakage: I_{IH}	V_I=DVDDO			1	µA
I_{IL}	V_I=DVSSO	-1			µA

ABSOLUTE MAXIMUM RATING

PARAMETER	SC1239-0		UNITS
	MIN	MAX	
AVDD to AVSS	-0.3	4.3	V
DVDDO to DVSSO	-0.3	4.3	V
DVDD18 to DVSSO	-0.3	2.2	V
INP, INN	-0.3	AVDD+0.3	V
Digital Input Voltage to DGND	-0.3	DVDDO+0.3	V
Digital Output Voltage to DVSSO	-0.3	DVDDO+0.3	V
Maximum Junction Temperature		125	°C

OVERVIEW

PROGRAMMABLE GAIN AMPLIFIER

The Programmable Gain Amplifier (PGA) can be set to gains of 1, 2, 4, 8, 16, 32, 64, or 128. Adjusting the internal gain of a sigma delta modulator is a technique, which can be used to get an appropriate LSB size for the transducers application. It will improve the resolution of the ADC. The PGA is combined with the ∑Δ modulator.

∑Δ MODULATOR

A second order single loop sigma delta modulator is used in the Sigma Delta ADC. The sigma delta modulator converts the input signal into a digital pulse train whose average duty cycle represents the digitized signal information. The integrators used in the modulator are switched capacitor based. The first integrator of the modulator is auto-zeroed.

There are eight different ∑Δ Modulator units in Octal-Core High Frequency RDAS. Each of modulator units can be programmed independently.

The modulator runs at clock frequency $f_{mod.}$ f_{mod} can be adjusted by setting the appropriate value of PRE1: PRE0 of CR1 control register as shown in the following table:

PRE1:PRE0	f_{MOD}
00	f_{CLK} /2
01	f_{CLK} /8
10	f_{CLK} /16
11	f_{CLK} /64

Where f_{CLK} is external clock frequency

The modulator is designed to work at a maximum sampling frequency of 2 MHz. All the eight modulator units run at the same modulator frequency. In case user try to set different modulator frequencies for different modulator cores, the modulator frequency set in the last core will be taken as the modulator frequency for all the cores.

INTEGRATED FILTER MODULE

Each of ∑Δ Modulator is followed by an independent integrated digital filter unit. It comprises of $sinc^5$ filter and internal registers. The decimation ratio of each unit of filter module can be programmed independently.

The on-chip digital filter processes the single bit data stream from the corresponding modulator unit using a $sinc^5$ filter. The sinc filters are conceptually simple, efficient and flexible, especially where variable resolution and data rates are required. The output data rate of digital filter is given as:

$$\text{Data Rate} = f_{MOD} / DR$$

The Decimation Ratio (DR) of the filter can vary from 31 to 8191 and its value is represented by 13 Bits of DECIM Register and last 5 bits of CR2 Register.

Each ADC core has its own registers bank which comprise of CR1, CR2, DECIM, OCR and FSR registers. The user can read/write these registers when that particular ADC core is selected using a particular channel address on input primary pins.

DRDY (DATA READY)

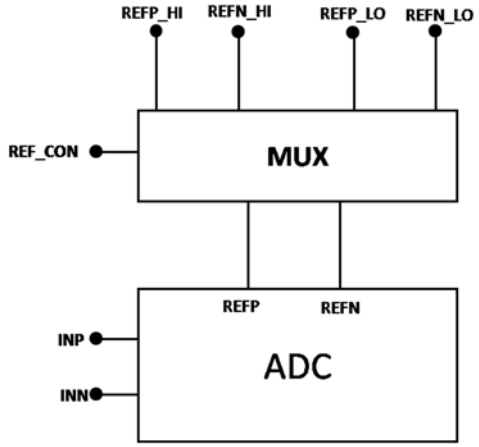
The DRDY pin is used as a status signal to indicate when new digital code is ready to be read from the selected ADC core of Octal-Core High Frequency RDAS. DRDY goes low when new data is available. It becomes high in the mid of second byte read during read operation from the data register in flight mode. In case, in response to the DRDY assertion no read operation is performed, DRDY will remain low till next filter clock cycle or till next channel change. It is mandatory for the user to read at least two bytes, otherwise the DRDY will remains low till next filter clock or channel change.

VOLTAGE REGULATOR

The device has on chip 1.8V linear voltage regulator. The input voltage range is 2.6V to 3.6V and full load current is 12mA.

REFERENCES

The device has two options of the differential references: REFP_HI, REFN_HI and REFP_LO, REFN_LO. For a particular ADC core any of the reference can be selected using the REF_CON bit of CR1 control register as shown below.



The device has on chip 1.22V bandgap reference circuitry also. To use it, the user needs to connect it externally with any one of two references.

CONTROL LOGIC

Any of the 8 ADC core for communication can be selected by applying appropriate three bits channel address on input primary pins CH_ADDR. All the operations like instruction decoding, command execution, SPI control, DRDY generation, calibration & over range management, etc are governed by this unit.

Octal-core High Frequency RDAS have two modes of operation i.e. flight mode and program mode. The chip can be made to operate in any mode based on the logic high/low of the primary input pin “MODE”.

Program Mode: During this mode (Mode Pin at Logic Low) user can program the control registers for different settings like decimation ratio, PGA, pre-scaler value, system/self calibration etc. All the commands will be recognized only in Program Mode.

Steps to be follow in program mode.

1. Set the mode of device in Program mode.
2. Set the address lines corresponding to a particular ADC core.
3. Enable the SS_N signal.
4. Set the control registers and perform the calibration.
5. Follow steps 2 and 4 for all the ADC cores.

Flight Mode: During this mode, data from selected ADC core sends out from the device. Whenever Master wants to

fetch data of a particular ADC core; place the address of ADC core on the address lines: CH_ADDR [2:0] and then asserts chip select enable signal. Thereafter, three dummy bytes are written on SPI bus and 24 bit data is received through DOUT. Valid data from device will be available at the falling edge of DRDY. During this mode no commands will be recognized by the device.

Steps to be follow in flight mode.

1. Set the mode of the device in Flight mode
2. Set the address lines corresponding to a particular ADC core.
3. Wait for negative edge of DRDY signal.
4. Enable the SS_N signal.
5. Read the data of selected ADC through DOUT.
6. Disable the SS_N Signal.
7. To read data from other ADC cores, repeat steps 2 to 6.

SERIAL INTERFACE

The serial interface is standard four-wire SPI compatible (DIN, DOUT, SCLK and SS_N). All ADC core can communicate serially through single SPI. The user has to select a particular ADC core for data transaction by placing a three bits address line CH_ADDR [2:0].

SS_N (Serial Interface Enable): The SS_N input must be externally asserted before a master device can exchange data with the ADC. SS_N must be Low for the duration of the transaction. DOUT pin will become tri-state when SS_N pin goes high. When SS_N is Low, the output data register will never be updated even if new data comes. After data read operation, it should be made high.

SCK (Serial clock): SCK function as a clock for serial communication. The device will sample serial data on positive edge of SCK. Data from device will be launched on negative edge of SCK.

DIN (Data input): DIN is the serial data input port. It is internally sampled at positive edge of SCK by SPI.

DOUT (Data output): DOUT is the serial data output port. It is internally launched by SPI at negative edge of SCK. DOUT immediately goes into tri-state when SS_N is high.

OFFSET AND GAIN CALIBRATION

Both the self offset error and complete system offset error in selected ADC core can be reduced with offset calibration. This is handled with two offset commands SEFOCAL and SYSOCAL. There is also a gain calibration module to compensate self gain and system gain error with SELFGAIN and SYSGAIN command respectively. ***Please refer calibration procedure section.*** Each calibration process takes seven conversion cycles to complete. Therefore, it takes 14 conversion cycles to complete both offset and gain calibration. Calibration must be performed after system reset, a change in decimation ratio or a change of the PGA.

Calibration commands will only update the Offset Calibration Register (OCR) with appropriate offset value. However, to enable the offset correction, OCEN bit of CR1 control register has to be set separately. Similarly to apply gain correction, GCALEN bit has to be set.

SELFGAIN command is only possible at PGA1.

OVER-LOAD DETECTION MODULE

Where digital code without calibration is such that it cannot be corrected after calibration then Over-Load detection module detects over-load and clip digital output appropriately to $7FFFFF_H$ and 800000_H.

Status of over-load detection module is available at ORD Pin. This pin will become high in case of over-load condition.

Over-load detection can be disabled by setting OLDD flag of CR2 control register. By default it is enabled.

OVER-RANGE DETECTION MODULE

If digital code after gain and offset calibration is out of the acceptable code range then digital over-range module detects over-range and clip digital output appropriately to $7FFFFF_H$ and 800000_H. To ensure the proper functioning of the Over Range Detection Module, following constraint on OCR & FSR register value must be followed:

Maximum value of OCR register should not exceed $3FFFFF_H$ for negative offset correction and $C00000_H$ for positive offset correction.

FSR value must be positive.

When device is in the over-range condition, the ORD pin will become high.

Over-range detection can be disabled by setting ORDD flag of CR2 control register. By default it is enabled.

ORDD bit also affects digital output range. Setting ORDD bit will half the digital output range as shown below.

ORDD BIT	ANALOG INPUT	DIGITAL OUTPUT CODE
0	$+V_{REF}$	$7FFFFF_H$
	0	000000_H
	$-V_{REF}$	800000_H
1	$+V_{REF}$	$3FFFFF_H$
	0	000000_H
	$-V_{REF}$	$C00000_H$

CALIBRATION PROCEDURE

The Octal-Core High Frequency RDAS has two commands namely SEFOCAL and SYSOCAL to compensate offset errors. Internal calibration of device is called self calibration. By executing SELFOCAL command, the device shorts the ADC input and stores the offset value into OCR register in 2's complement form.

For system calibration, the user must apply appropriate 'zero signal' to the selected input channel and then execute SYSOCAL command. In this case ADC computes the offset value based on the available differential input signal and stores it into OCR register in 2's complement form. The System gain calibration requires appositive "full scale differential input signal. On executing system gain command, ADC computes a value to nullify gain error. At the completion of calibration, the DRDY signal will go Low to indicate that calibration is complete and valid data is available.

Calibration commands will only update the Offset Calibration Register (OCR) with appropriate offset value. However, to enable the offset correction, OCEN bit of CR1 control register has to be set separately. Similarly to enable gain calibration set GCALEN bit of CR1 register. Each calibration process takes five conversion cycles to complete. DRDY will be asserted to indicate completion of the calibration process.

Apart from above commands, OSR and FSR can be accessed externally through RREG (Read Register) and WREG (Write Register) commands. This will provide flexibility to manually set the OCR and FSR.

COMMAND DEFINITIONS

The commands listed below control the operation of SC1239-0 Device. Some commands are stand-alone commands (e.g. SELFOCAL) while others require additional bytes (e.g., WREG requires command and the data bytes).

Operands:
rrrr represents the register address.

nnnnnnnn represents the data.

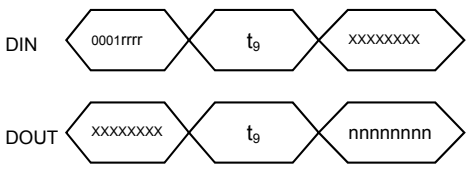
xxxx: these bits will be ignored while instruction decoding.

COMMANDS	DESCRIPTION	COMMAND BYTE	2ND COMMAND BYTE
RREG	Read from Register rrrr	0100 rrrr ($4r_H$)	-N.A.-
WREG	Write to Register rrrr	0101 rrrr ($5r_H$)	nnnnnnnn
SELFOCAL	Self Offset Calibration	0110 xxxx ($6x_H$)	-N.A.-
SYSOCAL	System Offset Calibration	0111 xxxx ($7x_H$)	-N.A.-
SELFGAIN	Self Gain Calibration	1000 xxxx ($8x_H$)	-N.A.-
SYSGAIN	System Gain Calibration	1001 xxxx ($9x_H$)	-N.A.-

RREG (READ REGISTER)

RREG (Read Register) command reads content of the specified register. The address of the register to be read is specified in the LSB nibble of the instruction.

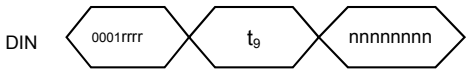
Operands: r, n
Bytes: 2
Encoding: 0100 rrrr



WREG (WRITE REGISTER)

WREG (Write Register) command writes the data to specified register. The address of the register to be written is specified in the LSB nibble of the first byte. Second byte represents the data to be written.

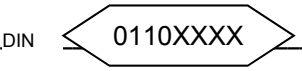
Operands: r, n
Bytes: 2
Encoding: 0101rrrr nnnnnnnn



SELFOCAL (SELF OFFSET CALIBRATION)

This command performs Self Offset Calibration. At the end of the calibration process, offset value will be stored in 24-bit internal Offset Calibration Register (OCR) is in 2's complement format. DRDY will be asserted low to indicate completion of the command.

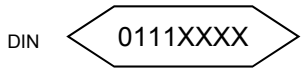
Operands: x
Bytes: 1
Encoding: 0110 xxxx



SYSOCAL (SYSTEM OFFSET CALIBRATION)

With this command ADC computes the offset value based on the available differential input signal on ADC input to nullify offset in the system. The offset value will be stored in 24-bit internal Offset Calibration Register (OCR) in 2's complement format. DRDY will be asserted low to indicate completion of the command.

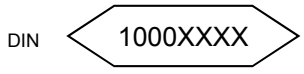
Operands: x
Bytes: 1
Encoding: 0111xxxx



SELFGIAN (SELF GIAN CALIBRATION)

This command performs Self Gain Calibration. At the end of the calibration process, gain calibration coefficient value will be stored in 24-bit internal FSR Register. DRDY will be asserted low to indicate completion of the command.

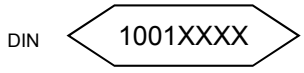
Operands: x
Bytes: 1
Encoding: 1000 xxxx



SYSGAIN (SYSTEM GAIN CALIBRATION)

With this command ADC computes the gain value based on the available differential input signal on ADC input to nullify gain error in the system. The gain value will be stored in 24-bit internal FSR Register. DRDY will be asserted low to indicate completion of the command.

Operands: x
Bytes: 1
Encoding: 1001xxxx



CONTROL / STATUS REGISTERS

The operation of the device is set up through following control / status registers.

Address	Register	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0_H	DIGITAL_CODE_B1 (R)	DC23	DC22	DC21	DC20	DC19	DC18	DC17	DC16
1_H	DIGITAL_CODE_B2 (R)	DC15	DC14	DC13	DC12	DC11	DC10	DC9	DC8
2_H	DIGITAL_CODE_B3 (R)	DC7	DC6	DC5	DC4	DC3	DC2	DC1	DC0
3_H	CR1 (RW)	PGA2	PGA1	PGA0	OCEN	GCALEN	REFCON	PRE1	PRE0
4_H	CR2 (RW)	Data Format	OLDD	ORDD	OSR12	OSR11	OSR10	OSR9	OSR8
5_H	DECIM_reg(RW)	OSR7	OSR6	OSR5	OSR4	OSR3	OSR2	OSR1	OSR0
7_H	OCR1 (RW)	OCR07	OCR06	OCR05	OCR04	OCR03	OCR02	OCR01	OCR00
8_H	OCR2 (RW)	OCR15	OCR14	OCR13	OCR12	OCR11	OCR10	OCR09	OCR08
9_H	OCR3 (RW)	OCR23	OCR22	OCR21	OCR20	OCR19	OCR18	OCR17	OCR16
A_H	FSR1 (RW)	FSR07	FSR06	FSR05	FSR04	FSR03	FSR02	FSR01	FSR00
B_H	FSR2 (RW)	FSR15	FSR14	FSR13	FSR12	FSR11	FSR10	FSR09	FSR08
C_H	FSR3 (RW)	FSR23	FSR22	FSR21	FSR20	FSR19	FSR18	FSR17	FSR16

R: Read only registers, RW: Read/Write registers
Note: At reset all registers are initialized to 00_H on reset.

CR1 (ADD: 03_H) CONTROL REGISTER-1

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
PGA2	PGA1	PGA0	OCEN	GCALEN	REFCON	PRE1	PRE0

BIT 7-5:PGA2:PGA1:PGA0: Programmable Gain Amplifier selection

000 = 1 100 = 16
001 = 2 101 = 32
010 = 4 110 = 64
011 = 8 111 = 128

Bit 4: OCEN: Offset Calibration Enable bit
OCE = 1: Enable offset calibration
OCE = 0: Disable offset calibration

Bit 3: GCALEN: Gain calibration Enable bit
GCALEN = 1: Enable Gain calibration
GCALEN = 0: Disable Gain calibration

Bit 2: REFCON: Reference Control Bit
0: REFP_LO and REFN_LO will be selected
1: REFP_HI and REFN_HI will be selected

Bit 1-0: PRE1:PRE0: Prescaler bits

PRE1:PRE0	f_{MOD}
00	f_{CLK} /2
01	f_{CLK} /8
10	f_{CLK} /16
11	f_{CLK} /64

CR2 (ADD: 04_H) CONTROL REGISTER- 2

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
DATA FORMAT	OLDD	ORDD	OSR12	OSR11	OSR10	OSR9	OSR8

Bit 7: Data Format of the output code
1 = Offset Binary output data
0 = 2's complement output data

Bit 6: OLDD: Over-Load Detection Disable
0 = Enable over-load detection.
1 = Disable over-load detection.

Bit 5: ORDD: Over-Range Detection Disable
0 = Enable over-range detection.
1 = Disable over-range detection.

Bit 2-0:OSR10:OSR9: OSR8 control bits.
Three MSBs of 13 bits of decimation ratio
Note: Any update in CR1 or CR2 control register will reset modulator and digital filter. DRDY will also go high.

DECIM (ADD: 05_H) CONTROL REGISTER-3

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
OSR7	OSR6	OSR5	OSR4	OSR3	OSR2	OSR1	OSR0

BIT 7-0: OSR7:OSR0
These bits are the 8 LSB bits of 13 bit decimation ratio.

OCR1 (ADD: 07_H) OFFSET CALIBRATION REGISTER-1
(Least Significant Byte)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
OCR07	OCR06	OCR05	OCR04	OCR03	OCR02	OCR01	OCR00

OCR2 (ADD: 08_H) OFFSET CALIBRATION REGISTER-2
(Middle Byte)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
OCR15	OCR14	OCR13	OCR12	OCR11	OCR10	OCR09	OCR08

OCR3 (ADD: 09_H) OFFSET CALIBRATION REGISTER-3
(Most Significant Byte)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
OCR23	OCR22	OCR21	OCR20	OCR19	OCR18	OCR17	OCR16

FSR1 (ADD: $0A_H$) FULL SCALE CALIBRATION REGISTER-1
(Least Significant Byte)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FSR07	FSR06	FSR05	FSR04	FSR03	FSR02	FSR01	FSR00

FSR2 (ADD: $0B_H$) FULL SCALE CALIBRATION REGISTER-2
(Middle Byte)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FSR15	FSR14	FSR13	FSR12	FSR11	FSR10	FSR09	FSR08

FSR3 (ADD: $0C_H$) FULL SCALE CALIBRATION REGISTER-3
(Most Significant Byte)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FSR23	FSR22	FSR21	FSR20	FSR19	FSR18	FSR17	FSR16

DIGITAL_CODE_B1 (ADD: 00_H) DIGITAL OUTPUT CODE
(Most Significant Byte)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
DC23	DC22	DC21	DC20	DC19	DC18	DC17	DC16

DIGITAL_CODE_B2 (ADD: 01_H) DIGITAL OUTPUT CODE
(Middle Byte)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
DC15	DC14	DC13	DC12	DC11	DC10	DC09	DC08

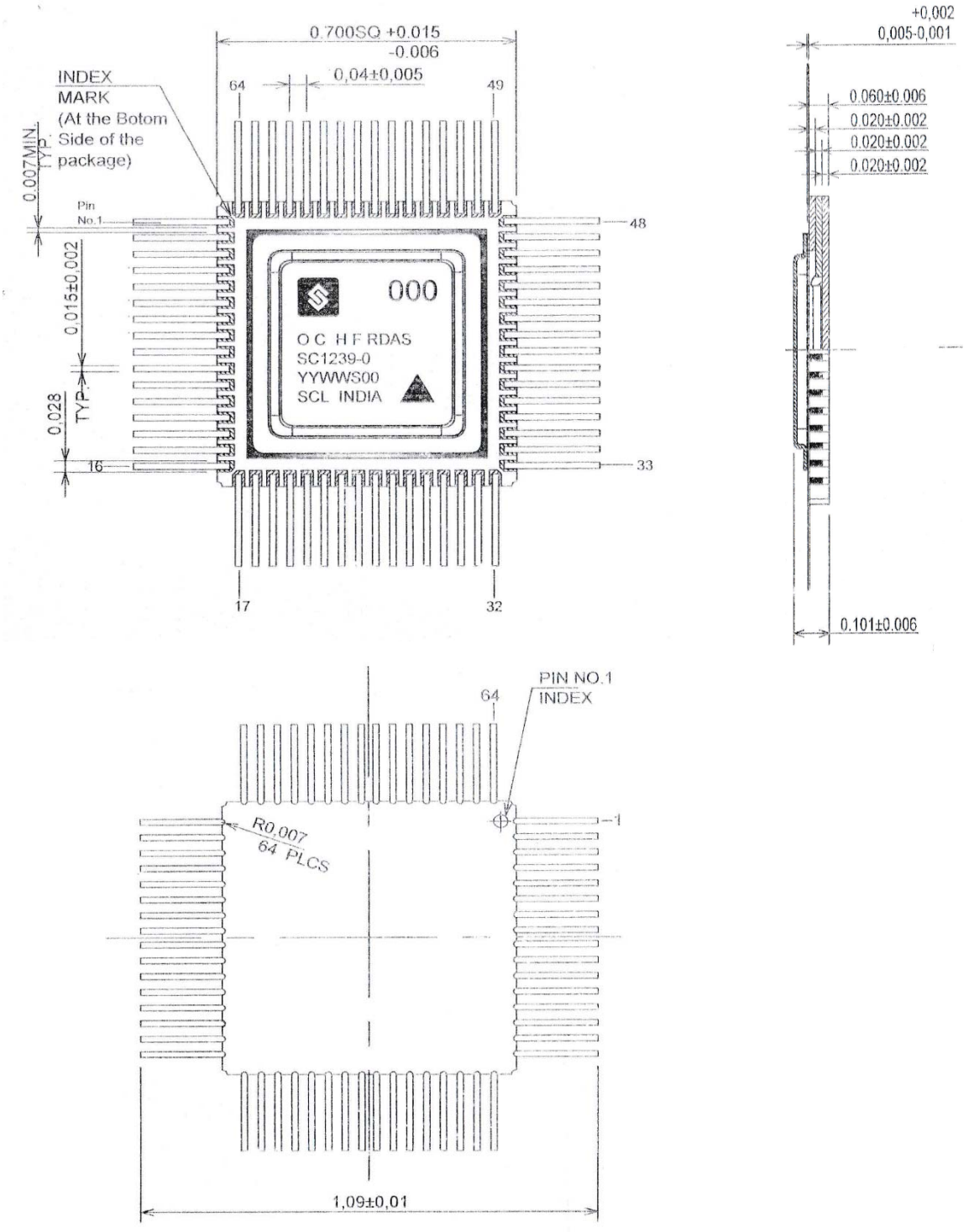
DIGITAL_CODE_B3 (ADD: 02_H) DIGITAL OUTPUT CODE
(Least Significant Byte)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
DC07	DC06	DC05	DC04	DC03	DC02	DC01	DC00

PACKAGE INFORMATION

64-PIN CQFP

ALL Dimensions are in inch unless until specified.



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