SC1237-0

Datasheet -August 2021

16 CHANNELS SIMULTANEOUS SAMPLING 24 BIT Σ-Δ ADC (MULTI-CORE RDAS1.1)

FEATURES:

- **Sixteen ΣΔ ADCs**
  - **24 Bits resolution**
  - **No missing code[1]**
  - **PGA from 1 to 128 (Binary Steps)**
  - **Programmable Output Data Rate**
  - **0.005% INL**
  - **19 Bits ENOB (PGA = 1, OSR=2047)**
  - **On-chip Offset and Gain Calibrations**
  - **Data Format Selection**
- **Thirty Two IDACs**
  - **8 Bits resolution**
  - **Programmable Full Scale Ranges of 0.5 mA, 1mA and 2mA.**
- **Precision on-chip 1.22V Reference Accuracy: 1.7%, Drift: ±80ppm**
- **On Chip 1.8V Voltage Regulator**
- **Program and Flight Mode Operation**
- **SPI Compatible**
- **3.0V TO 3.6V**
- **180nm SCL CMOS standard logic process**
- **θ_{JC} =0.88°C/W**

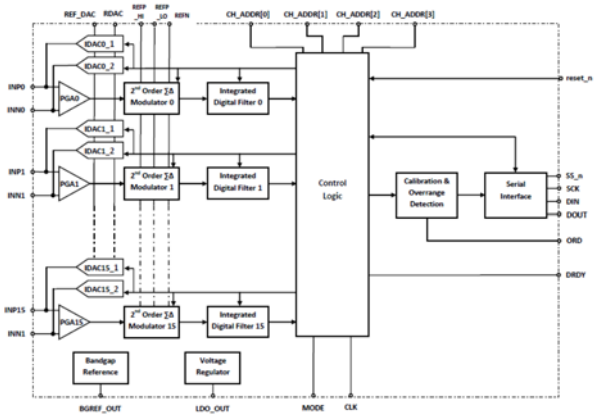
Notes: (1) Tested and verified upto 14 Bits.

DESCRIPTION:

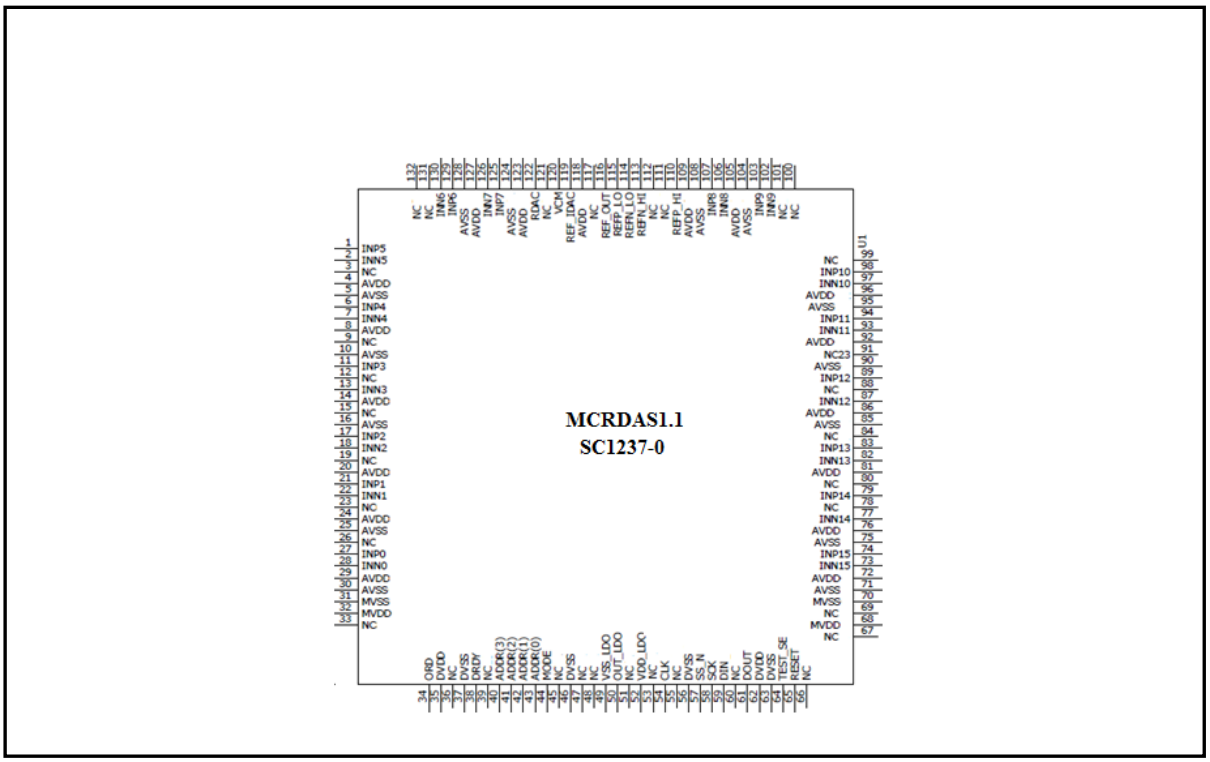
Multi-Core Reconfigurable Data Acquisition System (Multi Core RDAS) is a fully integrated data acquisition system. It incorporates 16 high resolution Sigma Delta (ΣΔ) ADCs, 32 Eight Bits IDACs along with the calibration and over-range detection unit for each ΣΔ ADC. User can communicate with any of the ADC through SPI interface using four bits channel address. There are two modes of operation: Program mode and Flight mode. User can select any of the modes through a primary input pin. During Program Mode, user can program all the ADC cores and IDACs and during flight mode user can read the data continuously.

Each ΣΔ ADC uses a second order modulator with a Programmable Gain Amplifier (PGA) and on-chip offset and gain calibration. ΣΔ Modulator converts the analog input signal into a single bit stream of 1s and 0s where the density of 1s and 0s represents the digitized information. The single bit data from modulator is then processed by a digital *Sinc*^{3} filter to produce a 24 bits digital output. The output data rate of ΣΔ ADC is programmable.

Each 8-bits current DAC is available with three different ranges: 0.5mA, 1mA and 2mA.



PIN CONFIGURATION:



PIN DESCRIPTIONS:

PIN NO.	NAME	Analog/ Digital	Description
1	INP5	Analog Input / Output	ADC 5 Positive Input / Current DAC 5 1st Output(Note-1)
2	INN5	Analog Input / Output	ADC 5 Negative Input / Current DAC 5 2nd Output(Note-1)
3	NC	-	Not Connected
4	AVDD	Analog	3.3 V – Analog Supply
5	AVSS	Analog	0 V – Analog Ground
6	INP4	Analog Input / Output	ADC 4 Positive Input / Current DAC 4 1st Output(Note-1)
7	INN4	Analog Input / Output	ADC 4 Negative Input / Current DAC 4 2nd Output(Note-1)
8	AVDD	Analog	3.3 V – Analog Supply
9	NC	-	Not Connected
10	AVSS	Analog	0 V – Analog Ground
11	INP3	Analog Input / Output	ADC 3 Positive Input / Current DAC 3 1st Output(Note-1)
12	NC	-	Not Connected
13	INN3	Analog Input / Output	ADC 3 Negative Input / Current DAC 3 2nd Output(Note-1)
14	AVDD	Analog	3.3 V – Analog Supply
15	NC	-	Not Connected
16	AVSS	Analog	0 V – Analog Ground
17	INP2	Analog Input / Output	ADC 2 Positive Input / Current DAC 2 1st Output(Note-1)
18	INN2	Analog Input / Output	ADC 2 Negative Input / Current DAC 2 2nd Output(Note-1)
19	NC	-	Not Connected
20	AVDD	Analog	3.3 V – Analog Supply
21	INP1	Analog Input / Output	ADC 1 Positive Input / Current DAC 1 1st Output (Note-1)
22	INN1	Analog Input / Output	ADC 1 Negative Input / Current DAC 1 2nd Output (Note-1)
23	NC	-	Not Connected
24	AVDD	Analog	3.3 V – Analog Supply

25	AVSS	Analog	0 V – Analog Ground
26	NC	-	Not Connected
27	INP0	Analog Input / Output	ADC 0 Positive Input / Current DAC 0 1st Output(Note-1)
28	INN0	Analog Input / Output	ADC 0 Negative Input / Current DAC 0 2nd Output(Note-1)
29	AVDD	Analog	3.3 V – Analog Supply
30	AVSS	Analog	0 V – Analog Ground
31	MVSS	Analog	0 V – It can be shorted to AVSS. Mixed Signal Ground
32	MVDD	Analog	3.3 V – It can be shorted to AVDD. Mixed Signal Supply
33	NC	-	Not Connected
34	ORD	Digital Output	Test Pin – Can be left open
35	DVDD	Digital	3.3 V – Digital PAD Supply
36	NC	-	Not Connected
37	DVSS	Digital	0 V – Digital Ground
38	DRDY	Digital Output: Active Low	Data Ready Signal
39	NC		Not Connected
40	ADDR[3]	Digital Input	4th bit of Channel Address to select any of 16 ADCs.
41	ADDR[2]	Digital Input	3rd bit of Channel Address to select any of 16 ADCs
42	ADDR[1]	Digital Input	2nd bit of Channel Address to select any of 16 ADCs
43	ADDR[0]	Digital Input	1st bit of Channel Address to select any of 16 ADCs
44	MODE	Digital Input	Mode Selection to select Program Mode or Flight Mode
45	NC	-	Not Connected
46	DVSS	Digital	0 V – Digital Ground
47	NC	-	Not Connected
48	NC	-	Not Connected
49	VSS_LDO	Digital	0 V – LDO Ground. It can be shorted externally to DVSS.
50	OUT_LDO	Digital	1.8V LDO Output for Digital Core Supply.
51	NC	-	Not Connected
52	VDD_LDO	Digital	3.3V – LDO Supply. To be shorted externally to DVDD.
53	NC	-	Not Connected
54	CLK	Digital Input	ADC Master Clock
55	NC	-	Not Connected
56	DVSS	Digital	0 V – Digital Ground
57	SS_N	Digital Input: Active Low	Chip Select
58	SCK	Digital Input	Serial Clock Input
59	DIN	Digital Input	Serial Data Input
60	NC	-	Not Connected
61	DOUT	Digital Output	Serial Data Output
62	DVDD	Digital	3.3 V – Digital PAD Supply
63	DVSS	Digital	0 V – Digital Ground
64	TEST_SE	Digital Input	Test Pin - Must to connected to DVSS
65	RESET	Digital Input: Active Low	Reset Signal: Reset the entire Chip. Reset signal should be of 4 Master Clock of ADC
66	NC	-	Not Connected
67	NC	-	Not Connected
68	MVDD	Analog	3.3 V –Mixed Signal Supply. It can be shorted to AVDD.
69	NC	-	Not Connected
70	MVSS	Analog	0 V – Mixed Signal Ground. It can be shorted to AVSS.
71	AVSS	Analog	0 V – Analog Ground
72	AVDD	Analog	3.3 V – Analog Supply
73	INN15	Analog Input / Output	ADC 15 Negative Input / Current DAC 15 2nd Output(Note-1)
74	INP15	Analog Input / Output	ADC 15 Positive Input / Current DAC 15 1stOutput(Note-1)
75	AVSS	Analog	0 V – Analog Ground

76	AVDD	Analog	3.3 V – Analog Supply
77	INN14	Analog Input / Output	ADC 14 Negative Input / Current DAC 14 2nd Output(Note-1)
78	NC	-	Not Connected
79	INP14	Analog Input / Output	ADC 14 Positive Input / Current DAC 14 1st Output(Note-1)
80	NC	-	Not Connected
81	AVDD	Analog	3.3 V – Analog Supply
82	INN13	Analog Input / Output	ADC 13 Negative Input / Current DAC 13 2nd Output(Note-1)
83	INP13	Analog Input / Output	ADC 13 Positive Input / Current DAC 13 1st Output(Note-1)
84	NC	-	Not Connected
85	AVSS	Analog	0 V – Analog Ground
86	AVDD	Analog	3.3 V – Analog Supply
87	INN12	Analog Input / Output	ADC 12 Negative Input / Current DAC 12 2nd Output(Note-1)
88	NC	-	Not Connected
89	INP12	Analog Input / Output	ADC 12 Positive Input / Current DAC 12 1st Output(Note-1)
90	AVSS	Analog	0 V – Analog Ground
91	NC	-	Not Connected
92	AVDD	Analog	3.3 V – Analog Supply
93	INN11	Analog Input / Output	ADC 11 Negative Input / Current DAC 11 2nd Output(Note-1)
94	INP11	Analog Input / Output	ADC 11 Positive Input / Current DAC 11 1st Output(Note-1)
95	AVSS	Analog	0 V – Analog Ground
96	AVDD	Analog	3.3 V – Analog Supply
97	INN10	Analog Input / Output	ADC 10 Negative Input / Current DAC 10 2nd Output
98	INP10	Analog Input / Output	ADC 10 Positive Input / Current DAC 10 1st Output
99	NC	-	Not Connected
100	NC	-	Not Connected
101	NC	-	Not Connected
102	INN9	Analog Input / Output	ADC 9 Negative Input / Current DAC 9 2nd Output(Note-1)
103	INP9	Analog Input / Output	ADC 9 Positive Input / Current DAC 9 1st Output(Note-1)
104	AVSS	Analog	0 V – Analog Ground
105	AVDD	Analog	3.3 V – Analog Supply
106	INN8	Analog Input / Output	ADC 8 Negative Input / Current DAC 8 2nd Output(Note-1)
107	INP8	Analog Input / Output	ADC 8 Positive Input / Current DAC 8 1st Output(Note-1)
108	AVSS	Analog	0 V – Analog Ground
109	AVDD	Analog	3.3 V – Analog Supply
110	REFP_HI	Analog Input	High Positive Reference Input Pin for ADC
111	NC	-	Not Connected
112	NC	-	Not Connected
113	REFN_HI	Analog Input	High Negative Reference Input Pin for ADC
114	REFN_LO	Analog Input	Low Negative Reference Input Pin for ADC
115	REFP_LO	Analog Input	Low Positive Reference Input Pin for ADC
116	REF_OUT	Analog Output	Reference Output (1.22V). User has to connect a decoupling capacitor of 0.1µF and 1µF w.r.t. AVSS at this pin.
117	NC	-	Not Connected
118	AVDD	Analog	3.3 V – Analog Supply
119	REF_IDAC	Analog Input	Reference Input for Current DAC (Max Voltage: 1.25V)
120	VCM	Analog Output	Common Mode Output (VDD/2). User has to connect a decoupling capacitor of 0.1µF and 1µF w.r.t. AVSS at this pin)
121	NC	-	Not Connected
122	RDAC	Analog	Current DAC Resistor
123	AVDD	Analog	3.3 V – Analog Supply
124	AVSS	Analog	0 V – Analog Ground
125	INP7	Analog Input / Output	ADC 7 Positive Input / Current DAC 7 1st Output(Note-1)
126	INN7	Analog Input / Output	ADC 7 Negative Input / Current DAC 7 2nd Output(Note-1)

127	AVDD	Analog	3.3 V – Analog Supply
128	AVSS	Analog	0 V – Analog Ground
129	INP6	Analog Input / Output	ADC 6 Positive Input / Current DAC 6 1st Output(Note-1)
130	INN6	Analog Input / Output	ADC 6 Negative Input / Current DAC 6 2nd Output(Note-1)
131	NC	-	Not Connected
132	NC	-	Not Connected

Note1: When a user want to use only ADC input pin, the current of the corresponding current DAC should be set to zero.

SPI TIMING SPECIFICATIONS DURING PROGRAM MODE:

User has to refer to the following timing diagram during the reading/writing of registers in Program Mode.

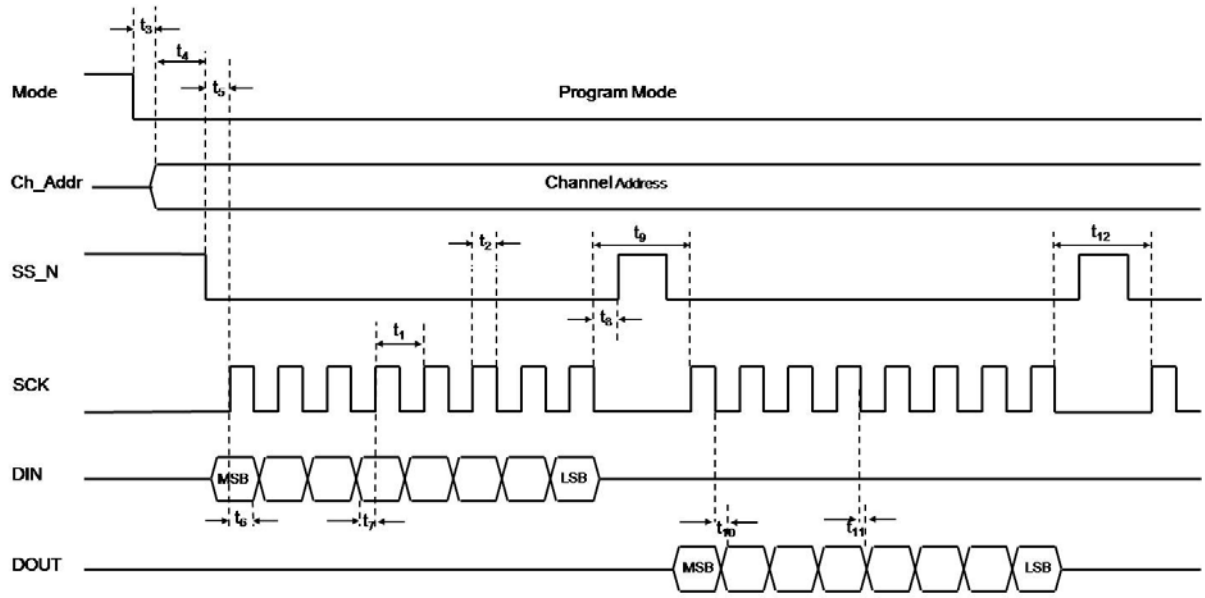


Fig. 1 Timing Specifications During Program Mode

TIMING SPECIFICATION TABLE

SPEC	DESCRIPTION	MIN	MAX	UNIT
t_1	SCK period	4 cycle		t_{CLK} Period
t_2	SCK pulse width (High and Low)	2 cycle		t_{CLK} Period
t_3	Mode change to channel change	1 cycle		t_{CLK} Period
t_4	Channel Change to SS_N low	4 cycle		t_{CLK} Period
t_5	SS_N low to first SCK edge	1 cycle		t_{CLK} Period
t_6	SCK rising edge to DIN valid (Hold time)	50		ns
t_7	DIN valid to SCK rising edge (Setup time)	50		ns
t_8	Last SCK falling edge to SS_N HIGH	100		ns
t_9	Delay between last SCL edge of 1st byte transfer and first SCK edge for subsequent 2nd byte transfer : RREG, WREG Command	10		t_{CLK} Period
t_{10}	SCK falling Edge to valid new DOUT		50[2]	ns
t_{11}	SCK falling Edge to DOUT, Hold Time	0[3]		ns
t_{12}	Final SCK edge of one command until first edge SCK of next command	4		t_{CLK} Period

t_{CLK}: Time period of ADC master clock

Notes: (1) DOUT goes immediately into tri-state whenever SS_N is high,
(2) DOUT pin output load should be less than 20pF
(3) DOUT should be sampled externally on rising edge of SCK. DOUT will remain valid till next falling edge.

FLIGHT MODE TIMING SPECIFICATIONS:

User has to refer the following timing diagram during the flight mode.

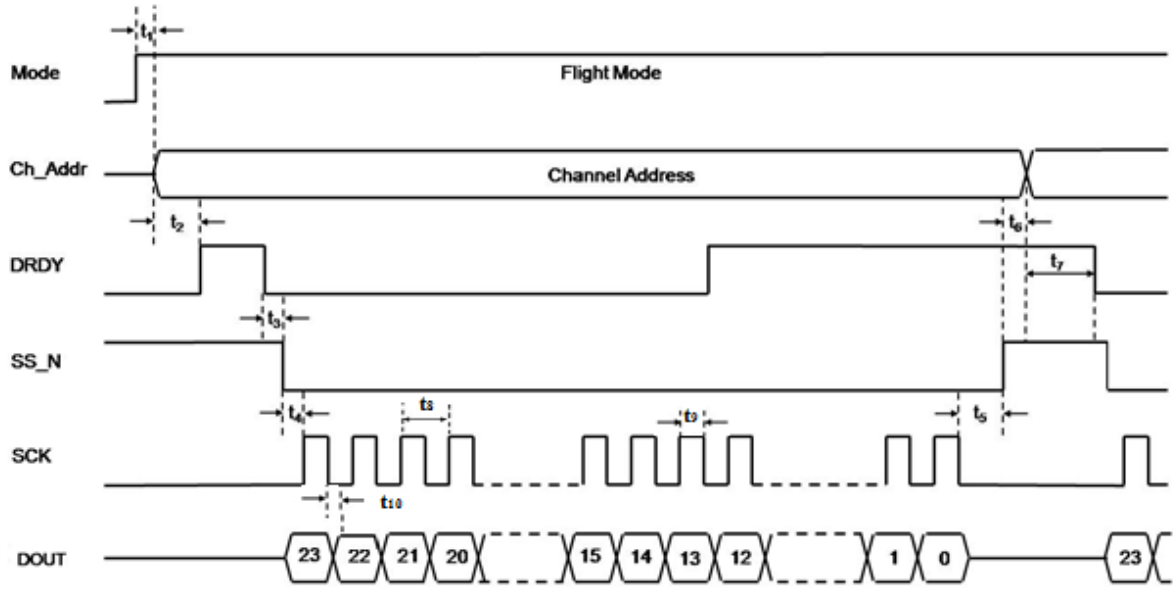


Fig. 2 Timing Specifications During Flight Mode.

TIMING SPECIFICATION TABLE

SPEC	DESCRIPTION	MIN	MAX	UNIT
t_1	Mode change to channel change	1		t_{clk} period
t_2	Channel Change to DRDY High (Note:1)	4		t_{clk} period
t_3	DRDY Low to SS_N low (Note:2)		1	t_{clk} period
t_4	SS_N low to 1st edge of SCK.	1		t_{clk} period
t_5	SCK low to SS_N High	5		t_{clk} period
t_6	SS_N High to channel change	1		t_{clk} period
t_7	Channel change to DRDY Low	20	40	t_{clk} period
t_8	SCK period	4 cycle		t_{CLK} Period
t_9	SCK pulse width (High and Low)	2 cycle		t_{CLK} Period
t_{10}	SCK falling Edge to valid new DOUT		50[3]	ns

t_{CLK}: Time period of ADC master clock

Notes: (1) In case the DRDY of the previous channel is turns low before changing the channel.
(2) Once DRDY goes low, user has to make SS_N low within one master clock.
(3) DOUT pin output load should be less than 20pF

ELECTRICAL CHARACTERISTICS

All specifications are at AVDD, DVDD, MVDD = +3.3V, VDD_LDO=3.3V, Temp. = 25ºC, OSR=2047, f_{MOD}= 156.250 KHz, f_{CLK} =5MHz, f_{Data} = 76.294 Hz, PGA=1, REFP_HI =2.5V, REFN_HI =0V, R_{DAC}=75K unless otherwise specified.

PARAMETER	TESTS CONDITIONS	SC1237-0			UNITS
		MIN	TYP	MAX	
ADC					
Analog Input Range		0		AVDD	V
Full Scale Input Range	V_{INP}-V_{INN}	-V_{REF}/PGA		+V_{REF}/PGA	V
Programmable Gain Amplifier	User Selectable	1		128	
Input Current (Dynamic)				25	µA
Input Capacitance			32		pF
Bandwidth					
Sinc^3 Filter**	-3dB		0.262*f_{Data}		Hz
Input Impedance	f_{MOD}= 78.125Kz		100		KΩ
Resolution		24			Bits
No Missing Code*	OSR=256, f_{CLK} =5MHz, f_{MOD} = f_{CLK} /64	14			Bits
Integral Non-Linearity	Best Fit Method			±0.005	% of FS
Offset Error	After Calibration			20	ppm of FS
Offset Drift	-55ºC to +125ºC			10	ppm of FS/°C
Gain Error	After Calibration			0.002	% of FS
Gain Drift	-55ºC to +125ºC			4	ppm/°C
Effective Number of Bits (ENOB)	Based on 100 samples			19	Bits
Input Common-Mode Rejection	At DC		83		dB
Reference Common-Mode Rejection	At DC	95			dB
Power Supply Rejection	DC, dB = –20 log(∆VOUT /∆VDD)		70		dB
Master Clock Rate	f_{CLK}			20	MHz
ON CHIP VOLTAGE REFERENCE					
Output Voltage	Load Current = 1µA	1.20	1.22	1.26	V
Load Regulation	Full Load =2.5mA			1	%
Drift	-55ºC to +125ºC			80	ppm/ºC
Start up Time**				240	µS
Output Impedance**			2.3		Ω
VOLTAGE REFERENCE INPUT					
External High Reference	(REFP_HI)-(REFN_HI)			2.5	V
	Bias Current		4		µA
External Low Reference	(REFP_LO)-(REFN_LO)			2.5	V
	Bias Current		4		µA
POWER SUPPLY REQUIREMENT					
Supply Voltage	AVDD	3.0	3.3	3.6	V
	DVDD	3.0	3.3	3.6	V
	VDD_LDO	3.0	3.3	3.6	V
Analog Current	I_{AVDD}		25	30	mA
Digital Current	I_{DVDD}		0.5	1	mA
Digital Current	$I_{LDO\ STATIC}$		6.0	7.5	mA
Digital Current	$I_{LDO\ DYNAMIC}$@ F_{CLK}=10MHz		9.0	10	mA
ON CHIP LDO					
Supply Voltage	VDD_LDO	3.0	3.3	3.6	V
Output Voltage	OUT_LDO	1.71	1.80	1.89	V
No Load Current			6.0	7.5	mA
Line Regulation				1	%
Load Regulation	@Full Load Current = 5mA (External)			1	%
Temp Drift	-55ºC to +125ºC			±2.0	%
IDAC					
Full Scale Output Current	R_{DAC} =75K, Range1		0.5		mA
	R_{DAC} =75K, Range2		1.0		mA
	R_{DAC} =75K, Range3		2.0		mA
Monotonocity		8			Bits

Compliance Voltage Nonlinearity Absolute Error Absolute Error Drift Mismatch Error Mismatch Error Drift	 At Same Range and Code -55ºC to +125ºC At Same Range and Code -55ºC to +125ºC			2.6 1 10 500 2 400	V %FSR % ppm/°C % FSR ppm/°C
TEMPERATURE RANGE Operating		-55		125	ºC
POWER DISSIPATION	@ All IDAC off		115		mW

* No missing codes are verified and tested upto 14bits. Device may perform for better results.
**Simulated Result

DIGITAL CHARACTERISTICS

DVDD= 3.0V to 3.6V

PARAMETER	TESTS CONDITIONS	SC1237-0			UNITS
		MIN	TYP	MAX	
Logic Family			CMOS		
Logic Level: V_{IH}		2		DVDD	V
V_{IL}		DVSS		0.8	V
V_{OH}	I_{OH}=8mA	3.0			V
V_{OL}	I_{OL}=8mA	DVSS		0.4	V
Input Leakage: I_{IH}	V_I=DVDD			1	µA
I_{IL}	V_I=DVSS	-1			µA

ABSOLUTE MAXIMUM RATING

PARAMETER	SC1237-0		UNITS
	MIN	MAX	
AVDD to AVSS	-0.3	4.3	V
DVDD to DVSS	-0.3	4.3	V
INP, INN	-0.3	AVDD+0.3	V
Digital Input Voltage to DGND	-0.3	DVDD+0.3	V
Digital Output Voltage to DVSS	-0.3	DVDD+0.3	V
Digital Output Current		8	mA
Maximum Junction Temperature		125	°C

OVERVIEW

PROGRAMMABLE GAIN AMPLIFIER

The Programmable Gain Amplifier (PGA) can be set to gains of 1, 2, 4, 8, 16, 32, 64, or 128. Adjusting the internal gain of a ∑Δ modulator is a technique, which can be used to get an appropriate LSB size for the transducers application. It will improve the resolution of the ADC.

∑Δ MODULATOR

A second order ∑Δ modulator is used in the ∑Δ ADC. The ∑Δ modulator converts the input signal into a digital pulse train whose average duty cycle represents the digitized signal information. The integrators used in the modulator are switched capacitor based.

There are sixteen different ∑Δ Modulator units in Multi-Core RDAS. Each of modulator units can be programmed independently.

The modulator runs at clock frequency f_{MOD} that can be adjusted by setting the appropriate value of PRE1: PRE0 of CR2 control register as shown in the following table:

PRE1:PRE0	f_{MOD}
00	f_{CLK} /32
01	f_{CLK} /64
10	f_{CLK} /128
11	f_{CLK} /256

where f_{CLK} is master clock frequency of ADC. The input signal is also sampled at f_{MOD}.

The modulator is designed to work at a maximum modulator frequency of *625 KHz.* All sixteen modulator units run at the same modulator frequency. It is recommended that user must set the same PRE1:PRE0 value in all the modulator cores. If different values of PRE1:PRE0 are used then, the last core PRE1:PRE0 values will be used for all the modulator cores.

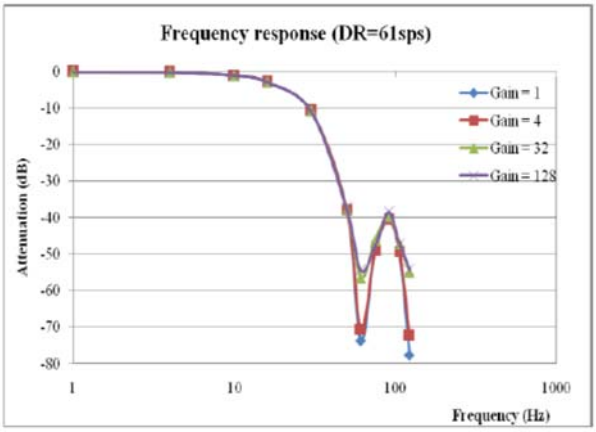
The input stage of ∑Δ modulator is a switched capacitor stage which samples the input signal at f_{MOD} on a sampling capacitor C_S of 32 *pf*. The value of the sampling capacitor is fixed for all the PGA values. The input impedance of the modulator stage can be calculated as:

$$Input\ Impedance = \frac{1}{4 f_{MOD} C_S}$$

For e.g. if f_{MOD} = 78.125 KHz, then input impedance is given as 100KΩ.

INTEGRATED FILTER MODULE

Each of ∑Δ Modulator is followed by an independent integrated digital filter unit. It comprises of *sinc*^{3} digital filter and internal registers. The Decimation Ratio (DR) of each unit of filter module can be programmed independently.



The on-chip digital filter processes the single bit data stream coming from the corresponding modulator unit using a *sinc*^{3} filter. The *sinc* filters are conceptually simple, efficient and flexible, especially where variable data rates are required. The output Data Rate of digital filter is given as:

$$\text{Data Rate} = f_{MOD} / \text{DR}$$

The Decimation Ratio (DR) of the filter is same as Oversampling Ratio (OSR). Since there is a droop in the output characteristic of the filter, the 3dB cut off frequency of the filter is *0.262* * DR. For example, if f_{MOD} is 125 KHz and DR is 512, then the Data Rate comes out to be 244Hz and maximum input frequency will be 0.262*244 i.e. 64Hz.

The DR of filter can vary from 20 to 2047 and its value is represented by 8 Bits of DECIM Register and first 3 LSBs of CR2 Register. Although, DR can have any of the value between 20 and 2047 but there are fixed numbers of decimation ratios which are implemented internally. A range of the decimation ratio belongs to a particular fixed internal decimation ratio. Depending on the selected decimation ratio from a particular range, filter will provide a gain. The gain of the filter will be:

$$Filter\ Gain = \left(\frac{DR}{Internal\ DR}\right)^3$$

A table is given below shows the Filter Gain on a various decimation ratio:

S. No.	Internal DR	DR Range		Filter Gain	
		MAX	MIN	MAX	MIN
1	2048	2047	1836	0.99	0.72
2	1626	1835	1458	1.44	0.72
3	1260	1457	1157	1.44	0.72
4	1024	1156	919	1.44	0.72
5	813	918	729	1.44	0.72
7	645	728	579	1.44	0.72
8	512	578	459	1.44	0.72
9	406	458	365	1.43	0.72
10	323	364	290	1.43	0.72
11	256	289	230	1.44	0.72
12	203	229	182	1.43	0.72
13	161	181	145	1.41	0.73
14	128	144	115	1.42	0.72
15	102	114	92	1.41	0.74
16	81	91	73	1.44	0.74
17	64	72	58	1.42	0.74
18	51	57	46	1.41	0.74
19	40	45	36	1.39	0.71
20	32	35	29	1.31	0.74
21	25	28	23	1.34	0.74
22	20	20	22	1.3	1

Depending on the value on DR, user can calculate Filter Gain. The output code of the filter data will be scaled by the corresponding Filter Gain. For e.g., If DR = 1350, the Corresponding Internal DR of the filter is 1260 (S. No. 3), then the filter gain is given as:

$$Filter\ Gain = \left(\frac{1350}{1260}\right)^3 = 1.23$$

The filter gain can be corrected using Gain Calibration.

Each ADC core has its own registers bank which comprise of CR1, CR2, DECIM, IDAC1, IDAC2, OCR and FSR registers. The user can read/write these registers during Program Mode Any of the ADC core can be selected by applying appropriate channel address at the ADDR[3:0]. The decimal equivalent of ADDR[3:0] is the selected ADC core. The details of the various registers are given in CONTROL/STATUS Registers Section.

IDAC

There are sixteen pairs of 8 Bit IDAC associated with 16 cores of ADCs. The output of each IDAC pair is shorted with positive and negative inputs of

corresponding ADC core. Each pair of IDAC can be programmed independently. The output current of a particular IDAC pair is set with RDAC, the range select bits in CR1 register and 8 Bit digital value in IDAC registers. The output current of IDAC is given as:

$$IDAC\ Current = \frac{V_{REF\_IDAC}}{8*R_{DAC}}\ (K)(2^{RANGE-1})(IDAC\ CODE)$$

RDAC resistor is an external resister to be connected at the RDAC pin. It is common to all IDACs. Range is the decimal equivalent of Range Select bits in CR1 register. IDAC CODE is the decimal equivalent of 8 bits binary value in IDAC register and K is 0.909. In case any IDAC is not being used, set the value of range as 00. It is to be noted that V_{REF_IDAC} can have a maximum value of 1.25V.

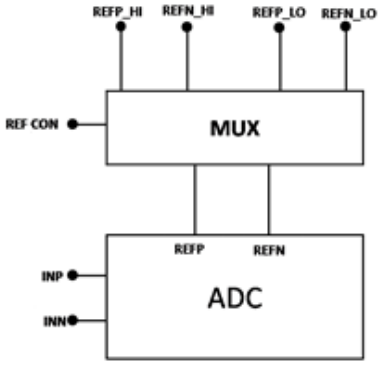
VOLTAGE REGULATOR

The device has an on chip 1.8V linear voltage regulator. The input voltage range is 3.0V to 3.6V This Voltage Regulator is provided to supply 1.8V to the digital core. The settling time of the voltage regulator is 240 µS. All the digital inputs must be applied after the settling of the regulator supply.

VOLTAGE REFERENCES INPUT

The device has two options of the differential references: REFP_HI–REFN_HI and REFP_LO–REFN_LO. For a particular ADC core any of the reference can be selected independently using the REFCON bit of CR1 control register.

REFCON Bit	Selected Reference
0	REP_LO–REFN_LO
1	REP_HI–REFN_HI



For e.g. if REFCON bit for ADC core0 is set as 1 and REFCON bit for ADC core1 is set as 0, then REFP_HI–REFN_HI pair will be selected for core0 and REFP_LO–REFN_LO pair will be selected for core1.

Both the differential reference pairs (REFP_HI–REFN_HI and REFP_LO–REFN_LO) are identical. User can apply a maximum value of 2.5V between REFP and REFN of any of differential reference pair.

ON CHIP BANDGAP REFERENCE

The device has an on chip Bandgap reference of 1.22V. To use it, the user needs to connect it externally with the REFP pin of any of the differential reference input pair (REFP_HI–REFN_HI or REFP_LO–REFN_LO) and the REFN pin of the corresponding pair must be connected to the Analog Ground. This Bandgap reference voltage can also be used as reference voltage of IDAC i.e. REF_IDAC can be shorted to REF_OUT.

SERIAL INTERFACE

The serial interface is standard four wires SPI compatible (DIN, DOUT, SCK and SS_N). All 16 ADC cores can

communicate serially through single SPI. The user has to select a particular ADC core for data transaction by placing an address on four bits address line CH_ADDR [3:0]. SPI serial interface signals are described below:

SS_N (Serial Interface Enable): The SS_N input must be externally asserted before a master device exchanges the data with the ADC. SS_N must be low for the duration of the transaction. DOUT pin will become tri- state when SS_N goes high. When SS_N is low, the output data register, from which the 24 bit output data is being transferred, will never be updated even if new data comes. After data read operation, it should be made high.

SCK (serial clock): SCK function as a clock for serial communication. The device will sample serial data on positive edge of SCK. Data from device will be launched on the negative edge of SCK.

DIN (Data input): DIN is the serial data input port. DIN is internally sampled at positive edge of SCK by SPI. The data to be transferred must be ready on the first positive edge of SCK.

DOUT (Data Output): DOUT is the serial data output port. DOUT is internally launched by SPI at negative edge of SCK by SPI. DOUT immediately goes into tri-state when SS_N is high.

DRDY (DATA READY)

The DRDY pin is used as a status signal to indicate when the new digital code of the selected ADC core is ready. DRDY goes low when new data of the selected ADC core is available. During flight mode, DRDY also goes low after some time of channel selection. Whenever user selects a channel, DRDY goes low as soon as output data of the selected channel gets ready to be read. It becomes high in the mid of second byte read during read operation in flight mode. After selecting a particular core during flight mode, it is mandatory for the user to read the data of the selected core. It is also mandatory for the user to read at least two bytes, otherwise the DRDY will remains low till next filter clock or channel change.

DRDY shows the readiness of the data to be read. User should never read the data when DRDY is high. The reading of the data during the flight mode starts by making SS_N low. Once SS_N signal is low, the data of the data register is blocked and it will not be updated even if the new data is available. But user has to make sure that never pull down the SS_N when DRDY is high.

CONTROL LOGIC

Any ADC can be selected by applying appropriate four bits channel address CH_ADDR [3:0]. The decimal equivalent of the Channel Address is the number of core which will be selected. For e.g. to select the 8^{th} core, user has to apply 1000 as channel address. All the operations like instruction decoding, command execution, SPI control, DRDY generation, calibration etc. are governed by this unit.

Multi-core RDAS have two modes of operation: Program Mode and Flight Mode. The chip can be made to operate in any mode based on the logic high/low of Mode Pin. Logic Low at the Mode pin will set Program Mode while Logic High at Mode pin will set Flight Mode.

Program Mode: During this mode (Mode Pin at Logic Low) user can program the control registers for different settings like decimation ratio, PGA, pre-scaler, IDAC currents etc. Calibration should also be carried out during this mode only. It is also possible to read the data of all the registers including Data Registers using read data command in Program mode. All the commands will be recognized only in Program Mode. Kindly refer to Fig. 1 for the timing diagram during Program Mode.

The steps to be followed during Program Mode are given below:

1. Set the mode of device in Program mode by applying 0 at the mode pin.
2. Set the address lines corresponding to a particular ADC core.
3. Enable the SS_N signal.
4. Set the control registers and perform the calibration (if needed).
5. Follow steps 2 and 4 for all the ADC cores.

When user is reading the 24 bits output data during the Program Mode, it is mandatory to keep SS_N low for the complete reading cycle i.e. during the reading of all the three bytes. Once SS_N is low, the data of the data register will not be updated even if new data is available. Also user has to make sure that SS_N should go low at the time when DRDY is low. Otherwise wrong data will be transferred.

Flight Mode: During this mode (Mode Pin at Logic High), data from selected ADC core goes out from the device. Refer to timing diagram given in Fig. 2 for the data reading during flight mode. Whenever user wants to read the data of a particular ADC core; place the address of the ADC core on the address lines: ADDR [3:0] and then asserts SS_N signal. Thereafter, three dummy bytes are written on SPI bus and 24 bit data is received through DOUT. Valid data from device will be available at the falling edge of DRDY. During this mode no commands will be recognized by the device. The steps of reading the data during flight mode are as follows:

1. Set the mode of the device in Flight mode.
2. Set the address lines corresponding to a particular ADC core.
3. Wait for negative edge of DRDY signal.
4. Enable the SS_N signal.
5. Read the data of selected ADC through DOUT.
6. Disable the SS_N Signal.
7. To read data from other ADC cores, repeat steps 2 to 6.

In Multi-Core RDAS device, a single calibration engine is used to process the data coming from all the 16 ADC's digital filter. The calibration engine takes 20 f_{CLK} to calibrate the data and this is the high period of DRDY after any channel change or after the new data is available within the same channel. Whenever there is a channel change or new data is available, DRDY goes high for 20 f_{CLK}. But there may be a case after the channel change that during calibration process, new data from the

FLIGHT MODE TIMING DIAGRAM

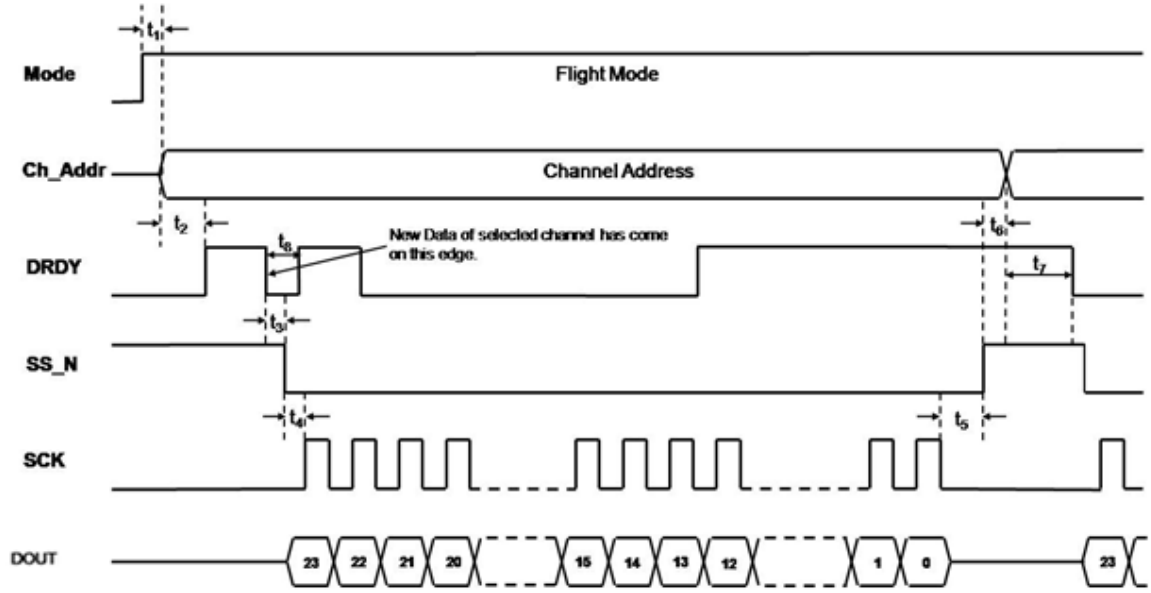


Fig. 3 Timing Specifications During Flight Mode.

TIMING SPECIFICATION TABLE

SPEC	DESCRIPTION	MIN	MAX	UNIT
t_1	Mode change to channel change	1		t_{clk} period
t_2	Channel Change to DRDY High (Note:1)	4		t_{clk} period
t_3	DRDY Low to SS_N low (Note:2)		1	t_{clk} period
t_4	SS_N low to 1st edge of SCK.	1		t_{clk} period
t_5	SCK low to SS_N High	5		t_{clk} period
t_6	SS_N High to channel change	1		t_{clk} period
t_7	Channel change to DRDY Low	20	40	t_{clk} period
t_8	Low period of DRDY in case of new data come at the same edge when DRDY was going low.	1		t_{clk} period

Notes: (1) In case the DRDY of the previous channel is turns low before changing the channel.
(2) Once DRDY goes low, user has to make SS_N low within one master clock. Detailed explanation of same is available in the DRDY section.

filter is available. In this case calibration unit takes the new data and process it. So the DRDY may remain high for 40 f_{CLK} as shown in Fig. 2.

Also there may be a special case that after the channel change, as DRDY goes low after 20 f_{CLK}, at the same time the new data from the filter comes. So after one f_{CLK}, DRDY again goes high because the calibration unit starts processing the new data coming from the digital filter of the selected channel. In this case, DRDY will go low only for one f_{CLK} and after that it will become high again. In this case the user has to pull down the SS_N within one f_{CLK} to avoid the corruption of data. In this particular case, after detecting the low edge of DRDY, if user makes the SS_N low after one f_{CLK}, then there may a case that SS_N is pull down at the time when DRDY was high. So, the corrupted data will be transferred. Kindly refer to Fig. 3 for better understanding of this case.

When it is not possible for the user to make the SS_N low within the one master clock of DRDY low edge after channel change, user need to check the status of DRDY after making the SS_N low. If the DRDY is high then again wait till DRDY goes low before reading the data. For e.g., in Fig. 3 after detecting low DRDY edge, if the user make the SS_N low after more than one f_{CLK} (when the DRDY may become high), wrong data will be transferred. Now if user again checks the status of DRDY within two master clocks, it will remain high and user has to wait till DRDY goes low before reading the data.

OVERLOAD AND OVERRANGE DETECTION MODULE:

These Modules prevents rollover of digital output code when analog input exceeds full scale value.

Digital output code will be clipped at $7FFFFF_H$and 800000_H when analog input exceeds positive and negative full scale respectively. In case the ADC input is more than 50 % of full scale range, the Over Load detection module will clip the digital output at $7FFFFF_H$ or 800000_H, accordingly.

Over-Range Detection Module also keeps into consideration of digital calibration i.e. any rollover of digital output due to calibration will also be detected by Over-Range Detection Module and will be clipped appropriately to $7FFFFF_H$and 800000_H.

To ensure the proper functioning of the Over-Range Detection Module, following constraint on OCR & FSR register value must be followed:

1. Maximum value of OCR register should not exceed $3FFFFF_H$ for negative offset correction and $C00000_H$ for positive offset correction.
2. FSR value must be positive. By default Over-Load and Over-Range Detection Modules are enabled.

1. ***Over-Load Detection module (OLDD)***

- In the scenario where digital code without calibration is such that it cannot be corrected after calibration then Over-Load detection module detects overload and clip digital output appropriately to $7FFFFF_H$ and 800000_H.
- Over-load detection can be disabled by setting OLDD bit of CR2 control register.

2. ***Over-Range Detection module (ORDD)***

- Over-range module checks for the digital code after digital offset and gain calibration. If digital code after gain and offset calibration is out of the

acceptable code range then digital over-range module detects over-range and clip digital output appropriately to $7FFFFF_H$ and 800000_H.

- Over-range detection can be disabled by setting ORDD bit of CR2 control register.

ORDD bit also affects digital output range. Setting ORDD bit will half the digital output range. In case of Over-Load or Over-Range detection, the primary output pin ORD will become high.
The Over-load and over-range modules work properly only when the decimation ratio is in the power of 2 i.e. the Digital Filter gain is unity. If the digital filter gain is not unity, then Over-range and Over-load protection module may not prevent over-range.

OFFSET AND GAIN CALIBRATION

Both the self offset error and system offset error in selected ADC core can be reduced with offset calibration. This is handled with two offset commands SELFOCAL and SYSOCAL. There is also a gain calibration module to compensate self gain and system gain error with SELFGAIN and SYSGAIN command respectively. ***Please refer calibration procedure section.*** Each calibration process takes five conversion cycles to complete. Therefore it takes 10 conversion cycles to complete both offset and gain error. Calibration must be performed after system reset, a change in decimation ratio or a change of the PGA. During Program mode, the user must perform the calibration on each and every core.

Calibration commands will only update the Offset Calibration Register (OCR) with appropriate offset value. However, to enable the offset correction, OCEN bit of CR1 control register has to be set separately. Similarly to apply gain correction, GCALEN bit has to be set.

SELFGAIN command is only possible at PGA1.

CALIBRATION PROCEDURE

The Multi-Core RDAS has two commands namely SEFOCAL and SYSOCAL to compensate offset errors. Internal calibration of device is called self-calibration. By executing SELFOCAL command, the device shorts the ADC input and stores the offset value into OCR register in 2's complement form.

For system calibration, the user must apply appropriate 'zero signal' to the selected input channel and then execute SYSOCAL command. In this case ADC computes the offset value based on the available differential input signal and stores it into OCR register in 2's complement form. The System gain calibration requires appositive "full scale differential input signal. On executing system gain command, ADC computes a value to nullify gain error. At the completion of calibration, the DRDY signal will go Low to indicate that calibration is complete and valid data is available.

Calibration commands will only update the Offset Calibration Register (OCR) with appropriate offset value. However, to enable the offset correction, OCEN bit of CR1 control register has to be set separately. Similarly to enable gain calibration set GCALEN bit of CR1 register. Each calibration process takes five conversion cycles to complete. DRDY will be asserted to indicate completion of the calibration process.

Apart from above commands, OSR and FSR can be accessed externally through RREG (Read Register) and WREG (Write Register) commands. This will provide flexibility to manually set the OCR and FSR.

POWER ON SEQUENCES

Multi-Core RDAS device needs power on sequencing. All the inputs must be applied after the power supply is settled. Analog inputs must be applied after AVDD and MVDD are settled. After DVDD/VDD_LDO is power up, the output of LDO, OUT_LDO (which is the 1.8V supply for the digital core) takes 240 µs to settle. Hence, all the digital input must be applied after 240 µs only.

COMMAND DEFINITIONS

The commands listed below control the operation of SC1237-0 Device. Some commands are stand-alone commands (e.g. SELFOCAL) while others require additional bytes (e.g., WREG requires command and the data bytes).

Operands:
rrrr represents the register address.

nnnnnnnn represents the data.

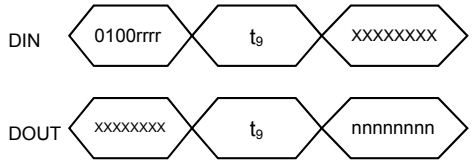
xxxx: these bits will be ignored while instruction decoding.

COMMANDS	DESCRIPTION	COMMANDBYTE	2ND COMMANDBYTE
RREG	Read from Register rrrr	0100rrrr($4r_H$)	-N.A.-
WREG	Write to Register rrrr	0101rrrr($5r_H$)	nnnnnnnn
SELFOCAL	Self Offset Calibration	0110xxxx($6x_H$)	-N.A.-
SYSOCAL	System Offset Calibration	0111xxxx($7x_H$)	-N.A.-
SELFGAIN	Self Gain Calibration	1000xxxx($8x_H$)	-N.A.-
SYSGAIN	System Gain Calibration	1001xxxx($9x_H$)	-N.A.-

RREG (READREGISTER)

RREG (Read Register) command reads content of the specified register. The address of the register to be read is specified in the LSB nibble of the instruction.

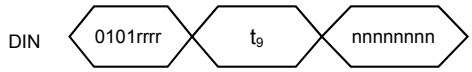
Operands: r,n
Bytes: 2
Encoding: 0100 rrrr



WREG (WRITE REGISTER)

WREG (Write Register) command writes the data to specified register. The address of the register to be written is specified in the LSB nibble of the first byte. Second byte represents the data to be written.

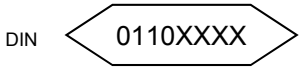
Operands: r, n
Bytes: 2
Encoding: 0101rrrr nnnnnnnn



SELFOCAL (SELF OFFSET CALIBRATION)

This command performs Self Offset Calibration. At the end of the calibration process, offset value will be stored in 24-bit internal Offset Calibration Register (OCR) is in 2's complement format. DRDY will be asserted low to indicate completion of the command.

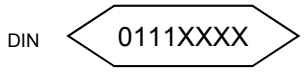
Operands: x
Bytes: 1
Encoding: 0110 xxxx



SYSOCAL (SYSTEM OFFSET CALIBRATION)

With this command ADC computes the offset value based on the available differential input signal on ADC input to nullify offset in the system. The offset value will be stored in 24-bit internal Offset Calibration Register (OCR) in 2's complement format. DRDY will be asserted low to indicate completion of the command.

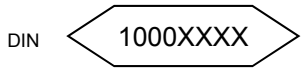
Operands: x
Bytes: 1
Encoding: 0111xxxx



SELFGAIN (SELF GAIN CALIBRATION)

This command performs Self Gain Calibration. At the end of the calibration process, gain calibration coefficient value will be stored in 24-bit internal FSR Register. DRDY will be asserted low to indicate completion of the command.

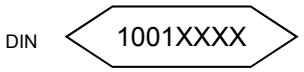
Operands: x
Bytes: 1
Encoding: 1000 xxxx



SYSGAIN (SYSTEM GAIN CALIBRATION)

With this command ADC computes the gain value based on the available differential input signal on ADC input to nullify gain error in the system. The gain value will be stored in 24-bit internal FSR Register. DRDY will be asserted low to indicate completion of the command.

Operands: x
Bytes: 1
Encoding: 1001xxxx



CONTROL / STATUS REGISTERS

The operation of the device is set up through following control / status registers.

Address	Register	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0_H	DIGITAL_CODE_B3 (R)	DC23	DC22	DC21	DC20	DC19	DC18	DC17	DC16
1_H	DIGITAL_CODE_B2 (R)	DC15	DC14	DC13	DC12	DC11	DC10	DC9	DC8
2_H	DIGITAL_CODE_B1 (R)	DC7	DC6	DC5	DC4	DC3	DC2	DC1	DC0
3_H	CR1 (RW)	PGA2	PGA1	PGA0	OCEN	GCALEN	REFCON	IDACR1	IDACR0
4_H	CR2(RW)	Data Format	OLDD	ORDD	PRE1	PRE0	OSR10	OSR9	OSR8
5_H	DECIM_reg (RW)	OSR7	OSR6	OSR5	OSR4	OSR3	OSR2	OSR1	OSR0
7_H	OCR1(RW)	OCR07	OCR06	OCR05	OCR04	OCR03	OCR02	OCR01	OCR00
8_H	OCR2(RW)	OCR15	OCR14	OCR13	OCR12	OCR11	OCR10	OCR09	OCR08
9_H	OCR3(RW)	OCR23	OCR22	OCR21	OCR20	OCR19	OCR18	OCR17	OCR16
A_H	FSR1(RW)	FSR07	FSR06	FSR05	FSR04	FSR03	FSR02	FSR01	FSR00
B_H	FSR2(RW)	FSR15	FSR14	FSR13	FSR12	FSR11	FSR10	FSR09	FSR08
C_H	FSR3(RW)	FSR23	FSR22	FSR21	FSR20	FSR19	FSR18	FSR17	FSR16
D_H	IDAC1 (RW)	IDAC1_7	IDAC1_6	IDAC1_5	IDAC1_4	IDAC1_3	IDAC1_2	IDAC1_1	IDAC1_0
E_H	IDAC2 (RW)	IDAC2_7	IDAC2_6	IDAC2_5	IDAC2_4	IDAC2_3	IDAC2_2	IDAC2_1	IDAC2_0

R: Read only registers
RW: Read/Write registers
Note: Atresetallregistersareinitializedto00_H on reset.

CR1 (ADD: 03_H) CONTROLREGISTER-1

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
PGA2	PGA1	PGA0	OCEN	GCALEN	REFCON	IDACR1	IDACR 0

BIT 7-5:PGA2:PGA1:PGA0: Programmable Gain Amplifier selection

000=1 100 = 16
001=2 101 = 32
010= 4 110 = 64
011= 8 111 = 128

Bit4: OCEN: Offset Calibration Enable bit
OCE = 1: Enable offset calibration
OCE = 0: Disable offset calibration

Bit3: GCALEN: Gain calibration Enable bit
GCALEN = 1: Enable Gain calibration
GCALEN = 0: Disable Gain calibration

Bit2: REFCON: Reference Control Bit
0: REFP_LO and REFN_LO will be selected
1:REFP_HI and REFN_HI will be selected

Bit1-0: IDACR1: IDACR0: Range Selection for current in IDAC
00 = off 10 = 1 mA
01 = 0.5 mA 11 = 2 mA

CR2 (ADD: 04_H) CONTROL REGISTER- 2

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
DATA FORMAT	OLDD	ORDD	PRE1	PRE0	OSR10	OSR9	OSR8

Bit7: Data Format of the output code
1 = Offset Binary output data
0 = 2's complement output data

Bit6: OLDD
0 = Enable over-load detection
1 = Disable over-load detection

Bit5: ORDD:
0 = Enable over-range detection
1 = Disable over-range detection

It makes output range half if disabled

ORDD BIT	ANALOG INPUT	DIGITAL OUTPUT CODE
0	$+V_{REF}$	$7FFFFF_H$
	0	000000_H
	$-V_{REF}$	800000_H
1	$+V_{REF}$	$3FFFFF_H$
	0	000000_H
	$-V_{REF}$	$C00000_H$

Bit4-3: PRE1:PRE0: Prescaler bits

PRE1:PRE0	f_{MOD}
00	f_{CLK} /32
01	f_{CLK} /64
10	f_{CLK} /128
11	f_{CLK} /256

Bit2-0:OSR10:OSR9: OSR8 control bits.
Three MSBs of 11bits of decimation ratio
Note: Any update in CR1 or CR2 control register will reset modulator and digital filter. DRDY will also go high.

DECIM (ADD: 05_H) CONTROLREGISTER-3

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
OSR7	OSR6	OSR5	OSR4	OSR3	OSR2	OSR1	OSR0

BIT 7-0:OSR7:OSR0
These bits are 8 LSB bits of 11 bit decimation ratio

OCR1 (ADD: 07_H) OFFSET CALIBRATION REGISTER-1
(Least Significant Byte)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
OCR07	OCR06	OCR05	OCR04	OCR03	OCR02	OCR01	OCR00

OCR2 (ADD: 08_H) OFFSET CALIBRATION REGISTER-2
(Middle Byte)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
OCR15	OCR14	OCR13	OCR12	OCR11	OCR10	OCR09	OCR08

OCR3 (ADD: 09_H) OFFSET CALIBRATION REGISTER-3
(Most Significant Byte)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
OCR23	OCR22	OCR21	OCR20	OCR19	OCR18	OCR17	OCR16

FSR1 (ADD: $0A_H$) FULL SCAEE REGISTER-1
(Least Significant Byte)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FSR07	FSR06	FSR05	FSR04	FSR03	FSR02	FSR01	FSR00

FSR2 (ADD: $0B_H$) FULL SCAEE REGISTER-2
(Middle Byte)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FSR15	FSR14	FSR13	FSR12	FSR11	FSR10	FSR09	FSR08

FSR3 (ADD: $0C_H$) FULL SCAEE REGISTER-3
(Most Significant Byte)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FSR23	FSR22	FSR21	FSR20	FSR19	FSR18	FSR17	FSR16

IDAC1 (ADD: $0E_H$) CURRENT DAC1

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
IDAC1_7	IDAC1_6	IDAC1_5	IDAC1_4	IDAC1_3	IDAC1_2	IDAC1_1	IDAC1_0

The DAC code bits to set IDAC1 current.

IDAC2 (ADD: $0F_H$) CURRENT DAC2

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
IDAC2_7	IDAC2_6	IDAC2_5	IDAC1_4	IDAC2_3	IDAC2_2	IDAC2_1	IDAC2_0

The DAC code bits to set IDAC2 current

DIGITAL_CODE_B3 (ADD: 00_H) DIGITAL OUTPUT CODE
(MOST SIGNIFICANT BYTE)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
DC23	DC22	DC21	DC20	DC19	DC18	DC17	DC16

DIGITAL_CODE_B2 (ADD: 01_H) DIGITAL OUTPUT CODE
(MIDDLE BYTE)

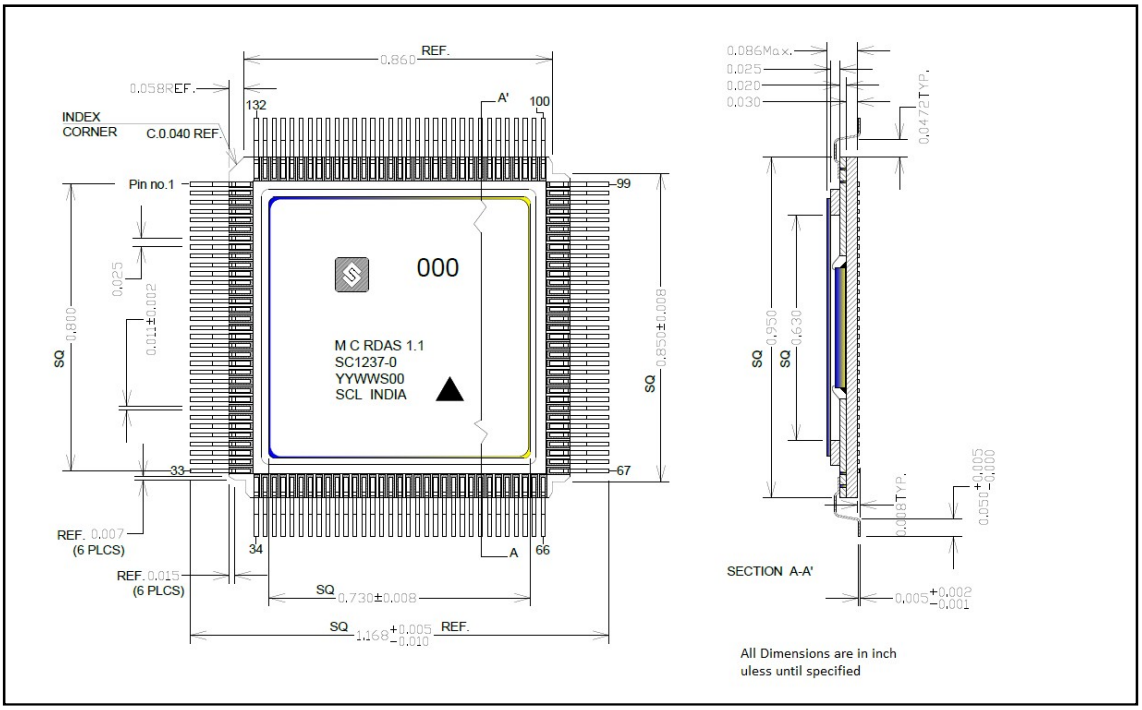
BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
DC15	DC14	DC13	DC12	DC11	DC10	DC09	DC08

DIGITAL_CODE_B1 (ADD: 02_H) DIGITAL OUTPUT CODE
(LEAST SIGNIFICANT BYTE)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
DC07	DC06	DC05	DC04	DC03	DC02	DC01	DC00

PACKAGE INFORMATION

132 Pin CQFP PACKAGE



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REVISION HISTORY

1) MCRDAS1.0 (SC1221-0) and MCRDAS1.1 (SC1237-0) are pin-to-pin compatible devices. One minor change in SC1237-0 is that the LDO output (1.8V) is internally shorted to digital core supply (DVDD18). Hence, pin number 47 and 53 are N.C.

2) The Over Load detection module is added to prevent any roll-over of the digital code when the input range exceeds the full scale range of ADC.

3) Pre-scalar values are changed from SC1221-0.

PRE1:PRE0	SC1237-0	SC1221-0
	f_{MOD}	f_{MOD}
00	f_{CLK} /32	f_{CLK} /64
01	f_{CLK} /64	f_{CLK} /128
10	f_{CLK} /128	f_{CLK} /256
11	f_{CLK} /256	f_{CLK} /512