DATA SHEET

8-BIT,1MSPS, 4-CORE SUCCESSIVE-APPROXIMATION-REGSITER(SAR) ANALOG TO DIGITAL CONVERTER

SC1236-0T1

Version 1.0, October 2022

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PRODUCT DESCRIPTION:

The 8-bit 4-Channel SAR ADC is a monolithic CMOS analog-to-digital converter capable of converting analog input signals into 8-bit digital word at 1 Mega samples per second (MSPS). The converter uses SAR architecture. Operating on a single 3.3V power supply, device achieves 8-bits effective resolution at Nyquist rate and consumes <10mW power. The inputs provide a full scale input swing equal to 3.3V. Full scale input range is recommended for optimum performance. The ASIC is fabricated in 180nm SCL CMOS standard logic process.

FEATURES

- **Resolution: 8Bit**
- **No missing code Guaranteed**
- **Output Data Format :Straight Binary**
- **Operating Voltage: 3.3V**
- **Power Consumption < 10mW**
- **Input Range : 3.3Vp-p Single Ended**
- **Operating Temperature (TA): -55ºC to +125ºC**
- **Package:64 PIN CQFP**
- **Technology: 180nm SCL CMOS Standard Logic Process**

APPLICATIONS:

- **Medical Imaging**
- **Industrial Process Control**

BLOCK DIAGRAM:

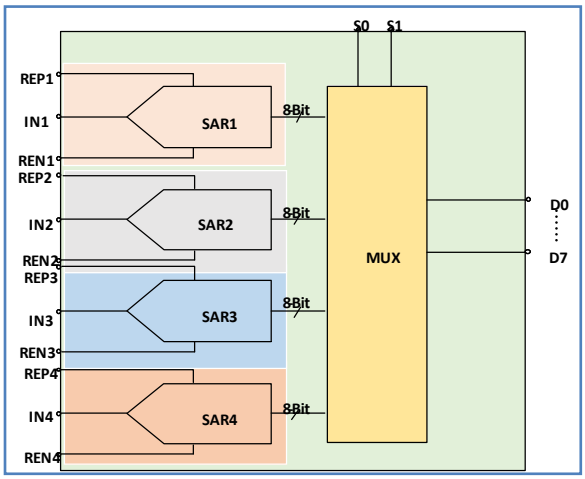

Figure-1: Device Block Diagram

DEVICE SUMMARY:

Table-1: Package Detail

Reference	Package	pins	Lead Finish	Description	Junction Temp. range
SC1236-0T1	**CQFP**	**64**	**Gold**	Engineering Model	-55°C to +125°C

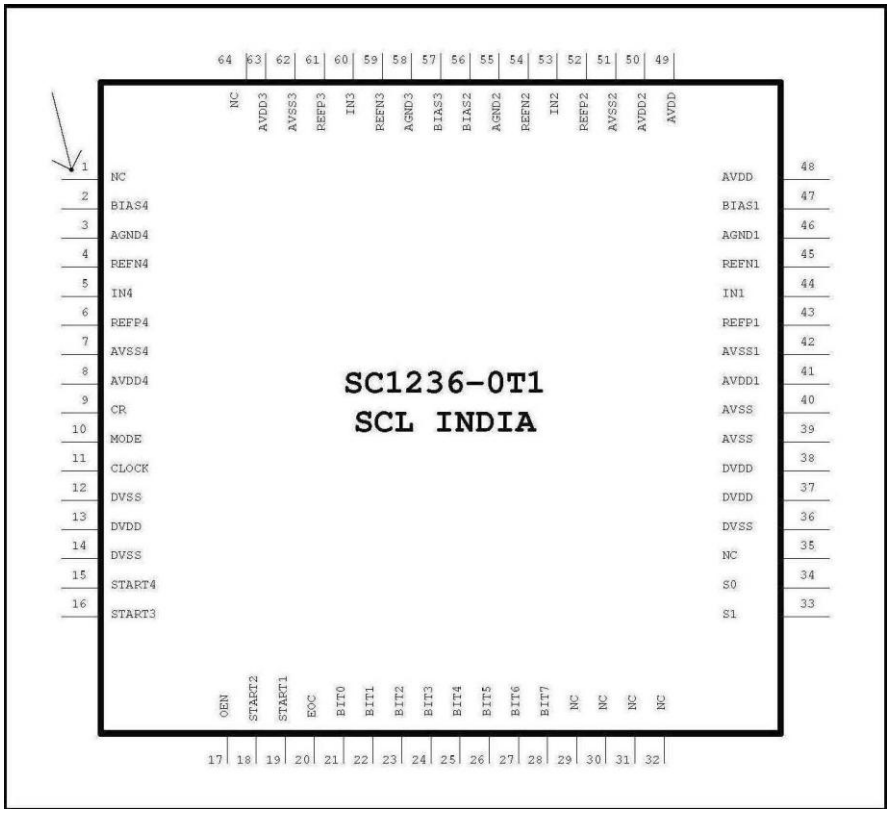

Figure-2: Pin Diagram

Table-2: Pin Configuration

Pin No.	Pin Name	Pin Type	Pin Description
7,39,40,42,51,62	AVSS	AP	Analog Negative Supply (0 V)
12,14,36	DVSS	DP	Digital Negative Supply (0 V)
8,41,48,49,50,63	AVDD	AP	Analog Positive Supply (+3.3 V)
13,37,38	DVDD	DP	Digital positive Supply (3.3 V)
9	$\overline{CR}$	DI	Clear for internal registers (Active Low)
10	MODE	DI	One Shot or Continuous Conversion Continuous Conversion: Mode=Logic1 One Shot Conversion: Mode=Logic0
11	CLOCK	DI	ADC Sampling Clock
17	$\overline{OEN}$	DI	Output enable (Active Low)
20	EOC	DO	ADC end of conversion
33	S1	DI	Control bit to select different ADC
34	S0	DI	Control bit to select different ADC
15	START4	DI	ADC4 Start
16	START3	DI	ADC3 Start
18	START2	DI	ADC2 Start
19	START1	DI	ADC1 Start
5	IN4	AI	ADC4 Analog Input
60	IN3	AI	ADC3 Analog Input
53	IN2	AI	ADC2 Analog Input
44	IN1	AI	ADC1 Analog Input
2	BIAS4	AP	ADC4 Bias Reference Voltage (1V)
57	BIAS3	AP	ADC3 Bias Reference Voltage (1V)
56	BIAS2	AP	ADC2 Bias Reference Voltage (1V)
47	BIAS1	AP	ADC1 Bias Reference Voltage (1V)
6	REFP4	AP	ADC4 Positive Reference Voltage (3.3V)
61	REFP3	AP	ADC3 Positive Reference Voltage (3.3V)
52	REFP2	AP	ADC2 Positive Reference Voltage (3.3V)
43	REFP1	AP	ADC1 Positive Reference Voltage (3.3V)
3	AGND4	AP	ADC 4 Common mode Analog Ground (1.65V)
58	AGND3	AP	ADC 3 Common mode Analog Ground (1.65V)
55	AGND2	AP	ADC 2 Common mode Analog Ground (1.65V)
46	AGND1	AP	ADC 1 Common mode Analog Ground (1.65V)
4	REFN4	AP	ADC4 Negative Reference Voltage (0V)
59	REFN3	AP	ADC3 Negative Reference Voltage (0V)

Pin No.	Pin Name	Pin Type	Pin Description
54	REFN2	AP	ADC2 Negative Reference Voltage (0V)
45	REFN1	AP	ADC1 Negative Reference Voltage (0V)
21	BIT0	DO	ADC digital output Bit (LSB)
22	BIT1	DO	ADC digital output Bit
23	BIT2	DO	ADC digital output Bit
24	BIT3	DO	ADC digital output Bit
25	BIT4	DO	ADC digital output Bit
26	BIT5	DO	ADC digital output Bit
27	BIT6	DO	ADC digital output Bit
28	BIT7	DO	ADC digital output Bit (MSB)
1,29,30,31,32,35,64	NC		Internally Not Connected

- # PIN TYPE: AI = Analog Input, AO = Analog Output, DI = Digital Input, DO = Digital Output, AP = Analog Power, DP = Digital Power.

Table-3: ADC Control Bit Selection

Pin No.	Pin Name	Pin Type	Pin Description
33,34	S1,S0	**State**	**Selected ADC**
		00	ADC1
		01	ADC2
		10	ADC3
		11	ADC4

ELECTRICAL SPECIFICATIONS:

All typical specifications are at T_A = 25°C, all power supply voltages = 3.3V unless otherwise stated. All maximum specifications are assured across operating temperature and voltage ranges.

Table-4: Electrical Specifications

Parameters	Test Conditions	Min.	Typ.	Max.	Units
POWER SUPPLY					
AVDD Analog supply voltage		2.97	3.3	3.63	V
DVDD Digital supply voltage		2.97	3.3	3.63	V
AVDD Operating current		0.381	0.956	1.175	mA
DVDD Operating current		0.063	0.122	0.192	mA
POWER DISSIPATION		1.89	3.55	4.24	mW
EXTERNALREFERENCE					
Bias Reference Voltage	BIAS		1.0		V
Positive reference voltage	REFP		3.3		V
Negative reference voltage	REFN		0		V
Common Mode Voltage	AGND		1.65		V
CURRENT REQUIREMENT					
Bias Reference Voltage	BIAS	0.082	0.121	0.137	mA
Positive reference voltage	REFP	0.005	0.028	0.049	mA
Negative reference voltage	REFN	0.006	0.027	0.060	mA
Common Mode Voltage	AGND	0.008	0.031	0.064	mA
JUNCTION TEMPERATURE		-55	25	125	°C
DIGITAL INPUT					
VIH : Logic-high input voltage		2.0		DVDD	V
VIL : Logic-low input voltage		0		0.8	V
IIH : Logic-high input current		-10	-0.9	10	µA
IIL : Logic-low input current		-10	1	10	µA
Input capacitance			5		pF
DIGITAL OUTPUT					
VOH : Logic-high output voltage	@5mA I_{OH}	3.24	3.28	3.3	V
VOL : Logic-low output voltage	@5mA I_{OL}	0	.06	0.4	V
Output load capacitance	@1MHz		10		pF

ELECTRICAL SPECIFICATIONS (CONTINUED):

Parameters	Test Conditions	Min.	Typ.	Max.	Units
Resolution			8	8	Bits
Conversion rate			1	1	MSPS
Input Range			3.3Vpp		
No missing codes			Guaranteed		
Differential nonlinearity	ADC1	-0.114	0.0035	0.14	LSB
	ADC2	-0.114	-0.0182	0.08	LSB
	ADC3	-0.114	0.00066	0.11	LSB
	ADC4	-0.114	-0.0041	0.08	LSB
Integral nonlinearity	ADC1	-0.114	0.0184	0.18	LSB
	ADC2	-0.096	0.03567	0.13	LSB
	ADC3	-0.118	0.01308	0.11	LSB
	ADC4	-0.138	0.038	0.14	LSB
Gain Error	ADC1	0.977	1.855	2.73	% of FSR
	ADC2	0.781	0.944	1.66	% of FSR
	ADC3	0.684	0.716	0.78	% of FSR
	ADC4	0.684	0.814	0.97	% of FSR
Offset Error	ADC1	0.5	0.625	0.75	LSB
	ADC2	0.25	0.563	0.75	LSB
	ADC3	0.25	0.438	0.5	LSB
	ADC4	0.5	0.688	0.75	LSB
Input referred noise			1		LSB
Effective resolution			8		Bit
AC LINEARITY					
Signal To Noise Ratio (SNR)	Clock =1MHz Test Frequency = 1004.301Hz	51.06	51.30	51.46	dB
Total Harmonics Distortion (THD)		-61.34	-58.95	-56.73	dB
Spurious-Free Dynamic Range (SFDR)		57.50	59.34	61.62	dB
Signal To Noise And Distortion (SINAD)		47.67	48.60	48.95	dB
ENOB		7.62	7.78	7.83	Bit
Analog Input capacitance (IN+,IN-)			10		pF

Table-5: Absolute Maximum Ratings*

Parameters	With respect To	Min.	Max.	Units
VIN	AVSS	-0.3	AVDD	V
DIGITAL INPUTS	AVSS	-0.3	AVDD	V
AVDD	AVSS	-0.3	3.9	V
DVDD	DVSS	-0.3	3.9	V
AVSS	DVSS	-0.3	0.3	V
DIGITAL OUTPUTS	DVSS	-0.3	DVDD	V
Storage Temperature		-65	150	ºC
Lead Temperature (10 Sec)			300	ºC
ESD Tolerance (HBM)**			> 1000	V
Latch Up Protection**			100	mA

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

**These are target value. Characterization for this is in progress.

SWITCHING SPECIFICATIONS

All typical specifications are at T_A = 25°C, all power supply voltages = 3.3 V, and conversion rate = 1MSPS, unless otherwise stated.

Table-6: **Typical timings for best performance with 1MSPS Data Rate**

Symbol	Parameter	Min	Typ	Max	Units
	Conversion Rate	1		1	MSPS
t_{CLK}	CLOCK Period		1000		ns
t_{on}	CLOCK Pulse Width High		500		ns
t_{off}	CLOCK Pulse Width Low		500		ns

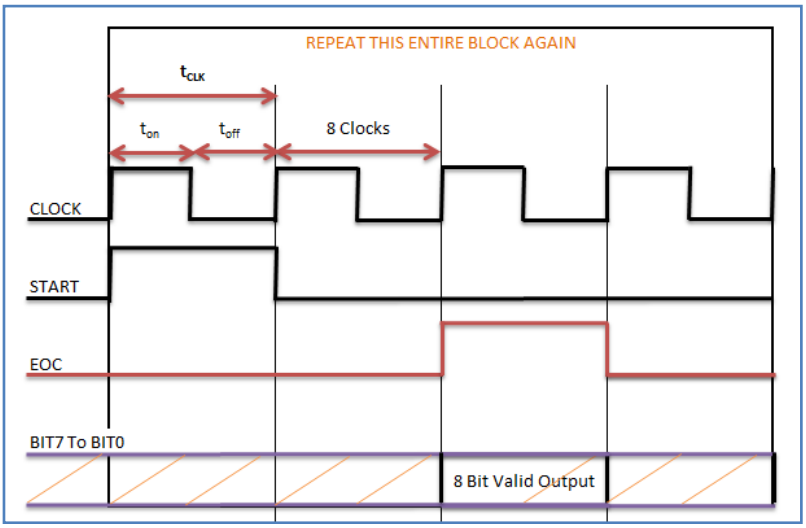

Figure-3: One Shot Mode Timing Diagram

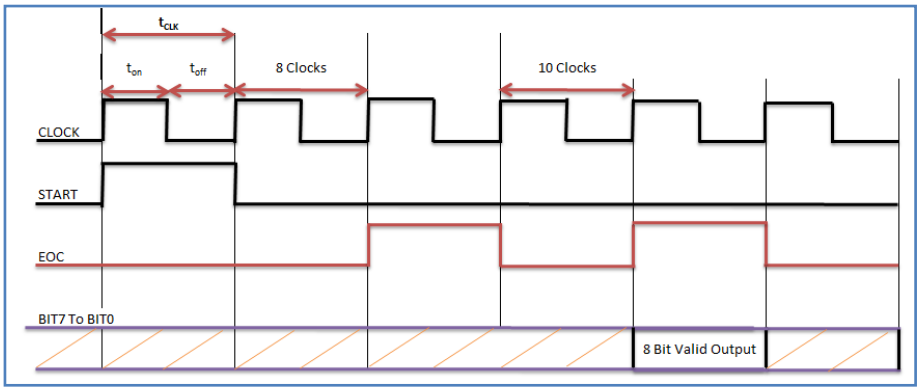

Figure-4: Continuous Conversion Mode Timing Diagram

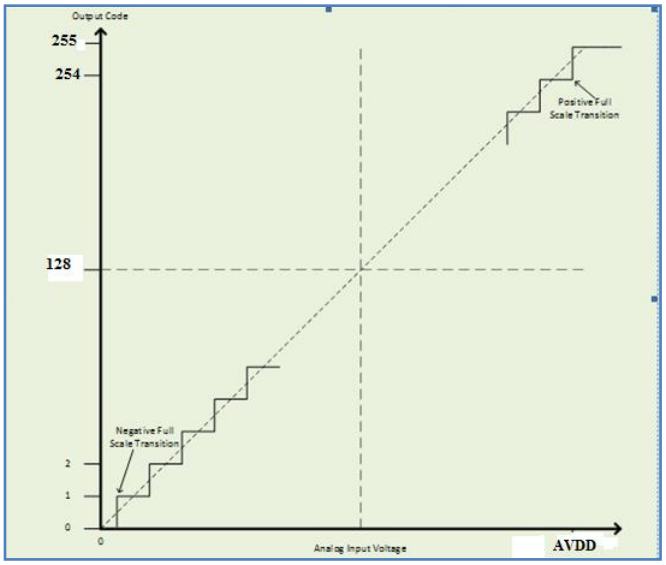

Figure-5: Transfer Characteristics of ADC

TYPICAL CHARACTERISTICS:

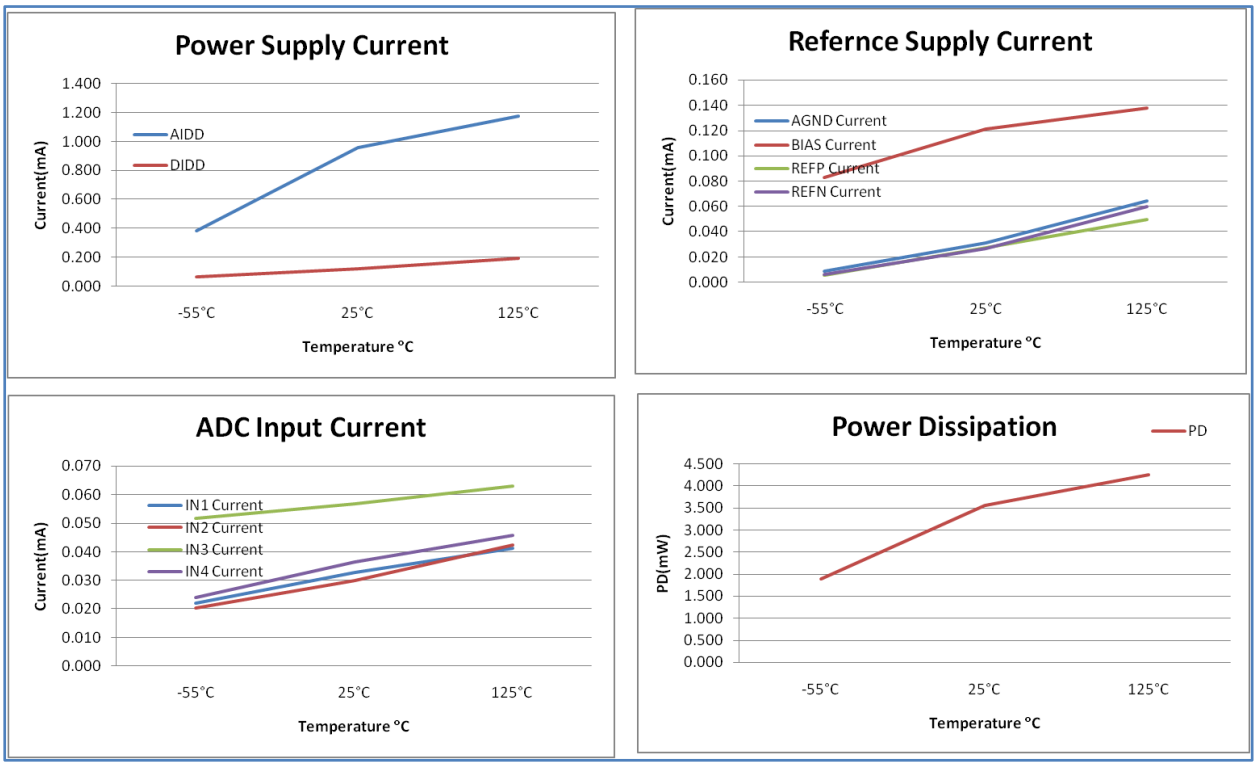

Figure 6: DC Characteristics

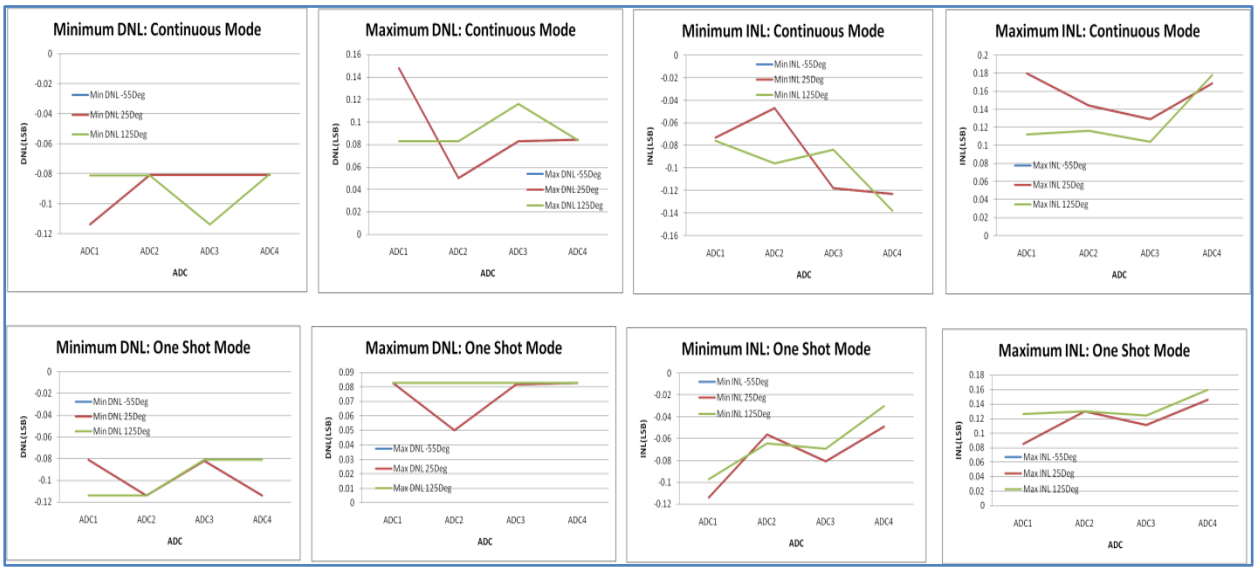

Figure-7: DNL/INL Plots

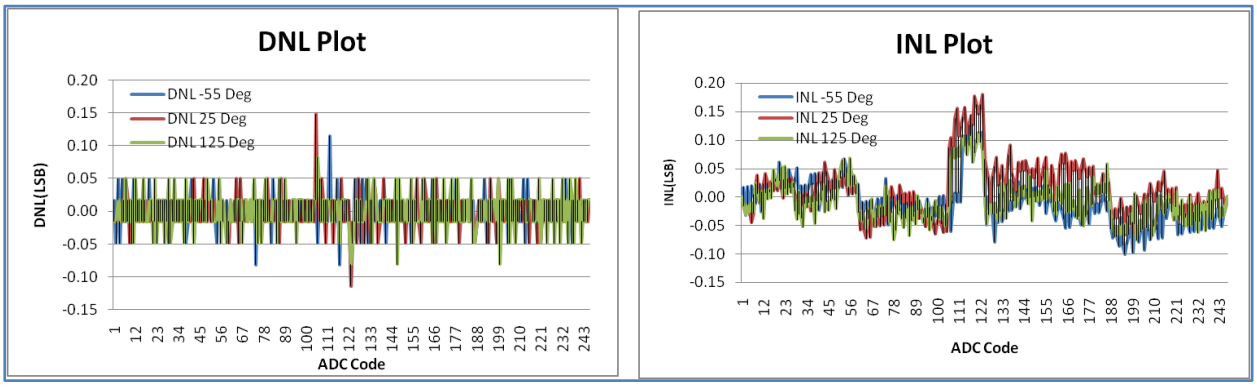

Figure-8: DNL/INL Plots

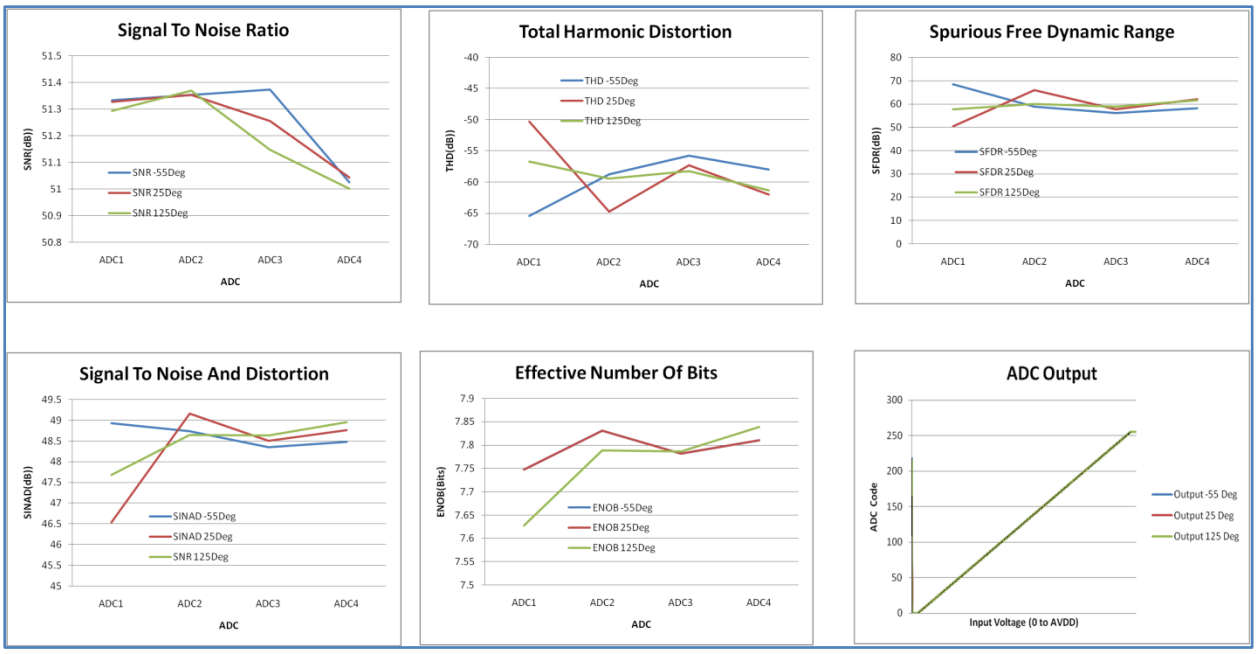

Figure-9: AC Plots

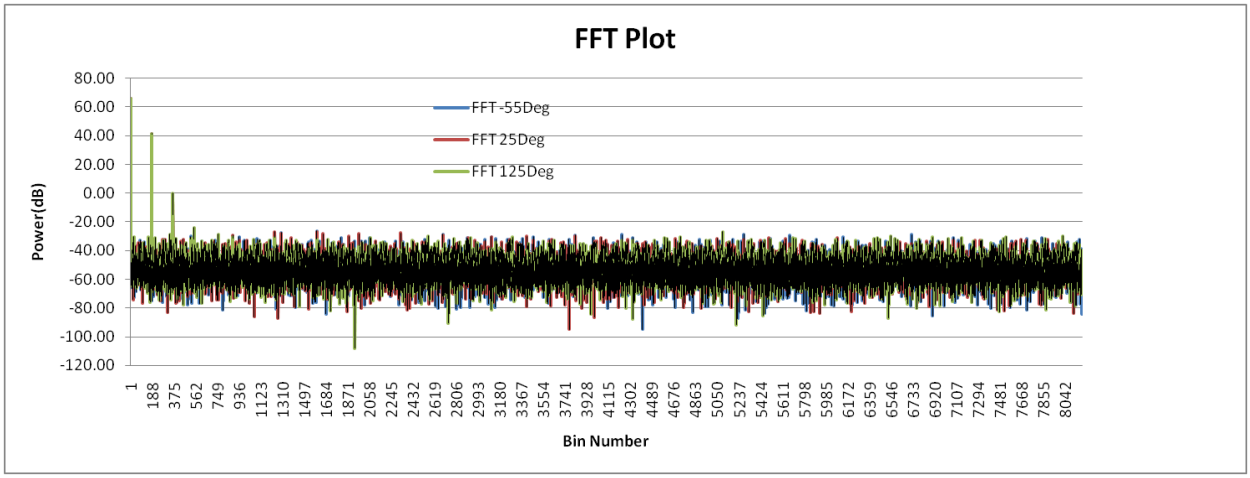

Figure-10: FFT Plots

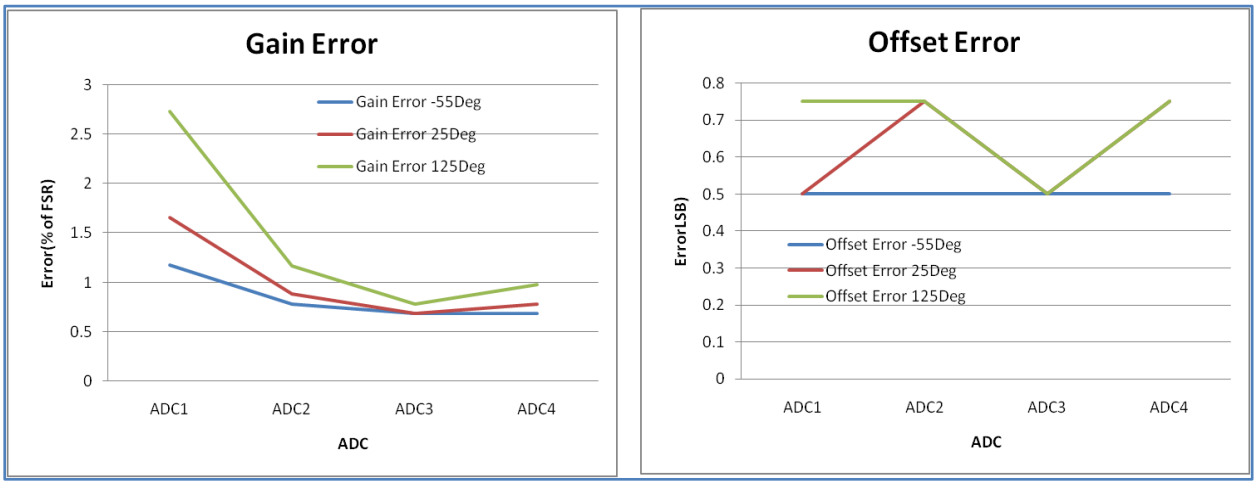

Figure-11: Gain and Offset Error

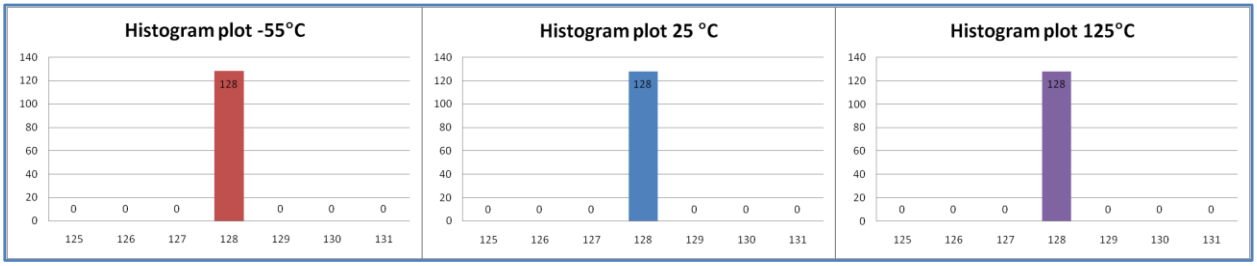

Figure-:12 Histogram plot of output codes with analog grounded input (IN=1.65V)

OVERVIEW:

DEFINITIONSOF KEY SPECIFICATIONS:

• **Differential Nonlinearity (DNL):** An ideal ADC exhibits code transitions that are exactly 1LSB apart. DNL is the deviation from this ideal value. Therefore, every code must have a finite width. No missing codes guaranteed to 8-bit resolution indicate that all 256 codes must be present overall operating conditions.

• **Input Referred Noise:** The noise is measured using histogram techniques. The standard deviation of the CSP output codes is calculated in LSB and represents the rms noise level of the total signal chain . The noise can be converted to an equivalent voltage, using the relationship

1 LSB = (ADC full scale / 2^N codes)

Where N is the bit resolution of the ADC. 1 LSB is approximately 12.941mV.

• **Effective Resolution:** The ratio of the full-scale input range to the rms input noise (from grounded input histogram test) is called as effective resolution.

$$Effective\ resolution = \log_2\left(\frac{2^N}{rms\ input\ noise\ (LSBs)}\right)$$

RMS Input Noise = Standard deviation from Grounded input Histogram Curve

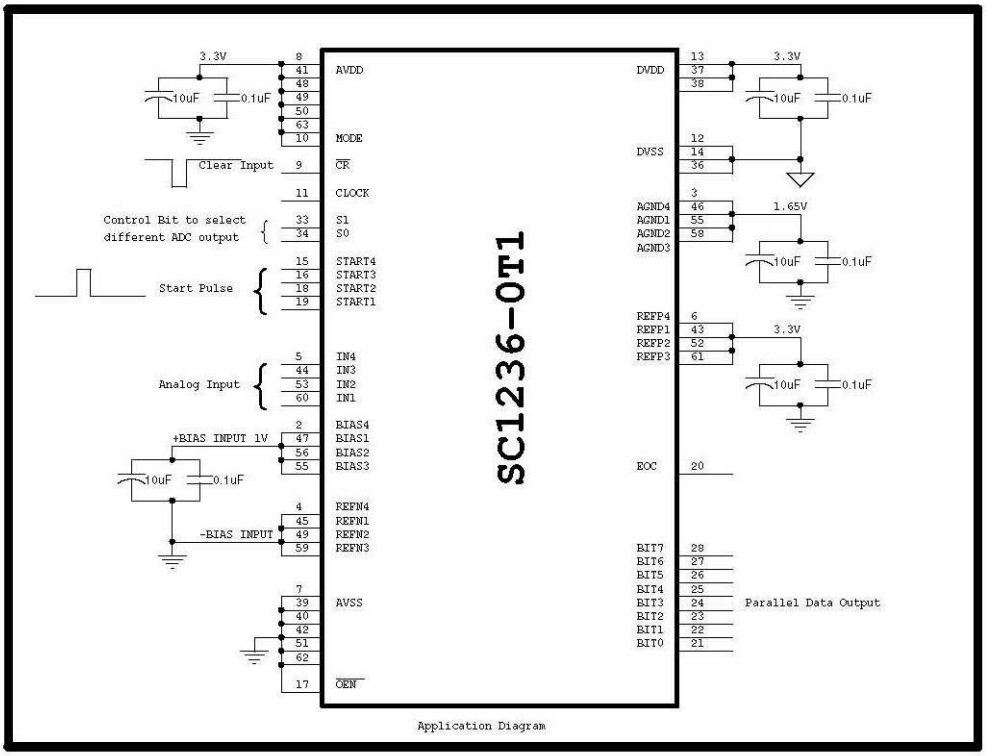

Figure-13: Application Diagram

PACKAGE DRAWING (100 Pin CQFJ):

Note7: All linear dimensions are in inches (mm.)

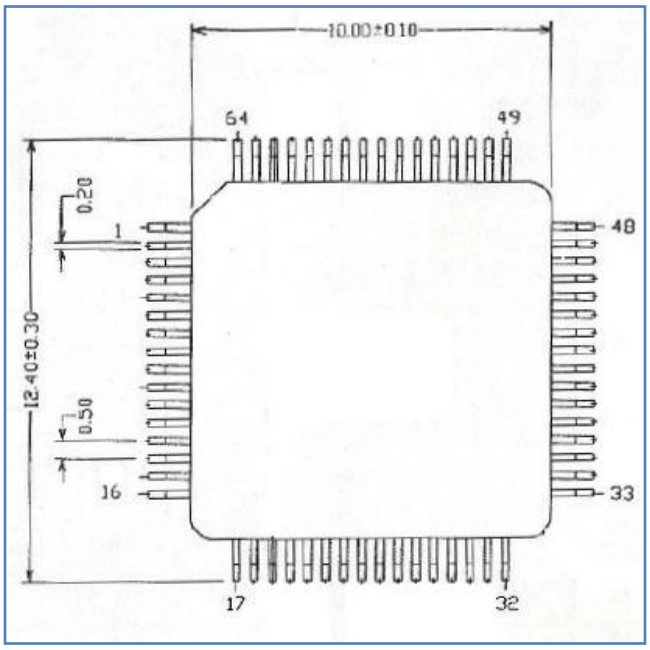

Figure-14: Package Drawing

Revision History			
S.No.	**Version**	**Date of release**	**Description**
1	1.0	October 20, 2022	
2			
3			
4			

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