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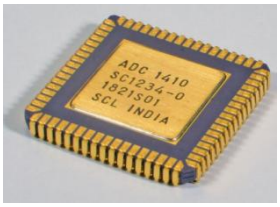


SCL-FEB 2022, VERSION 1

14-BIT, 10 MSPS PIPELINE ANALOG TO DIGITAL CONVERTER

FEATURES:

- **Resolution: 14Bits**
- **No missing code Guaranteed**
- **Output Data Format :Straight Binary**
- **On Chip Voltage References**
- **Operating Voltage: 3.3V**
- **Power Consumption < 250mW**
- **Input Range :2Vp-p Differential /Single Ended**
- **Power Down Mode**
- **Data Latency: 7 Clock Cycles**
- **Radiation hardened (TID) up to 150Krad(Si)**
- **Technology: 0.18µm SCL CMOS Standard Logic Process**
- **Package:68 PIN CQFJ**
- **θ_{jc} Jc: 2.06 ^{o}C/W**

DESCRIPTION

The 14-bit 10-MSPS is a monolithic CMOS analog-to-digital converter capable of converting analog input signals into 14-bit digital word at 10 Mega samples per second (MSPS) and designed for imaging applications. This converter uses a differential, pipeline architecture with digital error correction. Operating on a single 3.3V power supply, device achieves > 13-bits effective resolution at nyquist rate and consumes <250mW power. The Power Down feature reduces power consumption to <50mW. The differential inputs provide a full scale differential input swing equal to 4 times of V_{REF} (4*(CAPTE-CAPBE)). Full scale input range is recommended for optimum performance. The ASIC is fabricated in 0.18µm SCL CMOS Standard Logic Process

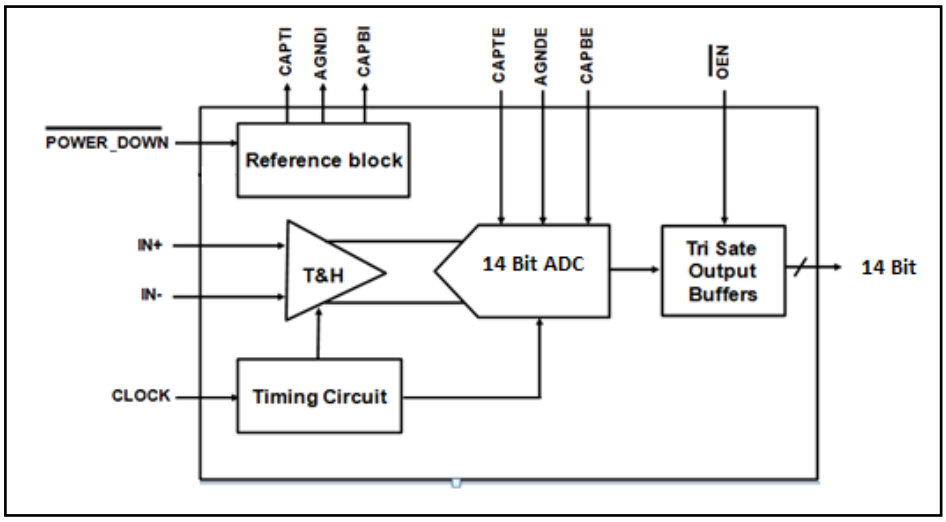


Fig 1: Block Diagram

DEVICE SUMMARY:

Reference	Package	Pins	Lead Finish
SC1234-0	CQFJ	68	Gold

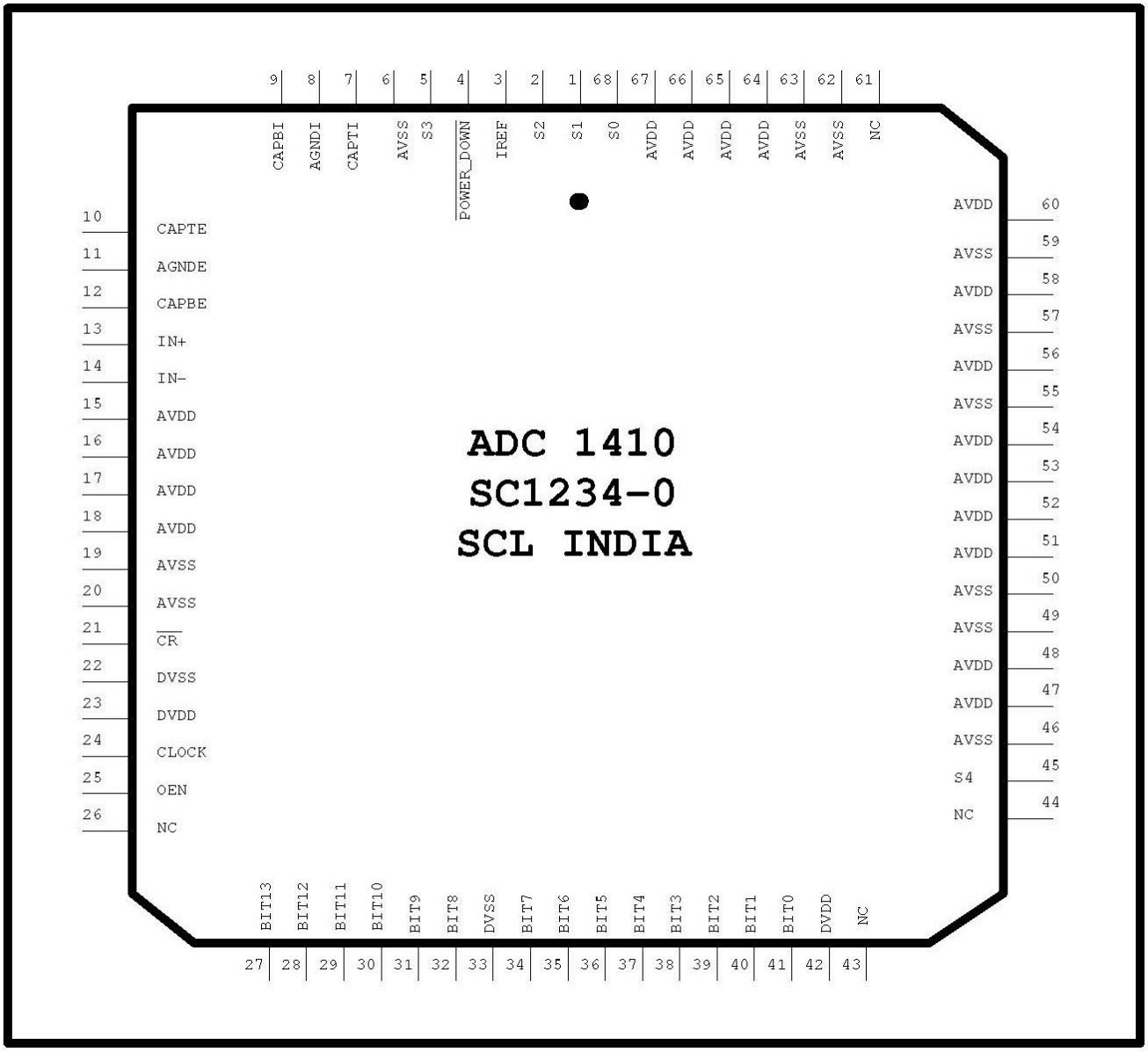


Fig 2: Pin Configuration

PIN DESCRIPTIONS:

PIN NO.	PIN NAME	PIN TYPE	DESCRIPTION
3, 5,6, 19, 20, ,45,46, 49, 50, 55, 57, 59, 62, 63	AVSS	AP	Analog Negative Supply (0 V)
4	$\overline{\text{POWER\_DOWN}}$	DI	Power Down PIN (Active Low)
7	CAPTI	AO	Internal ADC Top Reference Voltage
8	AGNDI	AO	Internal common mode Analog Ground
9	CAPBI	AO	Internal ADC Bottom Reference Voltage
10	CAPTE	AI	External ADC Top Reference Voltage
11	AGNDE	AI	External common mode Analog Ground
12	CAPBE	AI	External ADC Bottom Reference Voltage
13	IN+	AI	ADC IN+
14	IN-	AI	ADC IN-
1,2,15,16,17,18,47,48,51,52,53,54, 56,58,60,64,65,66,67,68	AVDD	AP	Analog Positive Supply (+3.3 V)
21	$\overline{\text{CR}}$	DI	Clear for internal registers (Active Low)
22,33	DVSS	DP	Digital Negative Supply (0 V)
23,42	DVDD	DP	Digital positive Supply (3.3 V)
24	CLOCK	DI	ADC Sampling Clock
25	$\overline{\text{OEN}}$	DI	Output enable (Active Low)
27	BIT13	DO	ADC digital output Bit (MSB)
28	BIT12	DO	ADC digital output Bit
29	BIT11	DO	ADC digital output Bit
30	BIT10	DO	ADC digital output Bit
31	BIT9	DO	ADC digital output Bit
32	BIT8	DO	ADC digital output Bit
34	BIT7	DO	ADC digital output Bit
35	BIT6	DO	ADC digital output Bit
36	BIT5	DO	ADC digital output Bit
37	BIT4	DO	ADC digital output Bit
38	BIT3	DO	ADC digital output Bit
39	BIT2	DO	ADC digital output Bit
40	BIT1	DO	ADC digital output Bit
41	BIT0	DO	ADC digital output Bit (LSB)
26,43,44,61	NC		Internally Not Connected

- TYPE: AI = Analog Input, AO = Analog Output, DI = Digital Input, DO = Digital Output, DP = Digital Power Supply,
  AP = Analog Power Supply.
- Pin 1, 2, 68 are not actual AVDD pins. These pins require logic 1, so it is connected to AVDD.
- Pin 3, 5, 45 are not actual AVSS pins. These pins require logic 0, so it is connected to AVSS.

ELECTRICAL SPECIFICATIONS:

All typical specifications are at T_A = 25°C, all power supply voltages = 3.3 V, conversion rate 10MSPS, with differential input unless otherwise stated. All specifications are assured across operating temperature and voltage ranges. Typical values are at 25°C, Min and Max values are measured across -55°C to 125°C.

Parameters	Test Conditions	Min.	Typ.	Max.	Units
POWER SUPPLY					
AVDD Analog supply voltage		2.97	3.3	3.63	V
DVDD Digital supply voltage		2.97	3.3	3.63	V
AVDD Operating current		33	44	52	mA
DVDD Operating current		20	22	23	mA
POWER DISSIPATION	Normal Mode	180	218	250	mW
	Power Down Mode			50	mW
EXTERNAL REFERENCE					
Positive reference voltage	CAPTE		1.9		V
Negative reference voltage	CAPBE		1.4		V
Common Mode Voltage	AGNDE		1.65		V
CURRENT REQUIREMENT					
Positive reference voltage	CAPTE	140	152	160	µA
Negative reference voltage	CAPBE	-144	-136	-127	µA
Common Mode Voltage	AGNDE*	-2.01	-1.45	-0.52	mA
INTERNAL REFERENCE					
Positive reference voltage	CAPTI	1.920	1.947	1.966	V
Negative reference voltage	CAPBI	1.418	1.442	1.460	V
Common Mode Voltage	AGNDI	1.669	1.695	1.711	V
CAPTI- CAPBI	CAPTI- CAPBI	0.498	0.504	0.507	V
INTERNAL REFERENCE DRIFT	CAPTI- CAPBI	-23	-7	10	ppm/°c
DIGITAL INPUT					
V_{IH} : Logic-high input voltage		2.0		DVDD	V
V_{IL} : Logic-low input voltage		0		0.8	V
I_{IH} : Logic-high input current		-10	-0.9	10	µA
I_{IL} : Logic-low input current		-10	1	10	µA
Input capacitance			5		pF
DIGITAL OUTPUT					
V_{OH} : Logic-high output voltage	@5mA I_{OH}	2.4	3.28	3.3	V
V_{OL} : Logic-low output voltage	@5mA I_{OL}	0	.06	0.4	V
Output load capacitance	@10MHz		10		pF

*** In Power Down mode AGNDE will sink ~10mA.**

ELECTRICAL SPECIFICATIONS (CONTINUED):

Parameters	Test Conditions	Min.	Typ.	Max.	Units
Resolution				14	Bits
Conversion rate		1		10	MSPS
Input Range			2		Vpp
No missing codes			Guaranteed		
Data latency			7		Clocks
Offset Error		-28	66	112	LSB
Gain Error		-1.4	-0.04	0.05	% FS
Input referred noise		1.41	1.44	1.52	LSB
Effective resolution		13.39	13.47	13.50	Bit
Analog Input capacitance (IN+,IN-)			10		pF

ABSOLUTE MAXIMUM RATINGS*

Parameters	With respect To	Min.	Max.	Units
VINP, VINN, CAPTE, CAPBE	AVSS	-0.3	AVDD	V
Digital Inputs	AVSS	-0.3	AVDD	V
AVDD	AVSS	-0.3	3.9	V
DVDD	DVSS	-0.3	3.9	V
AVSS	DVSS	-0.3	0.3	V
Digital Outputs	DVSS	-0.3	DVDD	V
Storage Temperature		-65	150	ºC
Lead Temperature (10 Sec)			300	ºC
ESD Tolerance (HBM)			> 1000	V
Latch Up Protection			100	mA

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

SWITCHING SPECIFICATIONS

All typical specifications are at T_A = 25°C, all power supply voltages = 3.3 V, and conversion rate = 10 MSPS, unless otherwise stated.

Switching Specifications

Parameter	Min	Typ	Max	Units
Conversion Rate	1		10	MSPS
CLK Period		100		ns
CLK Pulse Width High		50		ns
CLK Pulse Width Low		50		ns
Output Delay(t_{od})		6.5		ns

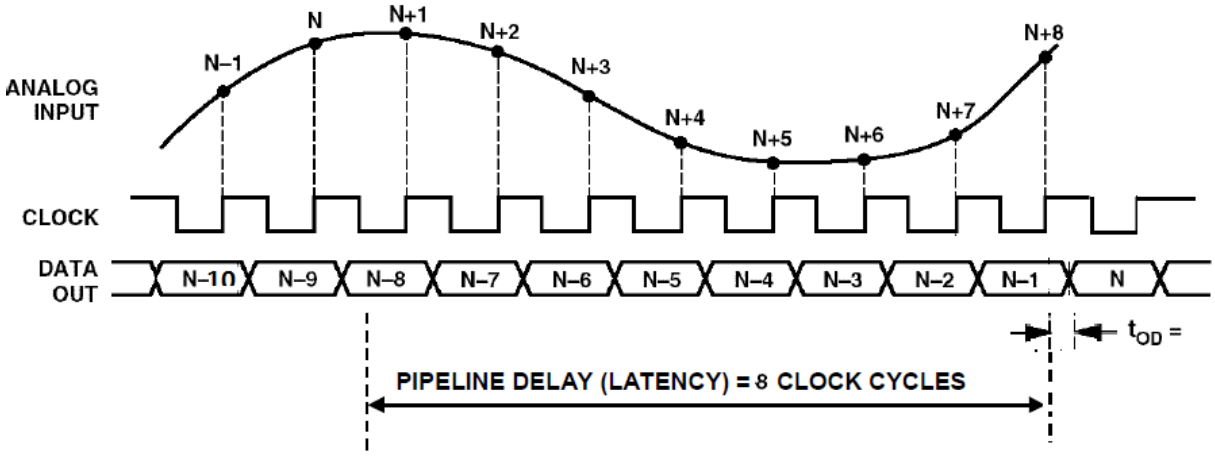


Fig 3: Timing Diagram

TYPICAL CHARACTERISTICS:

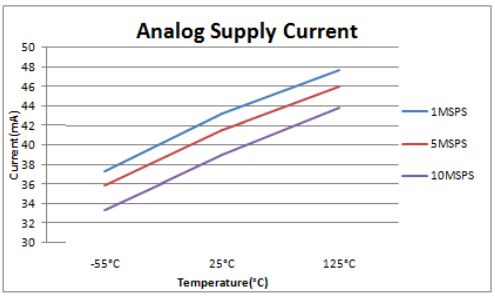


Fig 4: Analog Supply Current

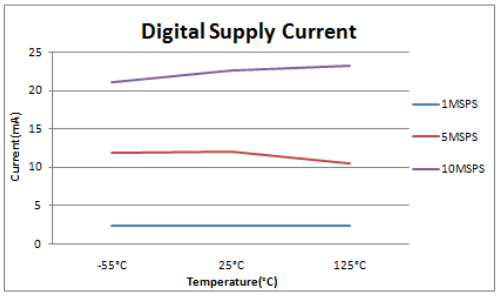


Fig 5: Digital Supply Current

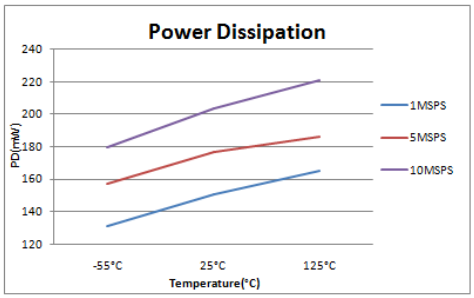


Fig 6: Power Dissipation

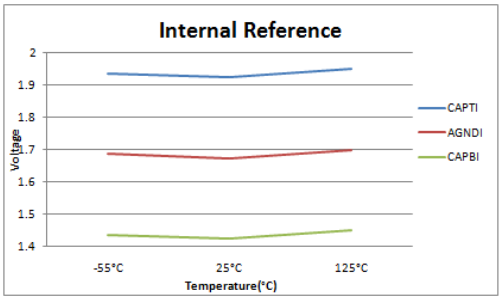


Fig 7: Internal Reference

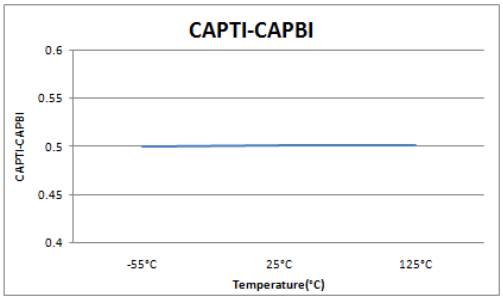


Fig 8: CAPTI-CAPBI

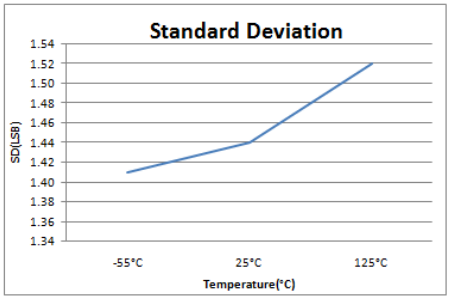


Fig 9: Standard Deviation (LSB)

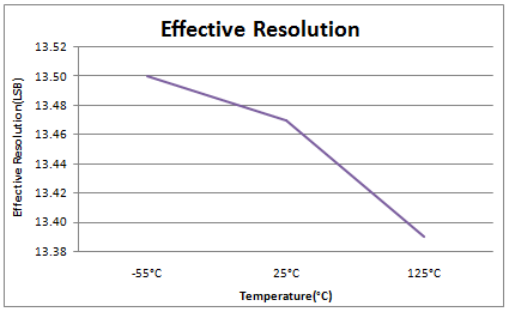


Fig 10: Effective Resolution (Bits)

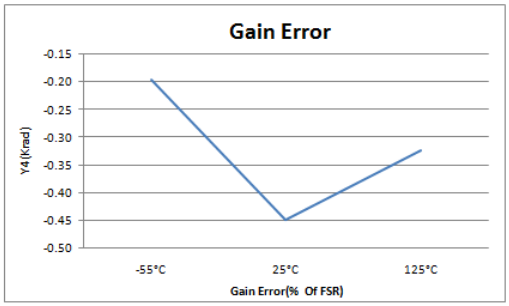


Fig 11: Gain Error (% of FSR)

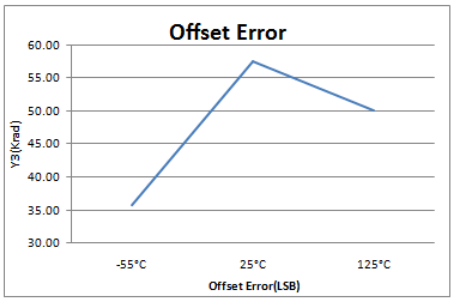
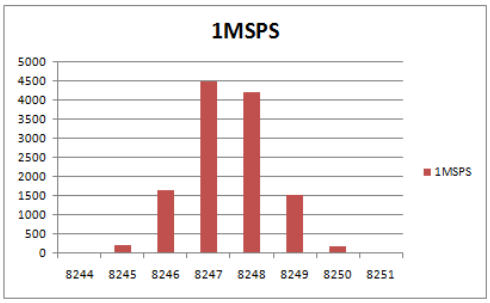
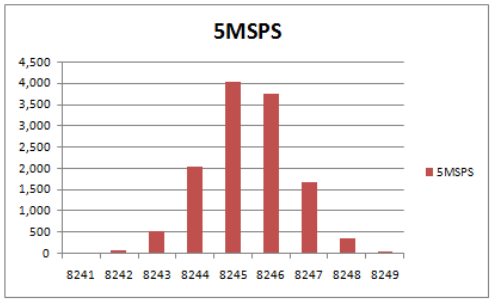


Fig 12: Offset Error (LSB)





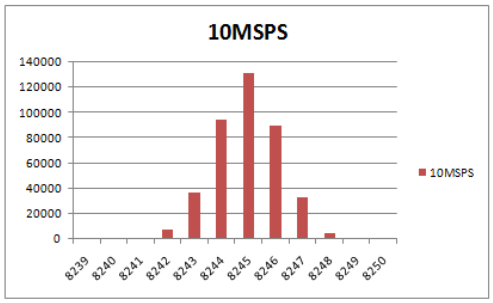


Fig 13: Histogram plot of output codes with analog inputs grounded (IN+ and IN- =1.65V)

OVERVIEW

Pipeline architecture is suitable for 14-bits resolution and 10-MSPS speed. This Analog to digital converter is implemented with 13-stage pipeline architecture. The design is based on switch capacitor (SC) circuitry. The pipeline converter architecture consists of high speed, low resolution cascaded stages to obtain a final conversion. The output of each stage is digitally corrected to obtain an accurate digital output. The pipeline architecture has an inherent sampling latency i.e. few initial clock cycles are required before the first digital conversion is completed. Because imaging signals are rarely pure sine waves, classical converter specifications such as SNR and signal-to-noise-and-distortion (SINAD) are not directly applicable to an imaging system. Instead, SNR can be defined in a somewhat different manner, based on wideband noise. The wideband noise of an ADC can be measured by using a "fixed-input histogram" test. In an ideal system, a fixed input should produce a single output code. Noise in the system will produce a range of codes; from their distribution, the rms noise value can be statistically calculated and then effective resolution can be calculated.

ANALOG INPUT (IN+, IN-)

In differential ended, 2Vpp input range means, IN+ (Pin no. 13) will vary from 1.15 to 2.15 and at the same time IN- (Pin no. 14) will vary from 2.15 to 1.15V. In Single ended, 2Vpp input range means, IN+ (Pin no.13) will vary from 0.65 to 2.65 (if common mode level is 1.65V) and at the same time IN- (Pin no. 14) will connect to common mode level of 1.65V.

THREE-STATE OUTPUTS

The digital outputs of the SC1234-0 can be placed in a high impedance state by setting $\overline{\text{OEN}}$ signal HIGH.

REFERENCE VOLTAGES

ADC1410 (SC134-0) features in-built internal reference voltages. To use internal reference voltages, CAPTI, AGNDI and CAPBI pins should be connected to CAPTE, AGNDE and CAPBE, respectively with suitable bypass capacitors. Temperature coefficient for internal voltage reference is approximately 100ppm/°C in the temperature range of -55°C to 125°C. Depending on the application requirements it might be advantageous to operate the ADC with an external reference voltage. This will improve the DC accuracy if the external reference circuitry is superior in its drift and accuracy.

CLEAR OPERATION

The $\overline{CR}$ PIN is used to clear all the internal resistors. It is active low signal. For the normal mode of operation clear input can be shorted to DVDD.

POWER DOWN MODE

ADC1410 (SC134-0) can be placed in power down mode by setting $\overline{POWER\_DOWN}$ signal LOW. In power down mode AGND current is in the range of <10mA. If $\overline{POWER\_DOWN}$ signal is low complete chip will be in power down mode except voltage reference. To make complete chip in power down $\overline{POWER\_DOWN}$ pin should be connected to DVSS.

DEFINITIONS OF KEY SPECIFICATIONS

- **Differential Nonlinearity (DNL)**

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Therefore, every code must have a finite width. No missing codes guaranteed to 14-bit resolution indicate that all 16384 codes must be present overall operating conditions.

- **Integral Nonlinearity (INL)**

Integral nonlinearity refers to the deviation of each individual code from a line drawn from "zero" through "full scale". The point used as "zero" occurs 1/2 LSB before the first code transition. "Full scale" is defined as a level $1\frac{1}{2}$ LSB beyond the last code transition. The deviation is measured from the centre of each particular code to the true straight line.

- **Total Output Noise**

The rms output noise is measured using histogram techniques. The standard deviation of the ADC output codes is calculated in LSB and represents the rms noise level of the total signal chain . The output noise can be converted to an equivalent voltage, using the relationship

$$1\ \text{LSB} = (\text{ADC full scale} / 2^N\ \text{codes})$$

Where N is resolution of the ADC. 1 LSB is approximately 122 μV.

- **Effective Resolution**

The ratio of the full-scale input range to the rms input noise (from grounded input histogram test) is called as effective resolution.

$$\text{Effective resolution} = \log_2\left(\frac{2^N}{\text{rms input noise (LSBs)}}\right)$$

APPLICATION DIAGRAM:

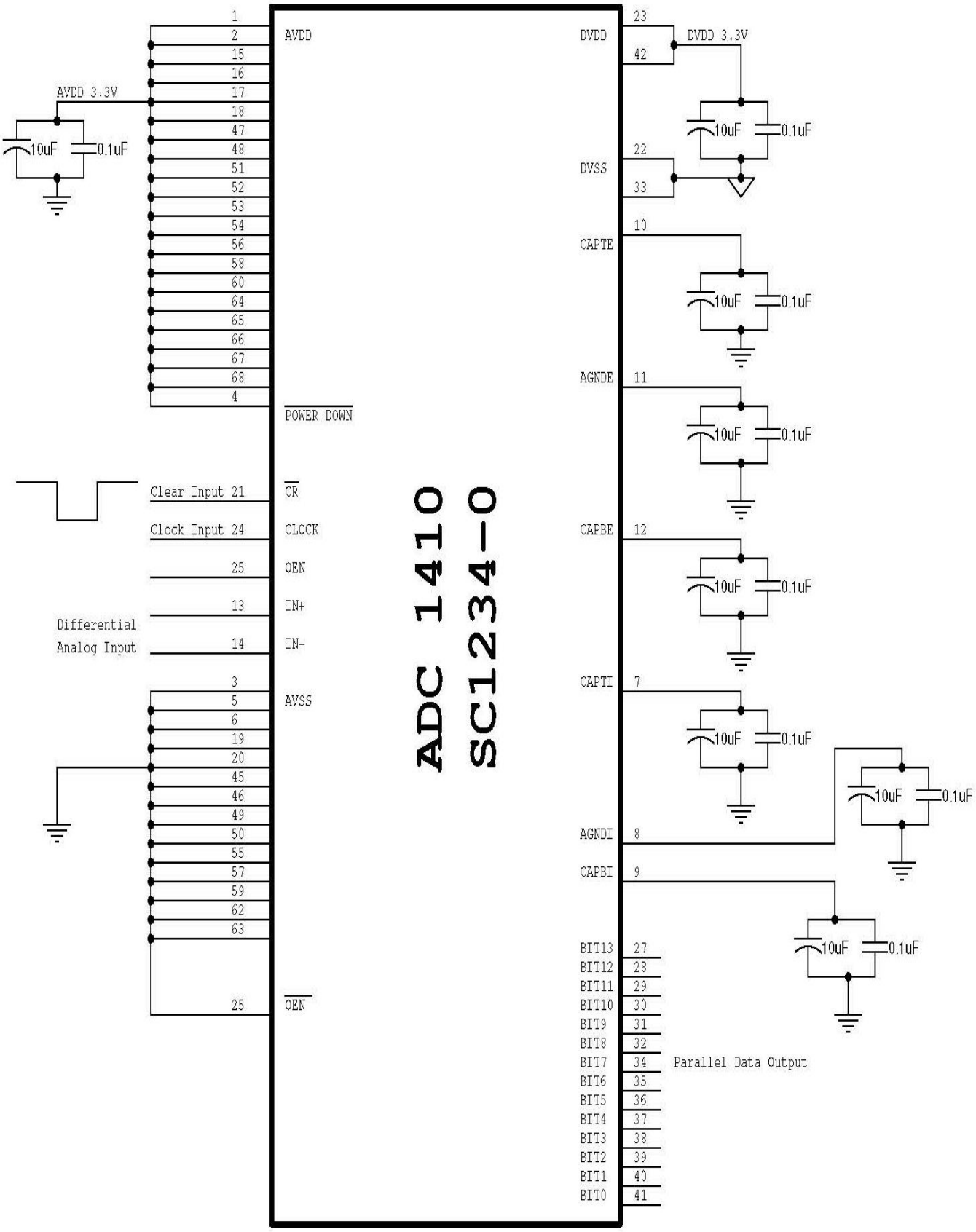


Fig. 16: Application Diagram for normal mode of operation with external reference.

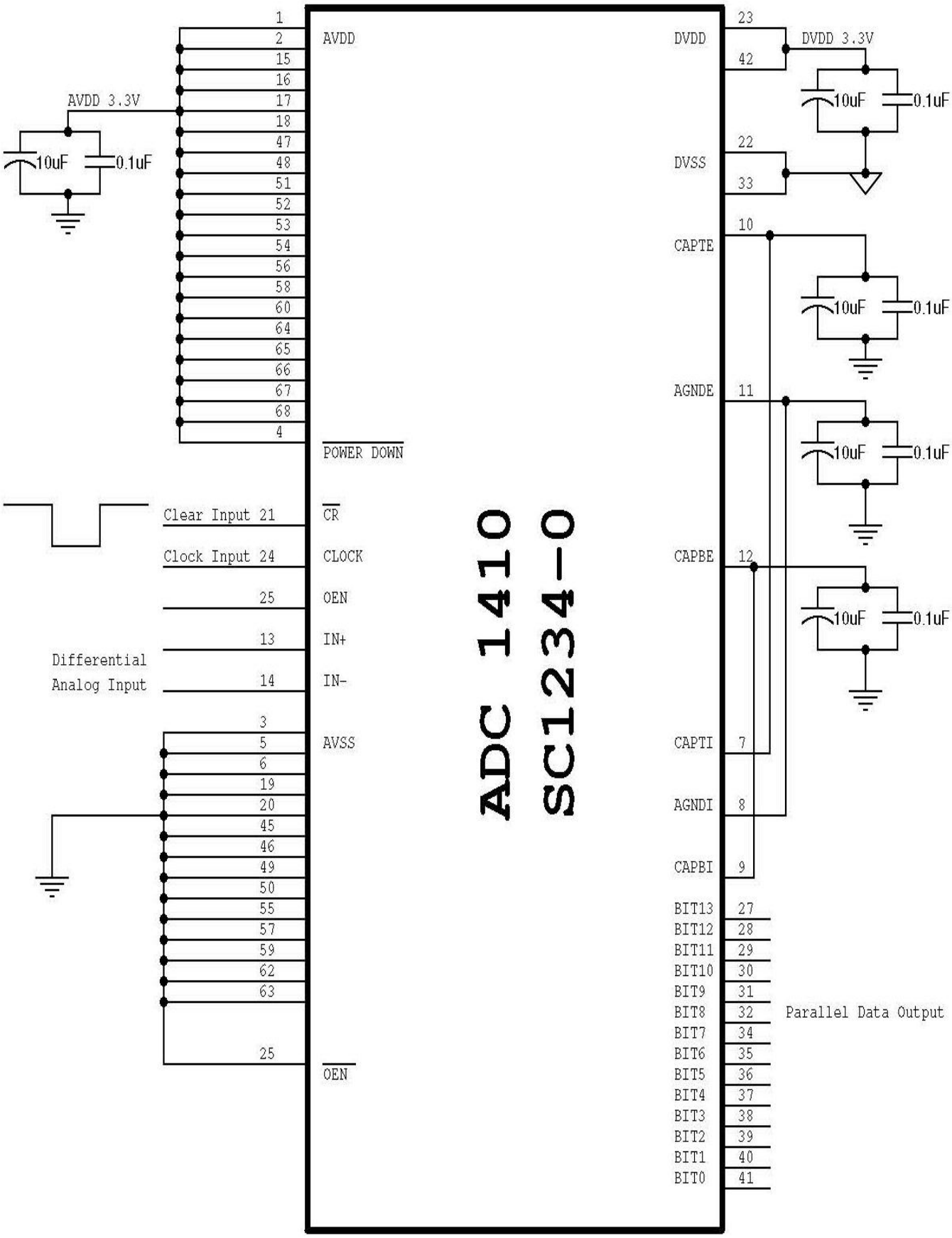
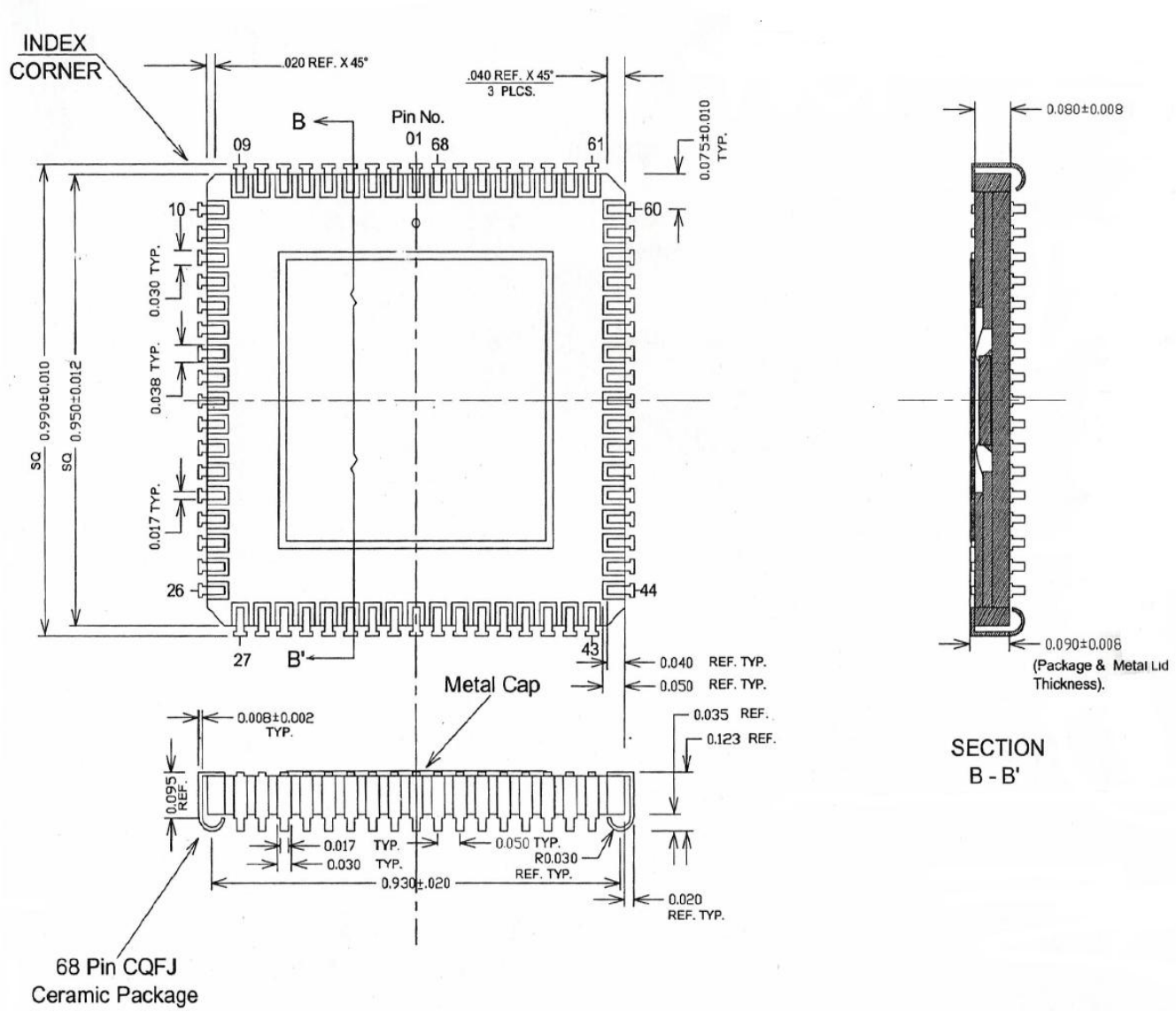


Fig. 17: Application Diagram for normal mode of operation with internal reference

PACKAGE DRAWING (68 Pin CQFJ):

NOTE: All linear dimensions are in inches.



Revision History			
S.No.	**Version**	**Date of release**	**Description**
1	1.0	Feb 01,2021	
2			
3			
4			

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