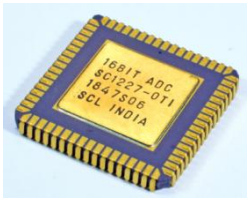
SEMI-CONDUCTOR LABORATORY
SCL, INDIA



SC1227-0T1

PRELIMINARY DATASHEET

January 2023, VERSION 1

16-BIT, 5 MSPS PIPELINE ANALOG TO DIGITAL CONVERTER

FEATURES:

- **Resolution: 16 Bits**
- **No missing code Guaranteed**
- **Output Data Format :Straight Binary**
- **On Chip Voltage References**
- **Operating Voltage: 3.3V**
- **Power Consumption < 130mW**
- **Input Range :2Vp-p Differential /Single Ended**
- **Power Down Mode**
- **Data Latency: 8 Clock Cycles**
- **Radiation hardened (TID) up to 150Krad(Si)**
- **Technology: 0.18µm SCL CMOS Standard Logic Process**
- **Package:68 PIN CQFJ**
- **θ_{jc} : 2.06 ^{o}C/W**

DESCRIPTION:

The 16-bit 5-MSPS is a monolithic CMOS analog-to-digital converter capable of converting analog input signals into 16-bit digital word at 5 Mega samples per second (MSPS) and designed for imaging applications. This converter uses a differential, pipeline architecture with digital error correction. Operating on a single 3.3V power supply, device achieves ≥ 13-bits effective resolution at nyquist rate and consumes < 130mW. The Power Down feature reduces power consumption to <15mW. The differential inputs provide a full scale differential input swing equal to 4 times of V_{REF} (4*(CAPTE-CAPBE)). Full scale input range is recommended for optimum performance. The ASIC is fabricated in 0.18µm SCL CMOS Standard Logic Process.

APPLICATIONS

- **Imaging applications**

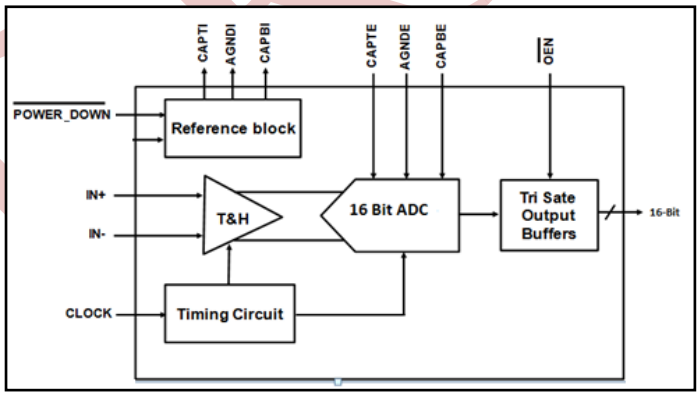


Figure 1: Block Diagram

Table 1: DEVICE SUMMARY:

Reference	Package	Pins	Lead Finish	Junction Temp. Range
SC1227-0T1	CQFJ	68	Gold	-40°C to +125°C

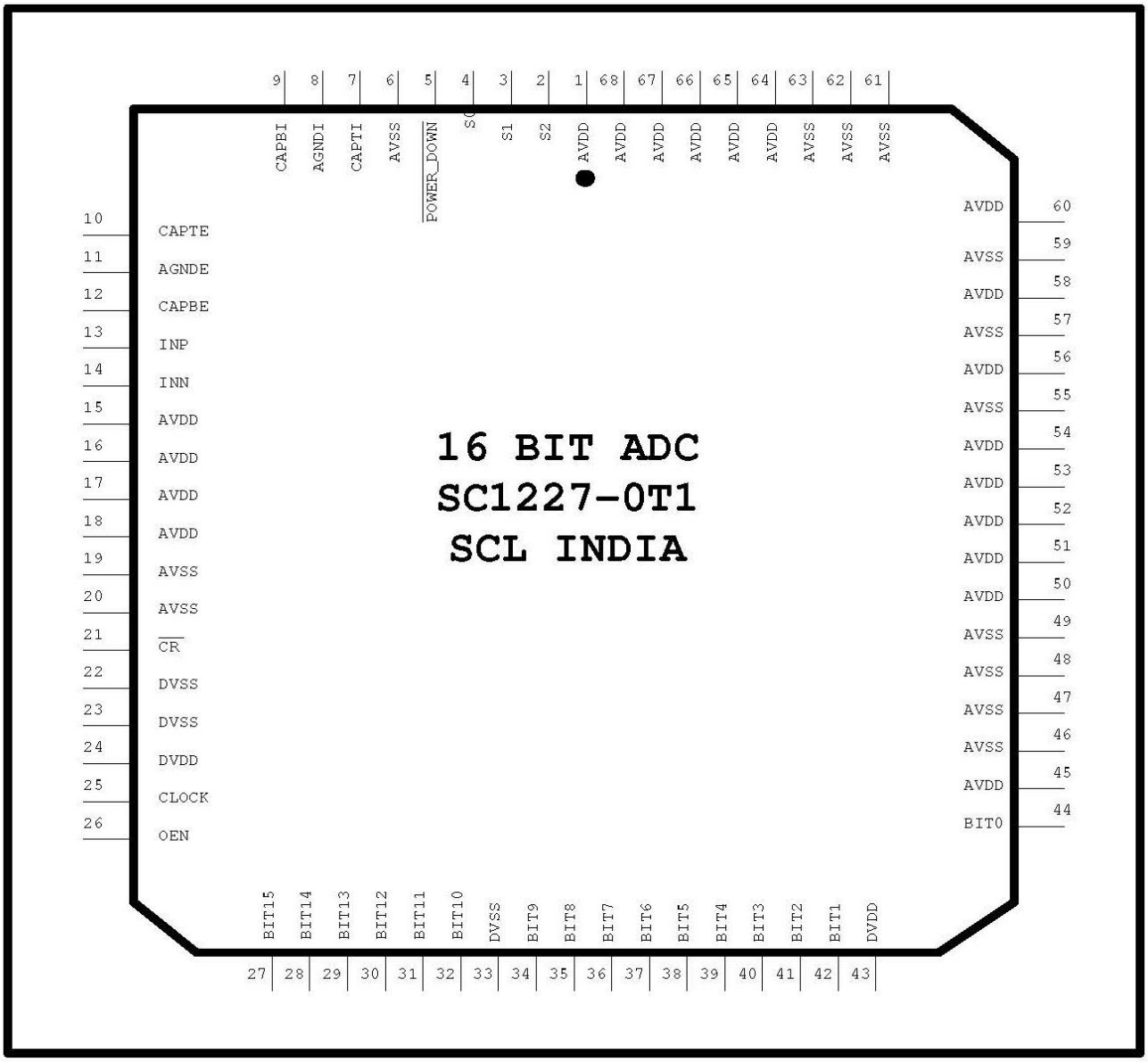


Figure 2: Pin Configuration

Table 2: PIN DESCRIPTIONS

PIN NO.	PIN NAME	PIN TYPE	DESCRIPTION
2,3,4,6,19,20,46,47,48, 49,55,57,59,61,62,63	AVSS	AP	Analog Negative Supply (0 V)
5	$\overline{\text{POWER\_DOWN}}$	DI	Power Down PIN (Active Low)
7	CAPTI	AO	Internal ADC Top Reference Voltage
8	AGNDI	AO	Internal common mode Analog Ground
9	CAPBI	AO	Internal ADC Bottom Reference Voltage
10	CAPTE	AI	External ADC Top Reference Voltage
11	AGNDE	AI	External common mode Analog Ground
12	CAPBE	AI	External ADC Bottom Reference Voltage
13	INP	AI	ADC IN+
14	INN	AI	ADC IN-
1,15,16,17,18,45,50,51,52,53, 54,56,58,60,64,65,66,67,68	AVDD	AP	Analog Positive Supply (+3.3 V)
21	$\overline{\text{CR}}$	DI	Clear for internal registers (Active Low)
22,23,33	DVSS	DP	Digital Negative Supply (0 V)
24,43	DVDD	DP	Digital positive Supply (3.3 V)
25	CLOCK	DI	ADC Sampling Clock
26	$\overline{\text{OEN}}$	DI	Output enable (Active Low)
27	BIT15	DO	ADC digital output Bit (MSB)
28	BIT14	DO	ADC digital output Bit
29	BIT13	DO	ADC digital output Bit
30	BIT12	DO	ADC digital output Bit
31	BIT11	DO	ADC digital output Bit
32	BIT10	DO	ADC digital output Bit
34	BIT9	DO	ADC digital output Bit
35	BIT8	DO	ADC digital output Bit
36	BIT7	DO	ADC digital output Bit
37	BIT6	DO	ADC digital output Bit
38	BIT5	DO	ADC digital output Bit
39	BIT4	DO	ADC digital output Bit
40	BIT3	DO	ADC digital output Bit
41	BIT2	DO	ADC digital output Bit
42	BIT1	DO	ADC digital output Bit
44	BIT0	DO	ADC digital output Bit (LSB)

- PIN Type: AI = Analog Input, AO = Analog Output, DI = Digital Input, DO = Digital Output, DP = Digital Power Supply, AP = Analog Power Supply.
- Pin 2, 3, 4 are not actual AVSS pins. These pins require logic 0, so connected to AVSS.

ELECTRICAL SPECIFICATIONS:

- All typical specifications are at T_A = 25°C, all power supply voltages = 3.3V, and conversion rate 1MSPS, unless otherwise stated.

Table 3: ELECTRICAL SPECIFICATIONS

Parameters	Test Conditions		Min.	Typ.	Max.	Units
POWER SUPPLY						
AVDD Analog supply voltage			2.97	3.3	3.63	V
DVDD Digital supply voltage			2.97	3.3	3.63	V
AVDD Operating current	Normal Mode	1MSPS		23		mA
		5MSPS		24		mA
DVDD Operating current	Normal Mode	1MSPS		2.6		mA
		5MSPS		13.5		mA
POWER DISSIPATION	Normal Mode	1MSPS		87		mW
		5MSPS		125		mW
	Power Down Mode			15		mW
EXTERNAL REFERENCE						
Positive reference voltage	CAPTE			1.9		V
Negative reference voltage	CAPBE			1.4		V
Common Mode Voltage	AGNDE			1.65		V
CURRENT REQUIREMENT						
Positive reference voltage	CAPTE			100	150	µA
Negative reference voltage	CAPBE			150	-140	µA
Common Mode Voltage	AGNDE*			-1		mA
INTERNAL REFERENCE						
Positive reference voltage	CAPTI			1.9080		V
Negative reference voltage	CAPBI			1.4090		V
Common Mode Voltage	AGNDI			1.6591		V
CAPTI- CAPBI	CAPTI- CAPBI			0.4989		V
DIGITAL INPUT						
V_{IH} : Logic-high input voltage			2.0		DVDD	V
V_{IL} : Logic-low input voltage			0		0.8	V
I_{IH} : Logic-high input current			-10	-0.9	10	µA
I_{IL} : Logic-low input current			-10	1	10	µA
Input capacitance				5		pF
DIGITAL OUTPUT						
V_{OH} : Logic-high output voltage	@100 µA I_{OH}		2.4	3.28	3.3	V
V_{OL} : Logic-low output voltage	@100 µA I_{OL}		0	.06	0.4	V
Output load capacitance	@5MHz			10		pF

* In power down mode AGND current is in the range of -3mA.

ELECTRICAL SPECIFICATIONS (CONTINUED):

All typical specifications are at T_A = 25°C, all power supply voltages = 3.3 V, and conversion rate = 1MSPS, unless otherwise stated. All maximum specifications are assured across operating temperature and voltage ranges.

Parameters	Test Conditions	Min.	Typ.	Max.	Units
Resolution				16	Bit
Data latency			8		Clocks
Conversion rate		1		5	MSPS
Input Range			2		Vpp
No missing codes		Guaranteed			
Differential nonlinearity		0.86		1.21	LSB
Gain Error		-1.3		1.1	% FS
Offset Error		-56		96	LSB
Input referred noise	1MSPS		4.43		LSB
	5MSPS		5.14		LSB
Effective resolution	1MSPS		13.85		Bit
	5MSPS		13.63		Bit
AC LINEARITY					
Signal To Noise Ratio (SNR)	Clock =1MHz Test Frequency = 1.0109KHz		68		dB
Total Harmonics Distortion (THD)			-75		dB
Spurious-Free Dynamic Range (SFDR)			76		dB
Signal To Noise And Distortion (SINAD)			51		dB
ENOB			11.03		Bit
Analog Input capacitance (IN+,IN-)			10		pF

Table 4: ABSOLUTE MAXIMUM RATINGS*

Parameters	With respect To	Min.	Max.	Units
VINP, VINN, CAPTE, CAPBE	AVSS	-0.3	AVDD	V
Digital Inputs	AVSS	-0.3	AVDD	V
AVDD	AVSS	-0.3	3.9	V
DVDD	DVSS	-0.3	3.9	V
AVSS	DVSS	-0.3	0.3	V
Digital Outputs	DVSS	-0.3	DVDD	V
Storage Temperature		-65	150	ºC
Lead Temperature (10 Sec)			300	ºC
ESD Tolerance (HBM)			> 1000	V
Latch Up Protection			100	mA

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

SWITCHING SPECIFICATIONS

All typical specifications are at T_A = 25°C, all power supply voltages = 3.3 V, and conversion rate = 1MSPS, unless otherwise stated.

Table 5: SWITCHING SPECIFICATIONS

Parameter	Min	Typ	Max	Units
Conversion Rate	1	1	5	MSPS
CLK Period		1000		ns
CLK Pulse Width High		500		ns
CLK Pulse Width Low		500		ns
Output Delay(t_{od})		7.3		ns

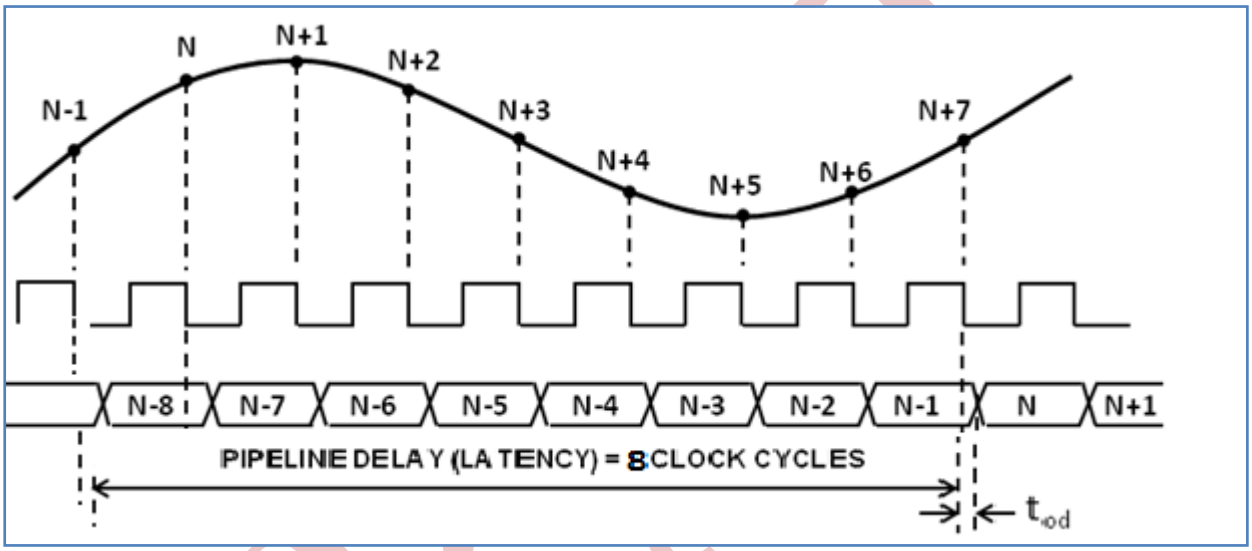


Figure 3: Timing Diagram

OVERVIEW

Pipeline architecture is suitable for 16-bits resolution and 5-MSPS speed. This Analog to digital converter is implemented with 15-stage pipeline architecture. The design is based on switch capacitor (SC) circuitry. The pipeline converter architecture consists of high speed, low resolution cascaded stages to obtain a final conversion. The output of each stage is digitally corrected to obtain an accurate digital output. The pipeline architecture has an inherent sampling latency i.e. few initial clock cycles are required before the first digital conversion is completed. Because imaging signals are rarely pure sine waves, classical converter specifications such as SNR and signal-to-noise-and-distortion (SINAD) are not directly applicable to an imaging system. Instead, SNR can be defined in a somewhat different manner, based on wideband noise. The wideband noise of an ADC can be measured by using a "fixed-input histogram" test. In an ideal system, a fixed input should produce a single output code. Noise in the system will produce a range of codes; from their distribution, the rms noise value can be statistically calculated and then effective resolution can be calculated.

ANALOG INPUT (IN+, IN-)

In differential ended, 2Vpp input range means, IN+ (Pin no. 13) will vary from 1.15V to 2.15V and at the same time IN- (Pin no. 14) will vary from 2.15V to 1.15V. In Single ended, 2Vpp input range means, IN+ (Pin no.13) will vary from 0.65V to 2.65V (if common mode level is 1.65V) and at the same time IN- (Pin no. 14) will connect to common mode level of 1.65V.

THREE-STATE OUTPUTS

The digital outputs of the SC1227-0T1 can be placed in a high impedance state by setting $\overline{\text{OEN}}$ signal HIGH.

REFERENCE VOLTAGES

SC1227-0T1 features in-built internal reference voltages. To use internal reference voltages, CAPTI, AGNDI and CAPBI pins should be connected to CAPTE, AGNDE and CAPBE, respectively through external analog buffers. Temperature coefficient for internal voltage reference is approx. 100ppm/°C. Depending on the application requirements it might be advantageous to operate the ADC with an external reference voltage. This will improve the DC accuracy if the external reference circuitry is superior in its drift and accuracy.

CLEAR OPERATION

The $\overline{\text{CR}}$ PIN is used to clear all the internal resistors. It is active low signal. For the normal mode of operation clear input can be shorted to DVDD.

POWER DOWN MODE

SC1227-0T1 can be placed in power down mode by setting $\overline{\text{POWER\_DOWN}}$ signal LOW. In power down mode AGND current is in the range of -3mA. If $\overline{\text{POWER\_DOWN}}$ signal is low, complete chip will be in power down mode except voltage reference. To make complete chip in power down $\overline{\text{POWER\_DOWN}}$ should be connected to DVSS.

DEFINITIONS OF KEY SPECIFICATIONS

- **DIFFERENTIAL NONLINEARITY (DNL)**

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Therefore, every code must have a finite width. No missing codes guaranteed to 16-bit resolution indicate that all 65536 codes must be present overall operating conditions.

- **INTEGRAL NONLINEARITY (INL)**

Integral nonlinearity refers to the deviation of each individual code from a line drawn from "zero" through "full scale". The point used as "zero" occurs 1/2 LSB before the first code transition. "Full scale" is defined as a level $1\frac{1}{2}$ LSB beyond the last code transition. The deviation is measured from the centre of each particular code to the true straight line.

- **TOTAL OUTPUT NOISE**

The rms output noise is measured using histogram techniques. The standard deviation of the ADC output codes is calculated in LSB and represents the rms noise level of the total signal chain . The output noise can be converted to an equivalent voltage, using the relationship

$$1\ \text{LSB} = (\text{ADC full scale} / 2^{N}\ \text{codes})$$

Where N is resolution of the ADC. 1 LSB is approximately 30μV.

- **EFFECTIVE RESOLUTION**

The ratio of the full-scale input range to the rms input noise (from grounded input histogram test) is called as effective resolution.

$$\text{Effective resolution} = \log_2\left(\frac{2^{N}}{\text{rms input noise (LSBs)}}\right)$$

APPLICATION DIAGRAM:

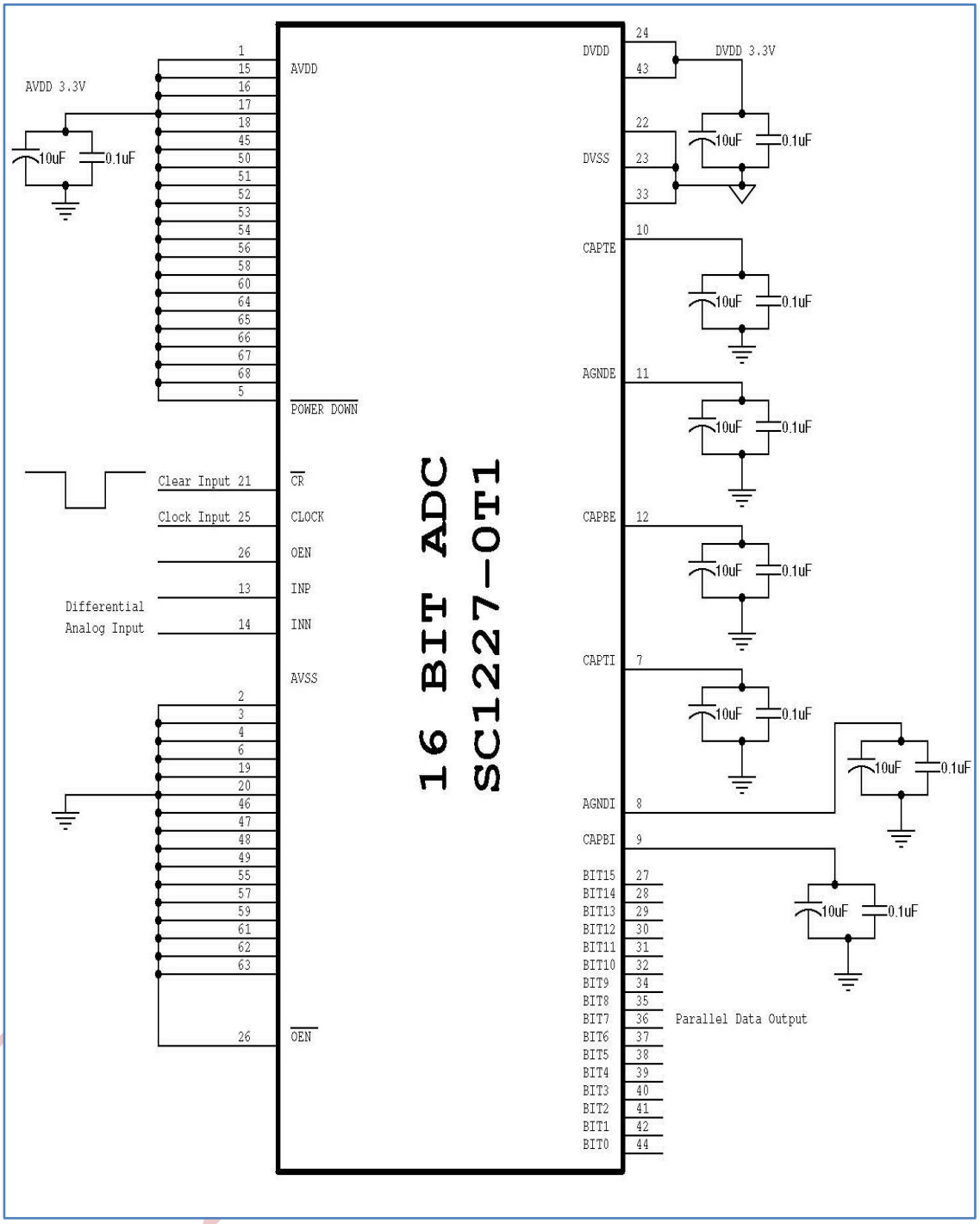


Figure 4: Application Diagram for normal mode of operation with external reference.

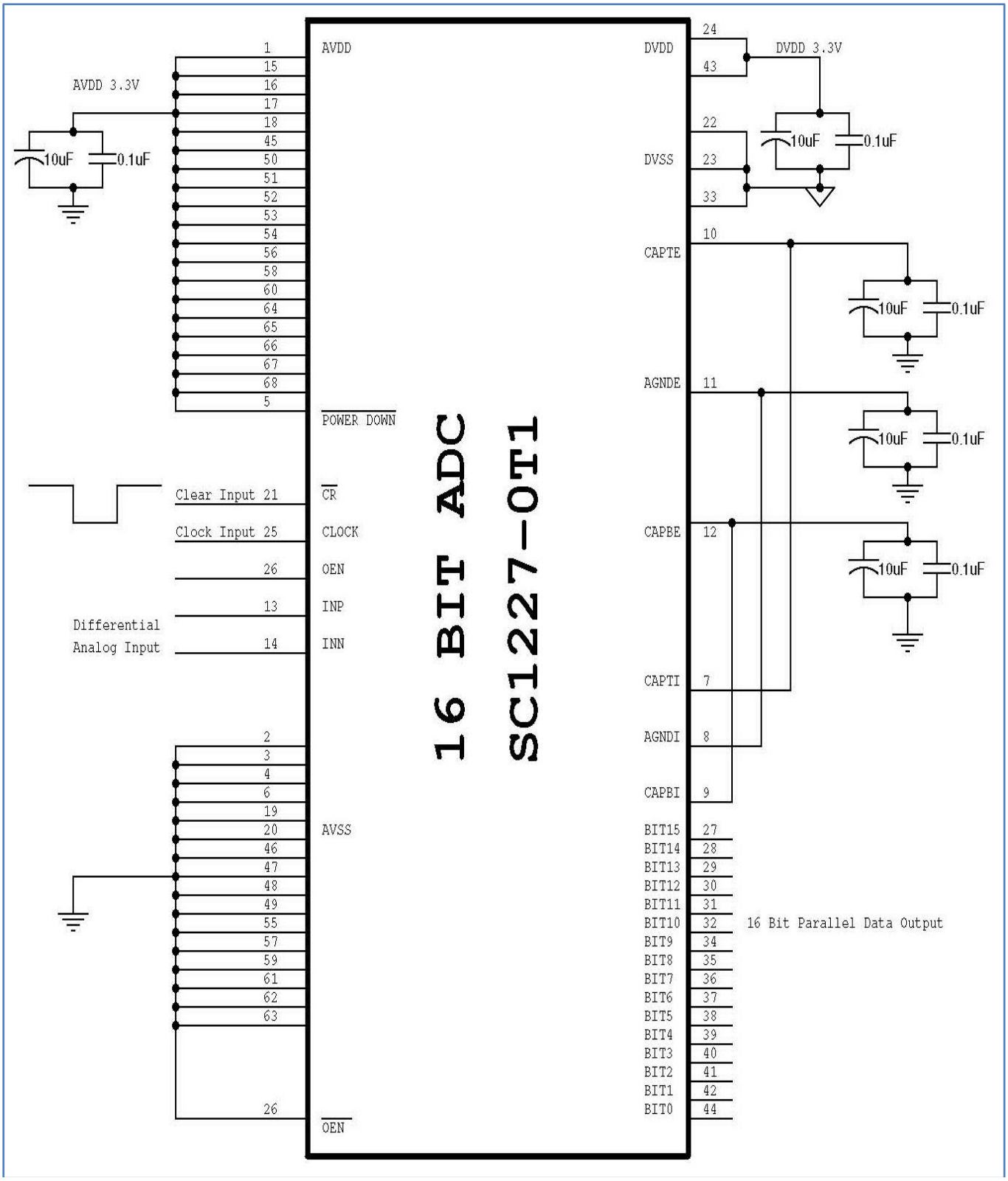


Figure 5: Application Diagram for normal mode of operation with internal reference

PACKAGE DRAWING (68 Pin CQFJ):

NOTE: All linear dimensions are in inches.

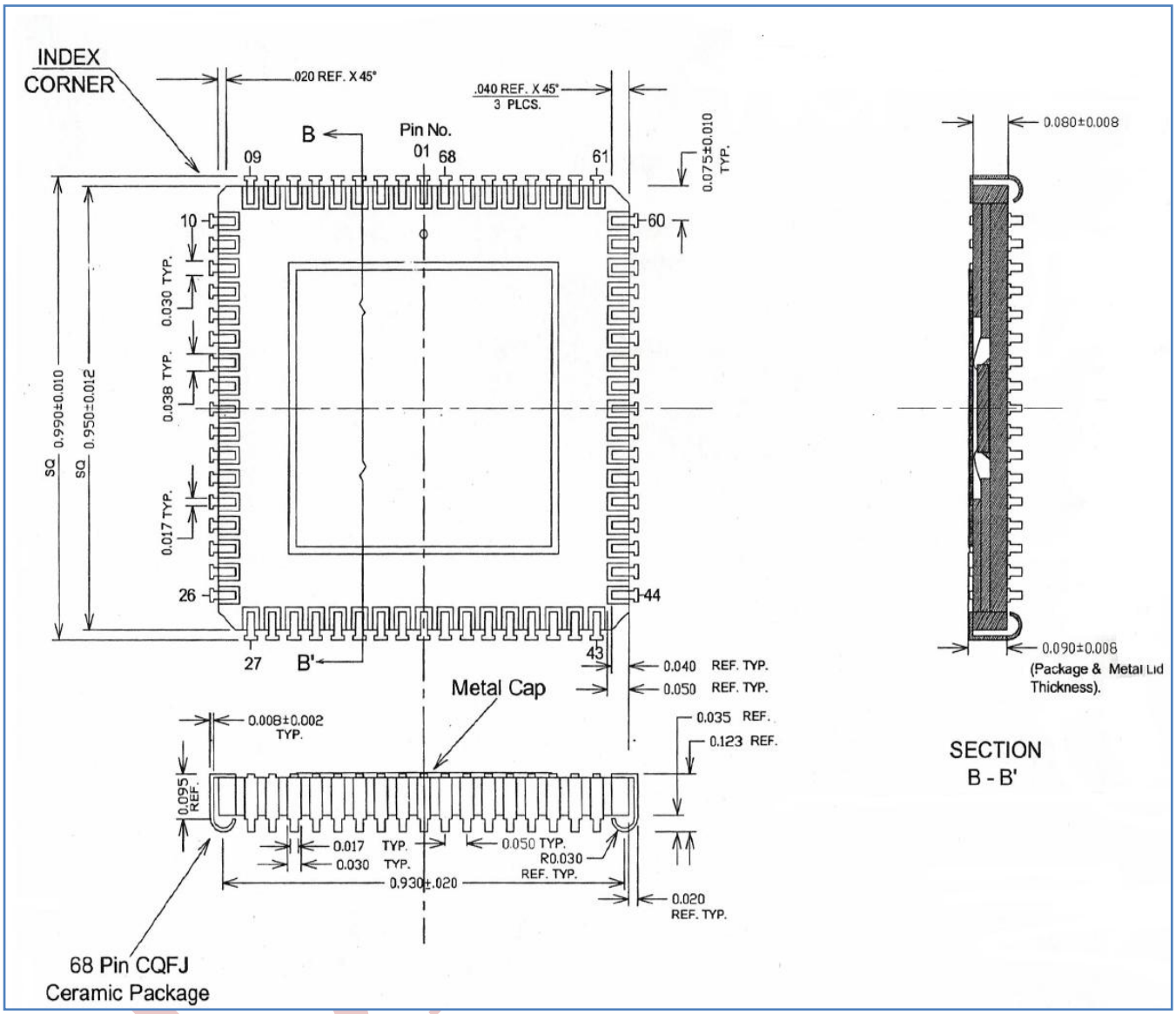


Figure 6: PACKAGE DRAWING

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