SC1221-0

SCL –DEC 2018

16 Channels Simultaneous Sampling 24 Bit Sigma Delta-ADC (Multi-Core RDAS)

FEATURES:

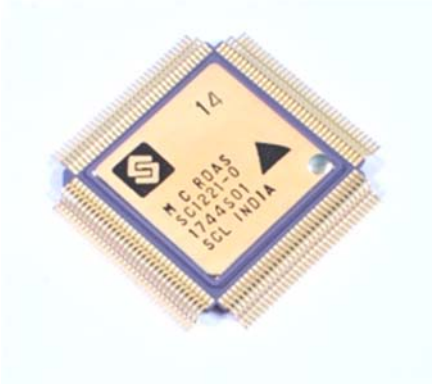
- **Sixteen ΣΔ ADCs**
  - **24 Bits resolution**
  - **No missing code[1]**
  - **PGA from 1 to 128 (Binary Steps)**
  - **Programmable Data Rate upto 9.76 KHz[2]**
  - **0.0045% INL**
  - **19 Bits ENOB (PGA = 1, OSR=2047)**
  - **On-chip Offset and Gain Calibrations**
  - **Over Range Detection**
  - **Data Format Selection**
- **Thirty Two IDACs**
  - **8 Bits resolution**
  - **Programmable Full Scale Ranges of 0.5 mA, 1mA and 2mA.**
- **Precision on-chip 1.22V Reference Accuracy: 1.7%, Drift: ±40ppm**
- **On Chip 1.8V Voltage Regulator**
- **Program and Flight Mode Operation**
- **SPI Compatible**
- **3.0V TO 3.6V**

DESCRIPTION:

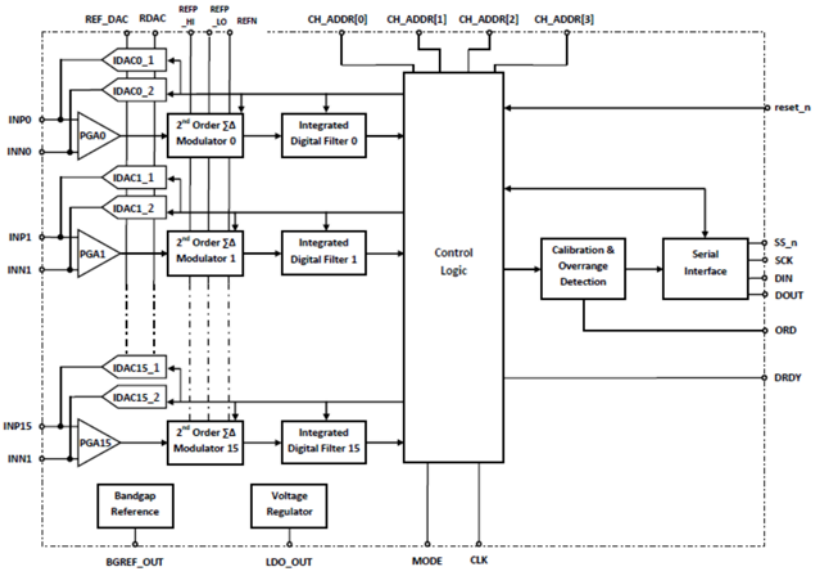
Multi-Core Reconfigurable Data Acquisition System (Multi-Core RDAS) is a fully integrated data acquisition system. It incorporates 16 high resolution Sigma Delta (ΣΔ) ADCs, 32 Eight Bits IDACs along with the calibration and over-range detection unit for each ΣΔ ADC. User can communicate with any of the ADC through SPI interface using four bits channel address. There are two modes of operation: Program mode and Flight mode. User can select any of the modes through a primary input pin.

Each ΣΔ ADC uses a second order modulator with a Programmable Gain Amplifier (PGA) and on-chip offset and gain calibration. It converts the analog input signal into a digital pulse train whose average duty cycle represents the digitized signal information. The pulse train is then processed by a digital sinc3 filter to produce a digital output. The output data rate of ΣΔ ADC is programmable.

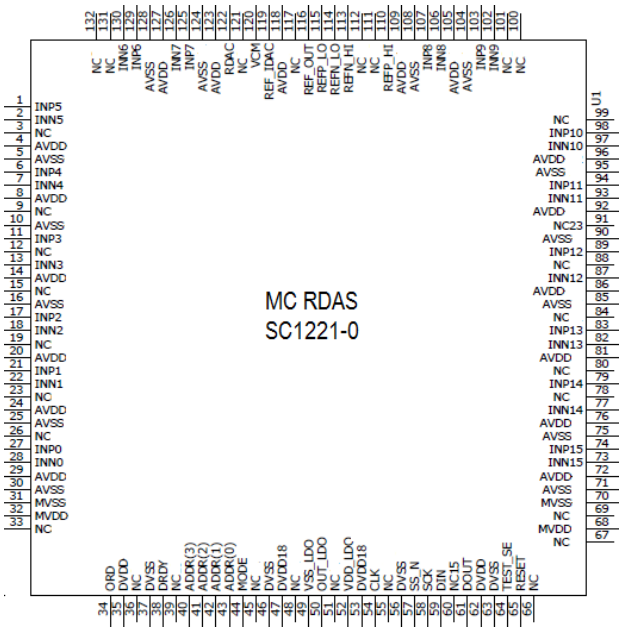
Each 8-bits current DAC is available with three different ranges: 0.5mA, 1mA and 2mA. The device interface is SPI Compatible.



Notes: (1) Tested and verified upto 14 Bits.
(2) 20MHz Clock Input



PIN CONFIGURATION:



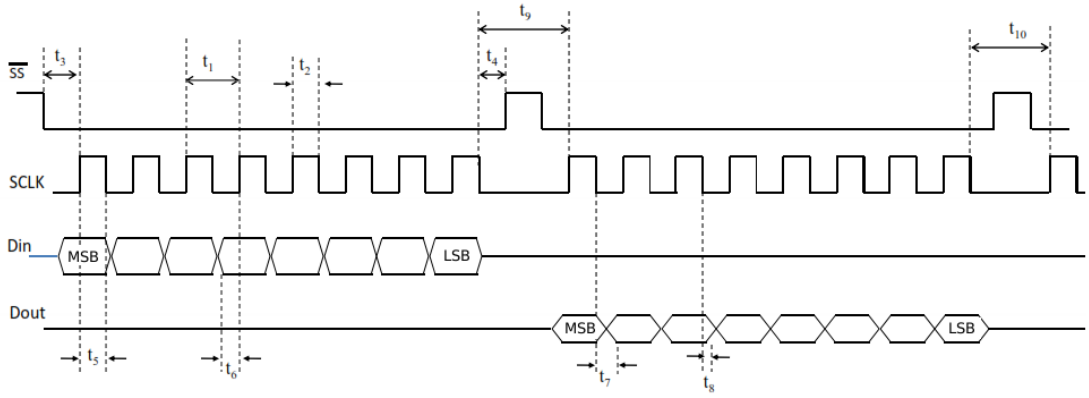
PIN DESCRIPTIONS:

PIN NO.	NAME	DESCRIPTION
1	INP5	Positive Analog Input 5 / Current IDAC5_1 output
2	INN5	Negative Analog Input 5 / Current IDAC5_2 output
3	NC	Not Connected
4	AVDD	Analog Power Supply (3.3 V)
5	AVSS	Analog Ground
6	INP4	Positive Analog Input 4 / Current IDAC4_1 output
7	INN4	Negative Analog Input 4 / Current IDAC4_2 output
8	AVDD	Analog Power Supply (3.3 V)
9	NC	Not Connected
10	AVSS	Analog Ground
11	INP3	Positive Analog Input 3 / Current IDAC3_1 output
12	NC	Not Connected
13	INN3	Negative Analog Input 3 / Current IDAC3_2 output
14	AVDD	Analog Power Supply (3.3 V)
15	NC	Not Connected
16	AVSS	Analog Ground
17	INP2	Positive Analog Input 2 / Current IDAC2_1 output
18	INN2	Negative Analog Input 2 / Current IDAC2_2 output
19	NC	Not Connected
20	AVDD	Analog Power Supply (3.3 V)
21	INP1	Positive Analog Input 1 / Current IDAC1_1 output
22	INN1	Negative Analog Input 1 / Current IDAC1_2 output
23	NC	Not Connected
24	AVDD	Analog Power Supply (3.3 V)
25	AVSS	Analog Ground
26	NC	Not Connected

27	INP0	Positive Analog Input 0 / Current IDAC0_1 output
28	INN0	Negative Analog Input 0 / Current IDAC0_2 output
29	AVDD	Analog Power Supply (3.3 V)
30	AVSS	Analog Ground
31	MVSS	Mixed Signal Ground (Can be connected to AVSS)
32	MVDD	Mixed Signal Supply (3.3V, can be connected to AVDD)
33	NC	Not Connected
34	ORD	Over Range Detection
35	DVDD	Digital I/O Power Supply (3.3 V)
36	NC	Not Connected
37	DVSS	Digital Ground
38	DRDY	Data Ready, Active Low
39	NC	Not Connected
40	CH_ADDR[3]	Channel Address bit 3
41	CH_ADDR[2]	Channel Address bit 2
42	CH_ADDR[1]	Channel Address bit 1
43	CH_ADDR[0]	Channel Address Bit 0
44	MODE	Mode Selection
45	NC	Not Connected
46	DVSS	Digital Ground
47	DVDD18	Digital Core Supply (1.8V)
48	NC	Not Connected
49	VSS_LDO	LDO Ground (Can be connected to DVSS)
50	OUT_LDO	Voltage Regulator Output (1.8V)
51	NC	Not Connected
52	DVDD_LDO	Digital I/O Power Supply (3.3V, can be connected to DVDD)
53	DVDD18	Digital Core Supply (1.8V) (Can be shorted to OUT_LDO)
54	CLK	Master Clock
55	NC	Not Connected
56	DVSS	Digital Ground
57	SS_N	Serial Interface Enable, Active Low
58	SCK	Serial Clock
59	DIN	Serial Data Input
60	NC	Not Connected
61	DOUT	Serial Data Output
62	DVDD	Digital Power Supply (3.3 V)
63	DVSS	Digital Ground (can be connected to DVSS)
64	test_se	Scan Enable Pin. In normal operation, it will be connected to DVSS.
65	reset_n	Reset , Active Low. This is master reset signal.
66	NC	Not Connected
67	NC	Not Connected
68	MVDD	Mixed Signal Supply (3.3V, can be connected to AVDD)
69	NC	Not Connected
70	MVSS	Mixed Signal Ground (Can be connected to AVSS)
71	AVSS	Analog Ground
72	AVDD	Analog Power Supply (3.3 V)
73	INN15	Negative Analog Input 15 / Current IDAC15_2 output
74	INP15	Positive Analog Input 15 / Current IDAC15_1 output
75	AVSS	Analog Ground
76	AVDD	Analog Power Supply (3.3 V)
77	INN14	Negative Analog Input 14 / Current IDAC14_2 output
78	NC	Not Connected
79	INP14	Positive Analog Input 14 / Current IDAC14_1 output

80	NC	Not Connected
81	AVDD	Analog Power Supply (3.3 V)
82	INN13	Negative Analog Input 13 / Current IDAC13_2 output
83	INP13	Positive Analog Input 13 / Current IDAC13_1 output
84	NC	Not Connected
85	AVSS	Analog Ground
86	AVDD	Analog Power Supply (3.3 V)
87	INN12	Negative Analog Input 12 / Current IDAC12_2 output
88	NC	Not Connected
89	INP12	Positive Analog Input 12 / Current IDAC12_1 output
90	AVSS	Analog Ground
91	NC	Not Connected
92	AVDD	Analog Power Supply (3.3 V)
93	INN11	Negative Analog Input 11 / Current IDAC11_2 output
94	INP11	Positive Analog Input 11 / Current IDAC11_1 output
95	AVSS	Analog Ground
96	AVDD	Analog Power Supply (3.3 V)
97	INN10	Negative Analog Input 10 / Current IDAC10_2 output
98	INP10	Positive Analog Input 10 / Current IDAC10_1 output
99	NC	Not Connected
100	NC	Not Connected
101	NC	Not Connected
102	INN9	Negative Analog Input 0 / Current IDAC9_2 output
103	INP9	Positive Analog Input 0 / Current IDAC9_1 output
104	AVSS	Analog Ground
105	AVDD	Analog Power Supply (3.3 V)
106	INN8	Negative Analog Input 0 / Current IDAC8_2 output
107	INP8	Positive Analog Input 0 / Current IDAC8_1 output
108	AVSS	Analog Ground
109	AVDD	Analog Power Supply (3.3 V)
110	REFP_HI	Positive Differential Reference Input High
111	NC	Not Connected
112	NC	Not Connected
113	REFN_HI	Negative Differential Reference Input High
114	REFN_LO	Negative Differential Reference Input Low
115	REFP_LO	Positive Differential Reference Input Low
116	REF_OUT	Output of Band Gap Reference. It must have 0.1µf cap to AVSS.
117	NC	Not Connected
118	AVDD	Analog Power Supply (3.3 V)
119	REF_IDAC	Input Reference Voltage for IDAC
120	VCM	Common mode Voltage Pin. It must have 0.1µf cap to AVSS.
121	NC	Not Connected
122	RDAC	Current DAC Resistor
123	AVDD	Analog Power Supply (3.3 V)
124	AVSS	Analog Ground
125	INP7	Positive Analog Input 7 / Current IDAC7_1 output
126	INN7	Negative Analog Input 7 / Current IDAC7_2 output
127	AVDD	Analog Power Supply (3.3 V)
128	AVSS	Analog Ground
129	INP6	Positive Analog Input 6 / Current IDAC6_1 output
130	INN6	Negative Analog Input 6 / Current IDAC6_2 output
131	NC	Not Connected
132	NC	Not Connected

SPI TIMING SPECIFICATIONS:



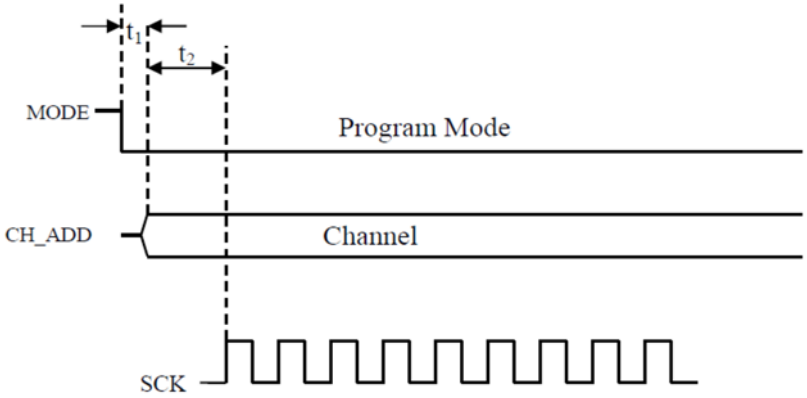
TIMING DIAGRAM

TIMING SPECIFICATION TABLE

SPEC	DESCRIPTION	MIN	MAX	UNIT
t_1	SCLK period	4 cycle		t_{CLK} Period
t_2	SCLK pulse width (High and Low)	2 cycle		t_{CLK} Period
t_3	SS low to first SCLK edge	100		ns
t_4	Last SCLK falling edge to SS HIGH	100		ns
t_5	SCK rising edge to DIN valid (Hold time)	50		ns
t_6	DIN valid to SCLK rising edge (Setup time)	50		ns
t_7	SCLK falling Edge to valid new DOUT		50[2]	ns
t_8	SCLK falling Edge to DOUT, Hold Time	0[3]		ns
t_9	Delay between last SCLK edge of 1st byte transfer and first SCLK edge for subsequent 2nd byte transfer : RREG, WREG Command	10		t_{CLK} Period
t_{10}	Final SCLK edge of one command until first edge SCLK of next command	4		t_{CLK} Period

Notes: (1) DOUT goes immediately into tri-state whenever SS is high,
(2) DOUT pin output load should be less than 20pF
(3) DOUT should be sampled externally on rising edge of SCLK. DOUT will remain valid till next falling edge.

PROGRAMING MODE TIMING SPECIFICATIONS:

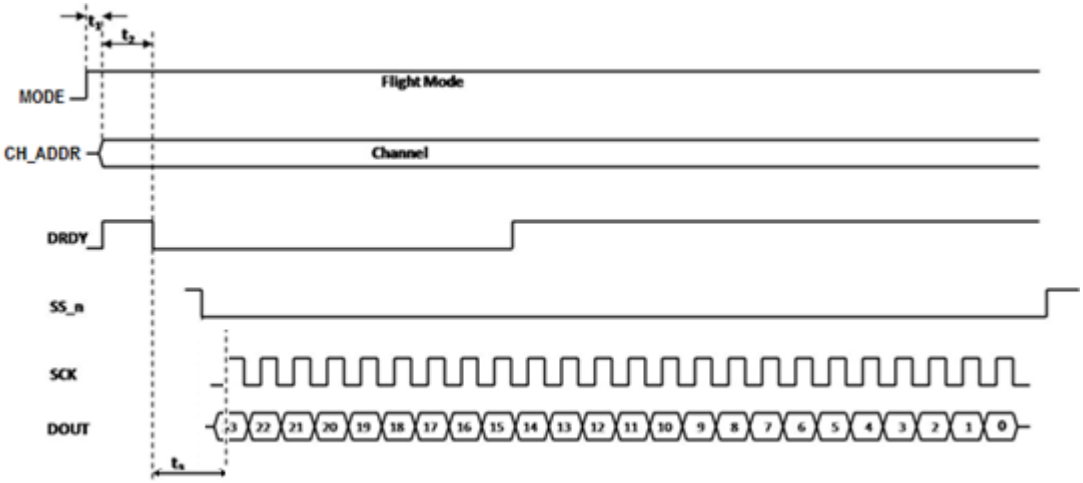


TIMING DIAGRAM

TIMING SPECIFICATION TABLE

SPEC	DESCRIPTION	MIN	MAX	UNIT
t_1	Mode change to channel change	1		t_{clk} period
t_2	Channel Change to First Edge of SCLK	4		t_{clk} period

FLIGHT MODE TIMING SPECIFICATIONS:



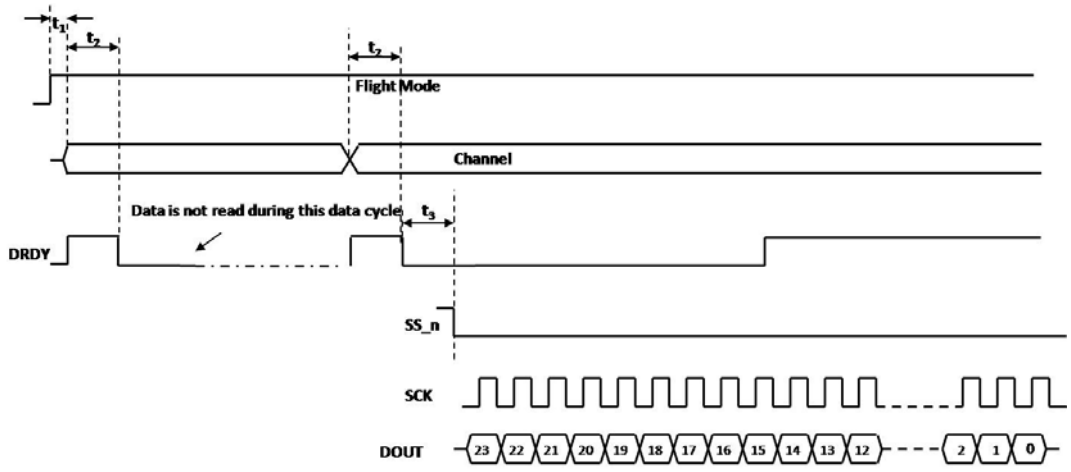
TIMING DIAGRAM

TIMING SPECIFICATION TABLE

SPEC	DESCRIPTION	MIN	MAX	UNIT
t_1	Mode change to channel change	1		t_{clk} period
t_2	Channel Change to DRDY Low	20		t_{clk} period
t_3	DRDY Low to First Edge of SCK	1		t_{clk} period

Notes: (1) It is mandatory read at least two bytes of output data, otherwise DRDY will remain low till next data is available or till next channel change or till next filter clock.
(2) In case filter clock comes during reading of output data, the data will not be updated until SS goes high.

FLIGHT MODE TIMING SPECIFICATIONS:



TIMING DIAGRAM

TIMING SPECIFICATION TABLE

SPEC	DESCRIPTION	MIN	MAX	UNIT
t_1	Mode change to channel change	1		t_{clk} period
t_2	Channel Change to DRDY Low	20		t_{clk} period
t_3	DRDY Low to SS_N LOW	1		t_{clk} period

Notes: In case a channel is selected and no read operation is performed, then DRDY will go high at the change of the channel and remain high for 20 master clock cycles.

ELECTRICAL CHARACTERISTICS

All specifications are at AVDD, DVDD, MVDD = +3.3V, DVDD18=+1.8V, Temp. = 25ºC, OSR=2047, f_{MOD} = 78.125 KHz, f_{CLK} =5MHz, f_{Data} = 38.147 Hz, PGA=1, REFP_HI =2.5V, REFN_HI =0V, R_{DAC}=75K unless otherwise specified.

PARAMETER	TESTS CONDITIONS	SC1221-0			UNITS
		MIN	TYP	MAX	
ADC					
Analog Input Range		0		AVDD	V
Full Scale Input Range	V_{INP}-V_{INN}	-V_{REF}/PGA		+V_{REF}/PGA	V
Programmable Gain Amplifier	User Selectable	1		128	
Input Current (Dynamic)				25	µA
Input Capacitance			32		pF
Bandwidth					
Sinc^3 Filter***	-3dB		0.262*f_{Data}		Hz
Input Impedance			100		KΩ
Resolution		24			Bits
No Missing Code*	OSR=256, f_{CLK} =5MHz, f_{MOD} = f_{CLK} /64	14			Bits
Integral Non-Linearity	Best Fit Method			±0.0045	% of FSR
Offset Error	After Calibration			80	ppm of FSR
Offset Drift	-40ºC to +125ºC			400	ppm of FSR
Gain Error	After Calibration			0.06	% of FSR
Gain Drift	-40ºC to +125ºC			0.1	% of FSR
Effective Number of Bits (ENOB)	Based on 100 samples			19	Bits
Common-Mode Rejection	At DC = 1.65		83		dB
Power Supply Rejection ****	DC, dB = –20 log(∆VOUT /∆VDD)		67		dB
Master Clock Rate	f_{CLK}			20	MHz
ON CHIP VOLTAGE REFERENCE					
Output Voltage	Load Current = 1µA	1.20	1.22	1.24	V
Load Regulation	Full Load =2.5mA			1	%
Drift	-40ºC to +125ºC			40	ppm/ºC
Start up Time***				50	µS
VOLTAGE REFERENCE INPUT					
External High Reference	(REFP_HI)-(REFN_HI)			2.5	V
External Low Reference	(REFP_LO)-(REFN_LO)			1.25	V
POWER SUPPLY REQUIREMENT					
Supply Voltage	AVDD	3.0	3.3	3.6	V
	DVDD	1.62	1.8	1.98	V
Analog Current			25	30	mA
Digital Current	STATIC		0.6	1	mA
Digital Current	DYNAMIC @ F_{CLK}=10MHz		3.2	5	mA
ON CHIP LDO					
Supply Voltage	VDD_LDO	3.0	3.3	3.6	V
Output Voltage	OUT_LDO	1.77	1.80	1.83	V
No Load Current			4.4	4.8	mA
Line Regulation				1	%
Load Regulation	@Full Load Current = 5mA			1	%
Temp Drift	-40ºC to +125ºC			±3	%
IDAC					
Full Scale Output Current	R_{DAC} =75K, Range1		0.5		mA
	R_{DAC} =75K, Range2		1.0		mA
	R_{DAC} =75K, Range3		2.0		mA
Monotonocity		8			Bits

Nonlinearity Mismatch Error Mismatch Error Drift	At Same Range and Code -40ºC to +125ºC		10	1 20 8	%FSR % Set Value % Set Value
TEMPERATURE RANGE Operating		-40		125	ºC

* No missing codes are verified and tested upto 14bits. Device may perform for better results.
*** Simulated Result **** Test results for Core 0.

DIGITAL CHARACTERISTICS

DVDD= 3.0V to 36V

PARAMETER	TESTS CONDITIONS	SC1221-0			UNITS
		MIN	TYP	MAX	
Logic Family			CMOS		
Logic Level: V_{IH}		2		DVDDO	V
V_{IL}		DVSS		0.8	V
V_{OH}	I_{OH}=8mA	3.0			V
V_{OL}	I_{OL}=8mA	DVSS		0.4	V
Input Leakage: I_{IH}	V_I=DVDDO			1	µA
I_{IL}	V_I=DVSS	-1			µA

ABSOLUTE MAXIMUM RATING

PARAMETER	SC1218-0		UNITS
	MIN	MAX	
AVDD to AVSS	-0.3	4.3	V
DVDD to DVSS	-0.3	4.3	V
DVDD18 to DVSS	-0.3	2.2	V
INP, INN	-0.3	AVDD+0.3	V
Digital Input Voltage to DGND	-0.3	DVDDO+0.3	V
Digital Output Voltage to DVSS	-0.3	DVDDO+0.3	V
Digital Output Current		8	mA
Maximum Junction Temperature		125	°C

OVERVIEW

PROGRAMMABLE GAIN AMPLIFIER

The Programmable Gain Amplifier (PGA) can be set to gains of 1, 2, 4, 8, 16, 32, 64, or 128. Adjusting the internal gain of a sigma delta modulator is a technique, which can be used to get an appropriate LSB size for the transducers application. It will improve the resolution of the ADC. The PGA is combined with the ∑Δ modulator.

∑Δ MODULATOR

A second order single loop sigma delta modulator is used in the Sigma Delta ADC. The sigma delta modulator converts the input signal into a digital pulse train whose average duty cycle represents the digitized signal information. The integrators used in the modulator are switched capacitor based. The first integrator of the modulator is auto-zeroed.

There are sixteen different ∑Δ Modulator units in Multi-Core RDAS. Each of modulator units can be programmed independently.

The modulator runs at clock frequency f_{MOD} that can be adjusted by setting the appropriate value of PRE1: PRE0 of CR2 control register as shown in the following table:

PRE1:PRE0	f_{MOD}
00	f_{CLK} /64
01	f_{CLK} /128
10	f_{CLK} /256
11	f_{CLK} /512

Where f_{CLK} is external clock frequency

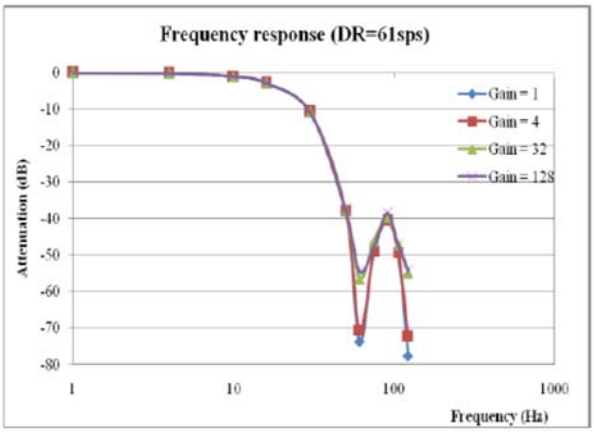
The modulator is designed to work at a maximum sampling frequency of *625 KHz.* All sixteen modulator units run at the same modulator frequency.

INTEGRATED FILTER MODULE

Each of ∑Δ Modulator is followed by an independent integrated digital filter unit. It comprises of $sinc^3$ filter and internal registers. The decimation ratio of each unit of filter module can be programmed independently.

The on-chip digital filter processes the single bit data stream from the corresponding modulator unit using a $sinc^3$ filter. The sinc filters are conceptually simple, efficient and flexible, especially where variable resolution and data rates are required. The output data rate of digital filter is given as:

$$\text{Data Rate} = f_{MOD} / DR$$



The Decimation Ratio (DR) of filter can vary from 20 to 2047 and its value is represented by 8 Bits of DECIM Register and first 3 LSBs of CR2 Register.

Each ADC core has its own registers bank which comprise of CR1, CR2, DECIM, IDAC1, IDAC2, OCR and FSR

registers. The user can read/write these registers when that particular ADC core is selected using a particular channel address on input primary pins.

Whenever there is step change in input, digital filter requires three cycles to settle.

IDAC

There are sixteen pair of 8 Bit IDAC associated with 16 units of ∑Δ Modulator. The output of each IDAC pair is shorted with positive and negative inputs of corresponding ∑Δ Modulator unit. Each pair of IDAC can be programmed independently. The output current of a particular IDAC pair is set with RDAC, the range select bits in CR1 register and 8 Bit digital value in IDAC registers. The output current of IDAC is given as:

$$IDAC\ Current = \frac{V_{REF\_IDAC}}{8*R_{DAC}}\ (2^{RANGE-1})(DAC\ CODE)$$

RDAC resistor is common to all IDACs. In case IDAC is not being used, set the value of range as 00. V_{REF}_IDAC can be maximum upto 1.25V

DRDY (DATA READY)

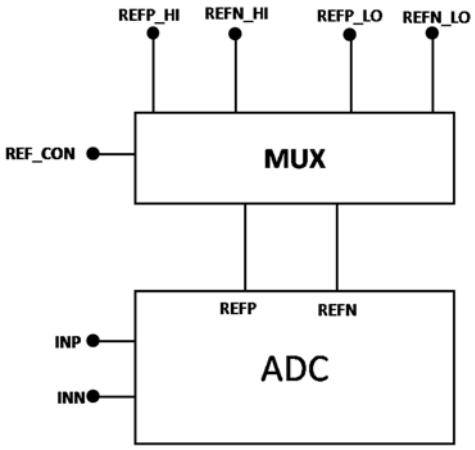
The DRDY pin is used as a status signal to indicate when new digital code is ready to be read from the selected ADC core of Multi-Core RDAS. DRDY goes low when new data is available. It becomes high in the mid of second byte read during read operation from the data register in flight mode. In case, in response to the DRDY assertion no read operation is performed, DRDY will remain low till next filter clock cycle or till next channel change. It is mandatory for the user to read at least two bytes, otherwise the DRDY will remains low till next filter clock or channel change.

VOLTAGE REGULATOR

The device has on chip 1.8V linear voltage regulator. The input voltage range is 2.6V to3.6V and full load current is 12mA.

REFERENCES

The device has two options of the differential references: REFP_HI, REFN_HI and REFP_LO, REFN_LO. For a particular ADC core any of the reference can be selected using the REF_CON bit of CR1 control register as shown below.



The device has on chip 1.22V bandgap reference circuitry also. To use it, the user needs to connect it externally with any one of two references.

CONTROL LOGIC

Any ADC can be selected by applying appropriate four bits channel address

CH_ADDR [3:0]. All the operations like instruction decoding, command execution, SPI control, DRDY generation, calibration & over range management, etc are governed by this unit.

Multi-core RDAS have two modes of operation i.e. flight mode and program mode. The chip can be made to operate in any mode based on the logic high/low of Mode Pin.

Program Mode: During this mode (Mode Pin at Logic Low) user can program the control registers for different settings like decimation ratio, PGA, pre-scaler, IDAC currents etc. All the commands will be recognized only in Program Mode.

Steps to be follow in program mode.

1. Set the mode of device in Program mode.
2. Set the address lines corresponding to a particular ADC core.
3. Enable the SS_N signal.
4. Set the control registers and perform the calibration.
5. Follow steps 2 and 4 for all the ADC cores.

Flight Mode: During this mode, data from selected ADC core sends out from the device. Whenever Master wants to fetch data of a particular ADC core; place the address of ADC core on the address lines: CH_ADDR [3:0] and then asserts chip select enable signal. Thereafter, three dummy bytes are written on SPI bus and 24 bit data is received through DOUT. Valid data from device will be available at the falling edge of DRDY. During this mode no commands will be recognized by the device.

Steps to be follow in flight mode.

1. Set the mode of the device in Flight mode
2. Set the address lines corresponding to a particular ADC core.
3. Wait for negative edge of DRDY signal.
4. Enable the SS_N signal.
5. Read the data of selected ADC through DOUT.
6. Disable the SS_N Signal.
7. To read data from other ADC cores, repeat steps 2 to 6.

SERIAL INTERFACE

The serial interface is standard four-wire SPI compatible (DIN, DOUT, SCLK and SS). All ADC core can communicate serially through single SPI. The user has to select a particular ADC core for data transaction by placing a four bits address line CH_ADDR [3:0]. SCLK frequency can go up to f_{CLK} /4. If SS pin goes HIGH the serial interface will reset and DOUT pin will become tri-state.

The SS must be Low during the communication. When SS is Low, the output data register will never be updated even if new data comes. After data read operation, it should be made high.

DIN is the serial data input port. It is internally sampled at positive edge of SCLK by SPI.

DOUT is the serial data output port and is launched at negative edge of SCLK. DOUT immediately goes into tri-state when SS is high.

OFFSET AND GAIN CALIBRATION

Both the self offset error and complete system offset error in selected ADC core can be reduced with offset

calibration. This is handled with two offset commands SEFOCAL and SYSOCAL. There is also a gain calibration module to compensate self gain and system gain error with SELFGAIN and SYSGAIN command respectively. ***Please refer calibration procedure section.*** Each calibration process takes five conversion cycles to complete. Therefore it takes 10 conversion cycles to complete both offset and gain error. Calibration must be performed after system reset, a change in decimation ratio or a change of the PGA.

Calibration commands will only update the Offset Calibration Register (OCR) with appropriate offset value. However, to enable the offset correction, OCEN bit of CR1 control register has to be set separately. Similarly to apply gain correction, GCALEN bit has to be set.

SELFGAIN command is only possible at PGA1.

OVER-LOAD DETECTION MODULE

Where digital code without calibration is such that it cannot be corrected after calibration then Over-Load detection module detects over-load and clip digital output appropriately to $7FFFFF_H$ and 800000_H.

Status of over-load detection module is available at ORD Pin. This pin will become high in case of over-load condition.

Over-load detection can be disabled by setting OLDD flag of CR2 control register. By default it is enabled. In case of overload condition of any one core, data output of other core get affected. So it is recommended to disable this bit.

OVER-RANGE DETECTION MODULE

If digital code after gain and offset calibration is out of the acceptable code range then digital over-range module detects over-range and clip digital output appropriately to $7FFFFF_H$ and 800000_H. To ensure the proper functioning of the Over Range Detection Module, following constraint on OCR & FSR register value must be followed:

Maximum value of OCR register should not exceed $3FFFFF_H$ for negative offset correction and $C00000_H$ for positive offset correction.

FSR value must be positive.

When device is in the over-range condition, the ORD pin will become high.

Over-range detection can be disabled by setting OVDD flag of CR2 control register. By default it is enabled.

OVDD bit also affects digital output range. Setting OVDD bit will half the digital output range as shown below.

OVDD BIT	ANALOG INPUT	DIGITAL OUTPUT CODE
0	$+V_{REF}$	$7FFFFF_H$
	0	000000_H
	$-V_{REF}$	800000_H
1	$+V_{REF}$	$3FFFFF_H$
	0	000000_H
	$-V_{REF}$	$C00000_H$

CALIBRATION PROCEDURE

The Multi-Core RDAS has two commands namely SEFOCAL and SYSOCAL to compensate offset errors. Internal calibration of device is called self calibration. By executing SELFOCAL command, the device shorts the ADC input and stores the offset value into OCR register in 2's complement form.

For system calibration, the user must apply appropriate 'zero signal' to the selected input channel and then execute SYSOCAL command. In this case ADC computes the offset value based on the available differential input signal and stores it into OCR register in 2's complement form. The System gain calibration requires appositive "full scale differential input signal. On executing system gain command, ADC computes a value to nullify gain error. At the completion of calibration, the DRDY signal will go Low to indicate that calibration is complete and valid data is available.

Calibration commands will only update the Offset Calibration Register (OCR) with appropriate offset value. However, to enable the offset correction, OCEN bit of CR1 control register has to be set separately. Similarly to enable gain calibration set GCALEN bit of CR1 register. Each calibration process takes five conversion cycles to complete. DRDY will be asserted to indicate completion of the calibration process.
Apart from above commands, OSR and FSR can be accessed externally through RREG (Read Register) and WREG (Write Register) commands. This will provide flexibility to manually set the OCR and FSR.

POWER ON SEQUENCES

The Device needs power on sequencing. All the inputs must be applied after the power supply is settled. Analog inputs must be applied after AVDD and MVDD are settled. After DVDD/VDD_LDO is power up, the output of LDO, OUT_LDO (which is the 1.8V supply for the digital core) takes 240 µs to settle. Hence, all the digital input must be applied after 240 µs only.

COMMAND DEFINITIONS

The commands listed below control the operation of SC1221-0 Device. Some commands are stand-alone commands (e.g. SELFOCAL) while others require additional bytes (e.g., WREG requires command and the data bytes).

Operands:
rrrr represents the register address.

nnnnnnnn represents the data.

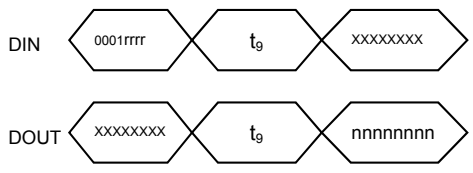
xxxx: these bits will be ignored while instruction decoding.

COMMANDS	DESCRIPTION	COMMAND BYTE	2ND COMMAND BYTE
RREG	Read from Register rrrr	0100 rrrr ($4r_H$)	-N.A.-
WREG	Write to Register rrrr	0101 rrrr ($5r_H$)	nnnnnnnn
SELFOCAL	Self Offset Calibration	0110 xxxx ($6x_H$)	-N.A.-
SYSOCAL	System Offset Calibration	0111 xxxx ($7x_H$)	-N.A.-
SELFGAIN	Self Gain Calibration	1000 xxxx ($8x_H$)	-N.A.-
SYSGAIN	System Gain Calibration	1001 xxxx ($9x_H$)	-N.A.-

RREG (READ REGISTER)

RREG (Read Register) command reads content of the specified register. The address of the register to be read is specified in the LSB nibble of the instruction.

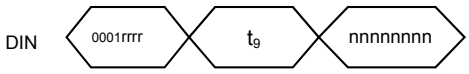
Operands: r, n
Bytes: 2
Encoding: 0100 rrrr



WREG (WRITE REGISTER)

WREG (Write Register) command writes the data to specified register. The address of the register to be written is specified in the LSB nibble of the first byte. Second byte represents the data to be written.

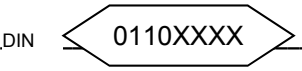
Operands: r, n
Bytes: 2
Encoding: 0101rrrr nnnnnnnn



SELFOCAL (SELF OFFSET CALIBRATION)

This command performs Self Offset Calibration. At the end of the calibration process, offset value will be stored in 24-bit internal Offset Calibration Register (OCR) is in 2's complement format. DRDY will be asserted low to indicate completion of the command.

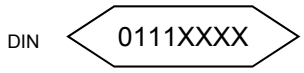
Operands: x
Bytes: 1
Encoding: 0110 xxxx



SYSOCAL (SYSTEM OFFSET CALIBRATION)

With this command ADC computes the offset value based on the available differential input signal on ADC input to nullify offset in the system. The offset value will be stored in 24-bit internal Offset Calibration Register (OCR) in 2's complement format. DRDY will be asserted low to indicate completion of the command.

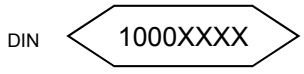
Operands: x
Bytes: 1
Encoding: 0111xxxx



SELFGIAN (SELF GIAN CALIBRATION)

This command performs Self Gain Calibration. At the end of the calibration process, gain calibration coefficient value will be stored in 24-bit internal FSR Register. DRDY will be asserted low to indicate completion of the command.

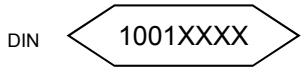
Operands: x
Bytes: 1
Encoding: 1000 xxxx



SYSGAIN (SYSTEM GAIN CALIBRATION)

With this command ADC computes the gain value based on the available differential input signal on ADC input to nullify gain error in the system. The gain value will be stored in 24-bit internal FSR Register. DRDY will be asserted low to indicate completion of the command.

Operands: x
Bytes: 1
Encoding: 1001xxxx



CONTROL / STATUS REGISTERS

The operation of the device is set up through following control / status registers.

Address	Register	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0_H	DIGITAL_CODE_B3 (R)	DC23	DC22	DC21	DC20	DC19	DC18	DC17	DC16
1_H	DIGITAL_CODE_B2 (R)	DC15	DC14	DC13	DC12	DC11	DC10	DC9	DC8
2_H	DIGITAL_CODE_B1 (R)	DC7	DC6	DC5	DC4	DC3	DC2	DC1	DC0
3_H	CR1 (RW)	PGA2	PGA1	PGA0	OCEN	GCALEN	REFCON	IDACR1	IDACR0
4_H	CR2 (RW)	Data Format	OLDD	OVDD	PRE1	PRE0	OSR10	OSR9	OSR8
5_H	DECIM_reg(RW)	OSR7	OSR6	OSR5	OSR4	OSR3	OSR2	OSR1	OSR0
7_H	OCR1 (RW)	OCR07	OCR06	OCR05	OCR04	OCR03	OCR02	OCR01	OCR00
8_H	OCR2 (RW)	OCR15	OCR14	OCR13	OCR12	OCR11	OCR10	OCR09	OCR08
9_H	OCR3 (RW)	OCR23	OCR22	OCR21	OCR20	OCR19	OCR18	OCR17	OCR16
A_H	FSR1 (RW)	FSR07	FSR06	FSR05	FSR04	FSR03	FSR02	FSR01	FSR00
B_H	FSR2 (RW)	FSR15	FSR14	FSR13	FSR12	FSR11	FSR10	FSR09	FSR08
C_H	FSR3 (RW)	FSR23	FSR22	FSR21	FSR20	FSR19	FSR18	FSR17	FSR16
D_H	IDAC1 (RW)	IDAC1_7	IDAC1_6	IDAC1_5	IDAC1_4	IDAC1_3	IDAC1_2	IDAC1_1	IDAC1_0
E_H	IDAC2 (RW)	IDAC2_7	IDAC2_6	IDAC2_5	IDAC2_4	IDAC2_3	IDAC2_2	IDAC2_1	IDAC2_0

R: Read only registers
RW: Read/Write registers
Note: At reset all registers are initialized to 00_H on reset.

CR1 (ADD: 03_H) CONTROL REGISTER-1

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
PGA2	PGA1	PGA0	OCEN	GCALEN	REFCON	IDACR1	IDACR 0

BIT 7-5:PGA2:PGA1:PGA0: Programmable Gain Amplifier selection
000 = 1 100 = 16
001 = 2 101 = 32
010 = 4 110 = 64
011 = 8 111 = 128

Bit4: OCEN: Offset Calibration Enable bit
OCE = 1: Enable offset calibration
OCE = 0: Disable offset calibration

Bit3: GCALEN: Gain calibration Enable bit
GCALEN = 1: Enable Gain calibration
GCALEN = 0: Disable Gain calibration

Bit2: REFCON: Reference Control Bit
0: REFP_LO and REFN_LO will be selected
1: REFP_HI and REFN_HI will be selected

Bit1-0: IDACR1: IDACR0: Range Selection for current in IDAC
00 = off 10 = 1 mA
01 = 0.5 mA 11 = 2 mA

CR2 (ADD: 04_H) CONTROL REGISTER- 2

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
DATA FORMAT	OLDD	OVDD	PRE1	PRE0	OSR10	OSR9	OSR8

Bit7: Data Format of the output code
1 = Offset Binary output data
0 = 2's complement output data

Bit6: OLDD: Analog over range detection
0 = Enable over-load detection.
1 = Disable over-load detection.
Note: It is recommended to disable OLDD bit.

Bit5: OVDD: Digital over range detection
0 = Enable over-range detection.
1 = Disable over-range detection.

Bit4-3: PRE1:PRE0: Prescaler bits

PRE1:PRE0	f_{MOD}
00	f_{CLK} /64
01	f_{CLK} /128
10	f_{CLK} /256
11	f_{CLK} /512

Bit2-0:OSR10:OSR9: OSR8 control bits.

Three MSBs of 11bits of decimation ratio
Note: Any update in CR1 or CR2 control register will reset modulator and digital filter. DRDY will also go high.

DECIM (ADD: 05_H) CONTROL REGISTER-3

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
OSR7	OSR6	OSR5	OSR4	OSR3	OSR2	OSR1	OSR0

BIT 7-0: OSR7:OSR0
These bits are 8 LSB bits of 11 bit decimation ratio

OCR1 (ADD: 07_H) OFFSET CALIBRATION REGISTER-1
(Least Significant Byte)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
OCR07	OCR06	OCR05	OCR04	OCR03	OCR02	OCR01	OCR00

OCR2 (ADD: 08_H) OFFSET CALIBRATION REGISTER-2
(Middle Byte)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
OCR15	OCR14	OCR13	OCR12	OCR11	OCR10	OCR09	OCR08

OCR3 (ADD: 09_H) OFFSET CALIBRATION REGISTER-3
(Most Significant Byte)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
OCR23	OCR22	OCR21	OCR20	OCR19	OCR18	OCR17	OCR16

FSR1 (ADD: $0A_H$) FULL SCAEE REGISTER-1
(Least Significant Byte)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FSR07	FSR06	FSR05	FSR04	FSR03	FSR02	FSR01	FSR00

FSR2 (ADD: $0B_H$) FULL SCAEE REGISTER-2
(Middle Byte)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FSR15	FSR14	FSR13	FSR12	FSR11	FSR10	FSR09	FSR08

FSR3 (ADD: $0C_H$) FULL SCAEE REGISTER-3
(Most Significant Byte)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FSR23	FSR22	FSR21	FSR20	FSR19	FSR18	FSR17	FSR16

IDAC1 (ADD: $0E_H$) CURRENT DAC1

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
IDAC1_7	IDAC1_6	IDAC1_5	IDAC1_4	IDAC1_3	IDAC1_2	IDAC1_1	IDAC1_0

The DAC code bits to set IDAC1 current.

IDAC2 (ADD: $0F_H$) CURRENT DAC2

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
IDAC2_7	IDAC2_6	IDAC2_5	IDAC1_4	IDAC2_3	IDAC2_2	IDAC2_1	IDAC2_0

The DAC code bits to set IDAC2 current

DIGITAL_CODE_B3 (ADD: 00_H) DIGITAL OUTPUT CODE
(MOST SIGNIFICANT BYTE)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
DC23	DC22	DC21	DC20	DC19	DC18	DC17	DC16

DIGITAL_CODE_B2 (ADD: 01_H) DIGITAL OUTPUT CODE
(MIDDLE BYTE)

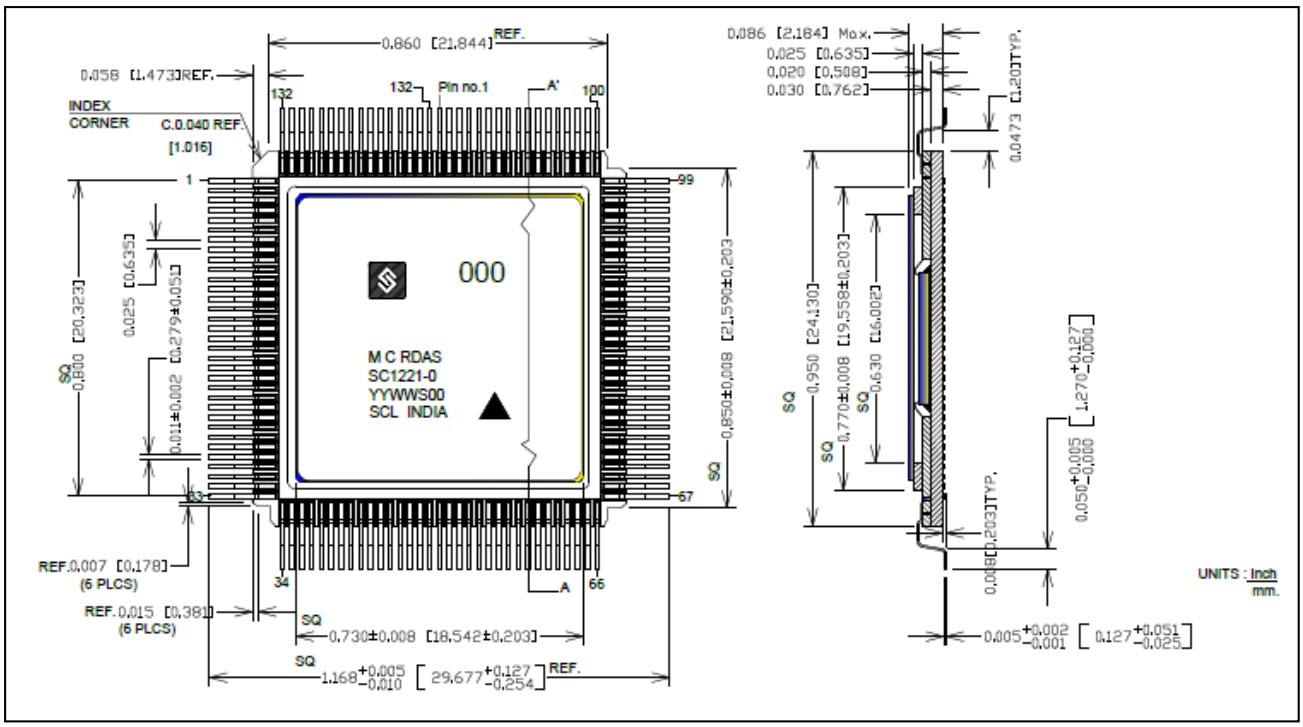
BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
DC15	DC14	DC13	DC12	DC11	DC10	DC09	DC08

DIGITAL_CODE_B1 (ADD: 02_H) DIGITAL OUTPUT CODE
(LEAST SIGNIFICANT BYTE)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
DC07	DC06	DC05	DC04	DC03	DC02	DC01	DC00

PACKAGE INFORMATION

132 Pin CQFP PACKAGE



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