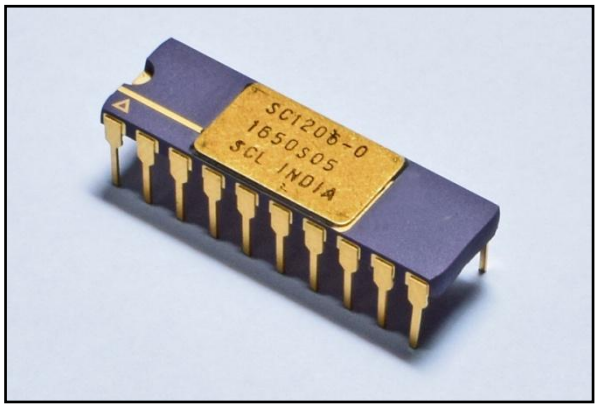
PROGRAMMABLE BIAS GENERATOR

(SC1206-0)



DATA SHEET

Version 1.0, February 2017

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PRODUCT DESCRIPTION:

SC1206-0 is a programmable output bias voltage generator with dynamic range of 1.6V (0.5V to 2.1V). It is capable of providing the input and output programmability which is achieved by giving programmed digital inputs to the system.

The output enable programmability is achieved with help of switches which can control the output programmability so as to give outputs in multiple output lines.

- **Line voltage: 3.0V-3.6V**
- **Dynamic range: 1.6V (0.5V to 2.1V)**
- **Resolution: 8bits**
- **Output drive current: 5mA**
- **Two Programmable outputs**
- **Output enable Programmability**
- **Programming Interface: 4wire serial**
- **Clock input: LVCMOS compatible**
- **Operating Temperature (T_A): -55ºC to +125ºC**
- **Low Power Dissipation**
- **Packaged in 20Lead Side Brazed package**
- **SCL 0.18µ CMOS technology**

FEATURES:

DEVICE SUMMARY:

Table 1: Device Summary

DEVICE	PACKAGE	PINS	LEAD FINISH	DESCRIPTION	TEMPERATURE RANGE
SC1206-0	20 Lead Side Brazed	20	Gold	Engineering Model	-55°C to +125°C

BLOCK DIAGRAM:

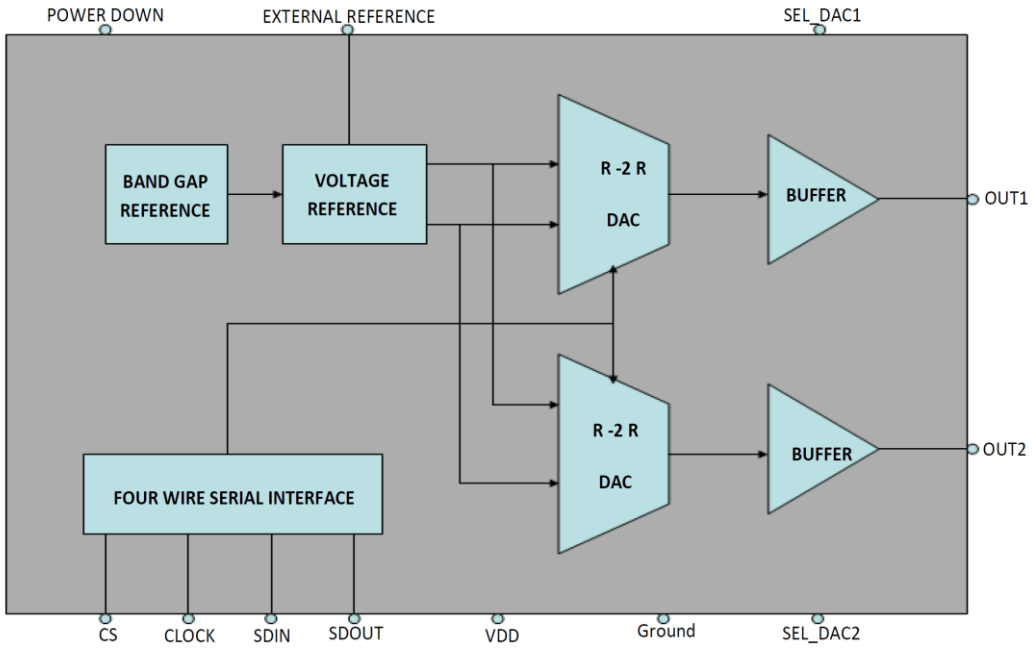


Figure 1: Device Pin Diagram

PIN CONFIGURATION:

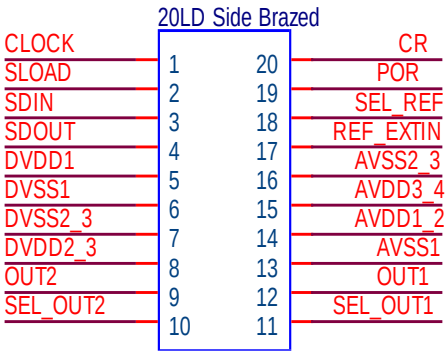


Figure 2: Device Pin Diagram

PIN DESCRIPTION:

Table 2: Pin Details

PIN NO.	PIN NAME	PIN DETAILS	DESCRIPTION
1.	CLOCK	Digital Input	Clock for Serial Programming
2.	SLOAD	Digital Input	Chip select
3.	SDIN	Digital Input	Serial data Input
4.	SDOUT	Digital Output	Serial data Out
5.	DVDD1	Power	Supply Voltage
6.	DVSS1	Ground	Supply Voltage
7.	DVSS2_3	Ground	Ground
8.	DVDD2_3	Power	Supply Voltage
9.	OUT2	Analog Output	Analog Output
10.	SEL_OUT2	Digital Input	Enable Pin for Out2 (Logic 1 to enable ouptut of DAC2)
11.	SEL_OUT1	Digital Input	Enable Pin for Out1 (Logic 1 to enable ouptut of DAC1)
12.	OUT1	Analog Output	Analog Output
13.	AVSS1	Ground	Ground
14.	AVDD1_2	Power	Supply Voltage
15.	AVDD3_4	Power	Supply Voltage
16.	AVSS2_3	Ground	Ground
17.	REF_EXTIN	Analog Input	External Reference
18.	SEL_REF	Digital Input	Disable Pin for External Reference (Logic 1 to enable internal ref)
19.	POR	Analog Output	Power on Reset
20.	CR	Digital Input	Clear pin for DAC registers (Active Low)

SPI TIMING DIAGRAM:

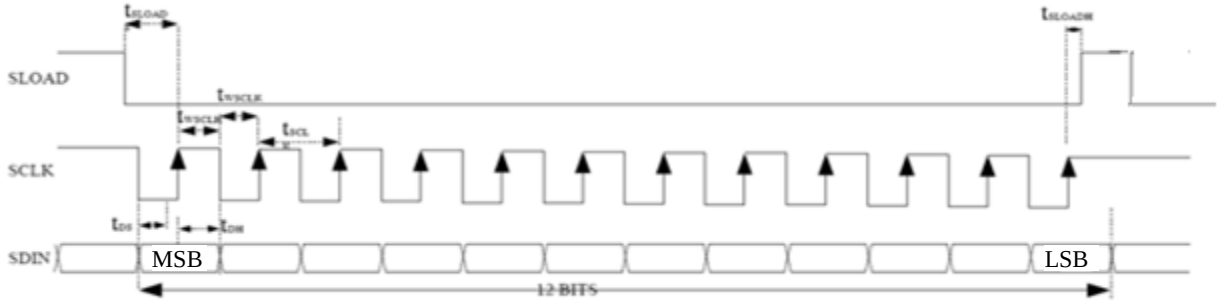


Figure 3: Write Operation (There must be high to low transition on SLOAD for minimum of one clock cycle for next register write)

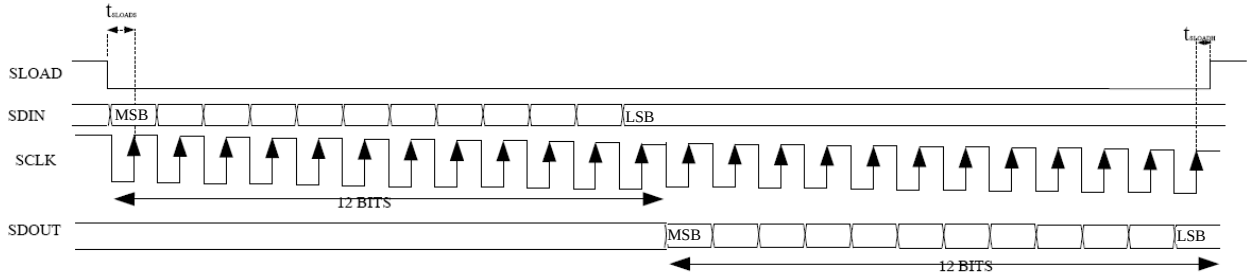


Figure 4: Read Operation (There must be high to low transition on SLOAD for minimum of one clock cycle for next register read)

SD11 MSB	SD10	SD09	SD08	SD07	SD06	SD05	SD04	SD03	SD02	SD01	SD00 LSB
READ/ WRITE	0	DAC	0	D7	D6	D5	D4	D3	D2	D1	D0

SD11 = Logic 1 Read the contents of the registers

= Logic 0 Write the contents into the registers

SD09 = Logic 0 Select register of DAC 1 selected

= Logic 1 Select register of DAC 2 selected

SD7-0 = DAC input bits

ABSOLUTE MAXIMUM RATING [(1)]:

Over operating free-air temperature range (unless otherwise stated)

Table 3: Absolute Maximum Rating

PARAMETER	WITH RESPECT TO	MIN.	MAX.	UNIT
External Reference	AVSS	-0.3	AVDD+0.3	V
Digital Inputs	AVSS	-0.3	AVDD+0.3	V
AVDD	AVSS	-0.3	3.9	V
DVDD	DVSS	-0.3	3.9	V
AVSS	DVSS	-0.3	0.3	V
Digital Outputs	DVSS	-0.3	DVDD+0.3	V
Storage Temperature		-65	150	°C
Lead Temperature (10sec)			100	°C
ESD Tolerance (HBM)		1000		V
Latch Up Protection		±100		mA

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS:

Table 4: Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply voltage (DVDD/AVDD)	3.0	3.3	3.6	V
V_{IH}	High level input voltage	2.0	-	-	V
V_{IL}	Low level input voltage	-	-	0.8	V
V_{OH}	High level output voltage	2.9	-	-	V
V_{OL}	Low level output voltage	-	-	0.5	V
I_{LOAD}	Output drive current	-	-	5	mA
T_A	Ambient temperature range	-55	-	+125	ºC
f_{MAX}	Programming speed of serial interface	20			MHz

DC ELECTRICAL SPECIFICATIONS

Test condition: V_{DD} = 3.3± 0.3V, T_A = -55°C to +125°C, C_{IN} = 0.1uF, unless otherwise specified.

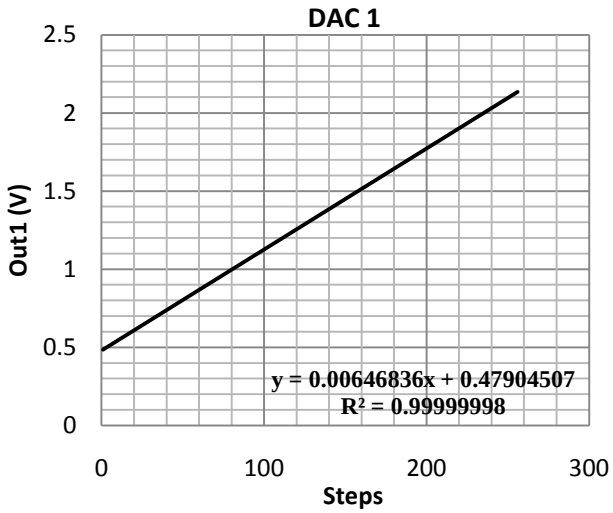
Table 5: DC Electrical Specification

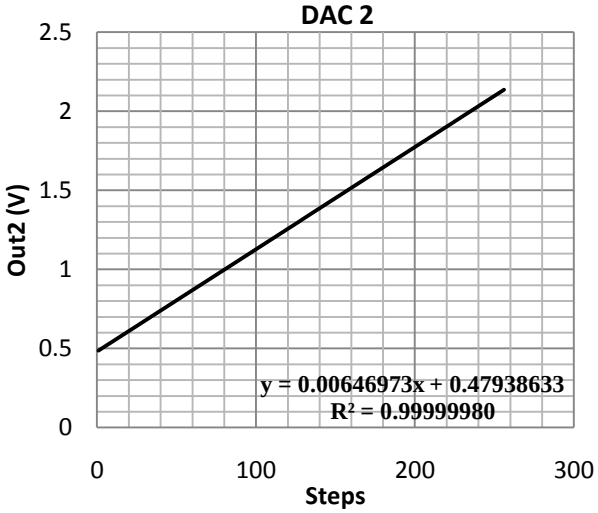
PARAMETER	TEST CONDITIONS	SC1206-0			UNITS
		MIN	TYP	MAX	
Nominal Output Voltage	Programmed @ 0x00 Min value	0.45	0.48	0.55	V
	Programmed @ 0x7F Mid value	1.2	1.3	1.35	
	Programmed @ 0xFF Max value	1.9	2.1	2.2	V
Output Voltage Range	No Load	1.6	1.63	1.66	V
Resolution	No Load	6.3	6.4	6.5	mV
Temperature Drift	Internal Reference, No load	-	26.16	-	ppm/°C
	Internal Reference with R_{LOAD} = 270Ω (I_{LOAD} = 5mA)	-	32.24	-	
	External Reference = 1.65V, No Load, C_{IN} @ REF_EXTIN = 1uF	-	18.42	-	
Load Regulation	0.1mA ≤ I_{LOAD} ≤ 5mA	-	0.25	0.5	%/mA
Line Regulation	3.0V ≤ V_{IN} ≤ 3.6V, No Load	-	0.07	0.1	%/V
Output Impedance	R_{LOAD} = 100Ω,i.e., I_{LOAD} = 5mA_{PP}, C_{LOAD} = 10pF (100KHz to 50MHz) @0x7F	4	-	150	ohm
Noise	No Load (100KHz to 1MHz)	-	-	18	µV
	No Load (100KHz to 20MHz)	-	-	90	
	No Load (100KHz to 100MHz)	-	-	150	
Power Dissipation	No Load	-	5.2	7	mW

TYPICAL CHARACTERISTICS

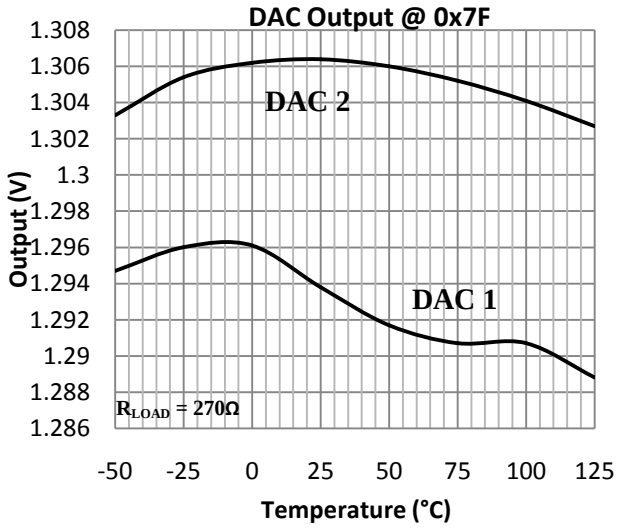
Test condition: V_{DD} = 3.3± 0.3V, T_A = -55°C to +125°C, C_{IN} = 0.1uF, unless otherwise specified.

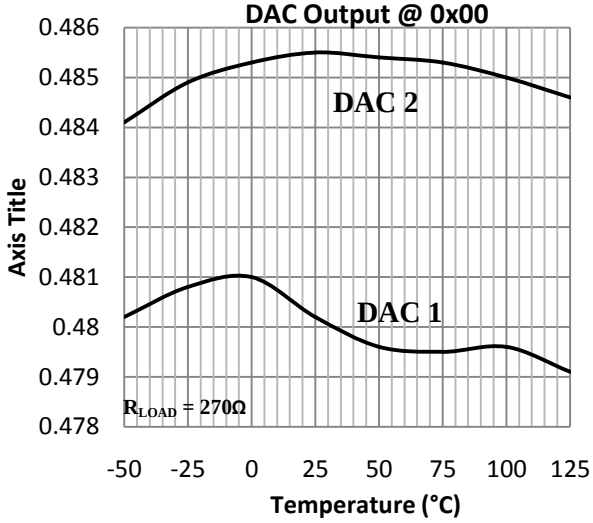
OUTPUT LINEARITY

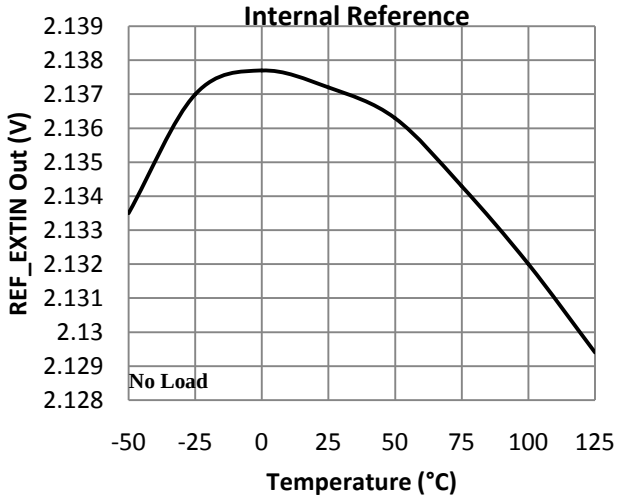


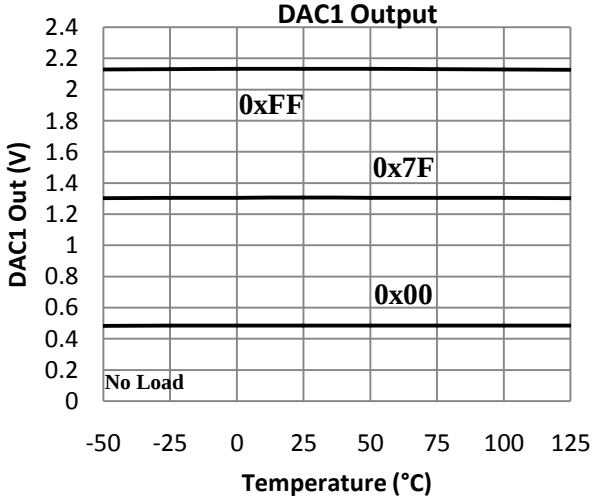


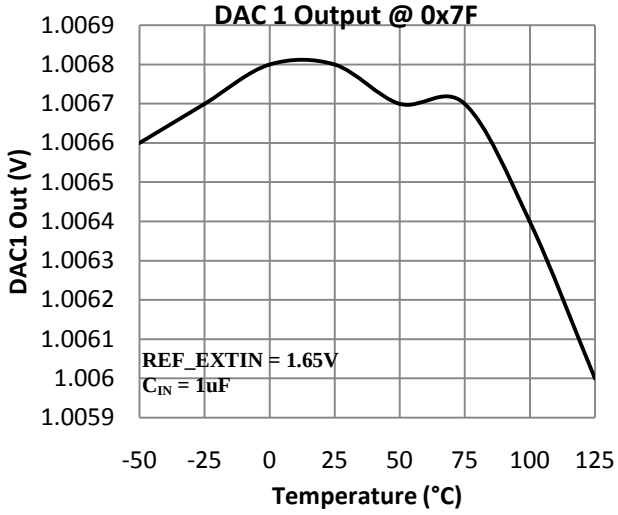
TEMPERATURE VARIATION

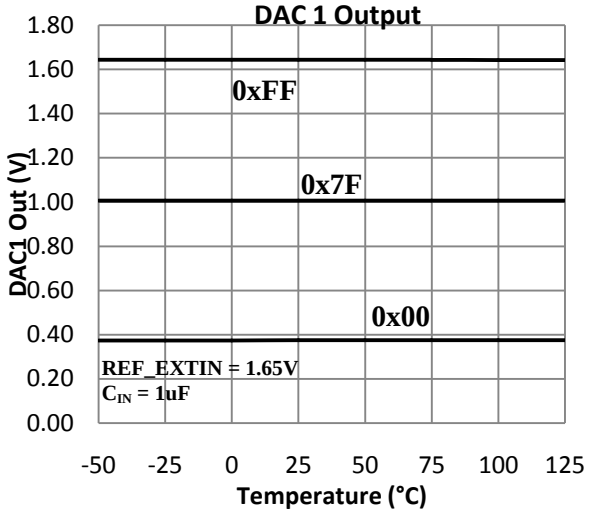


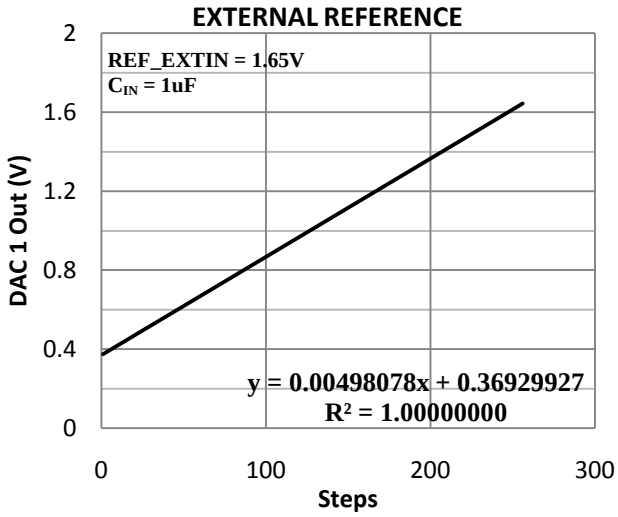


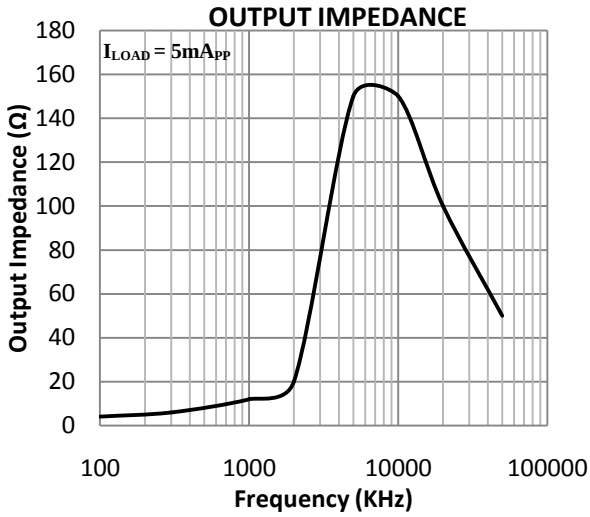


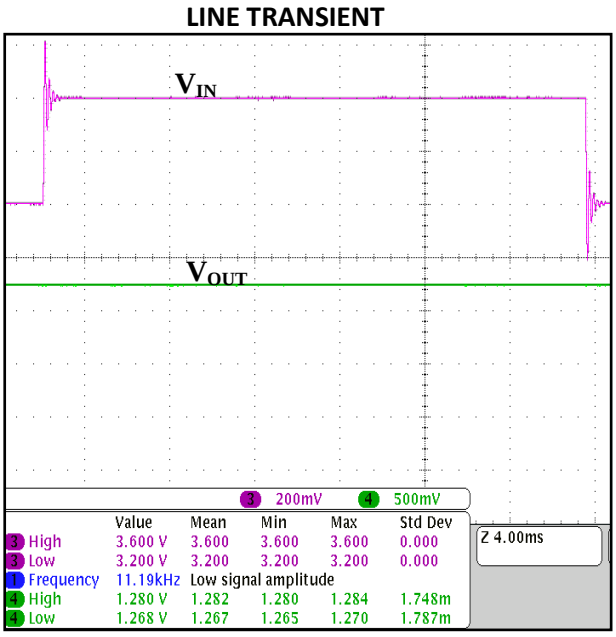


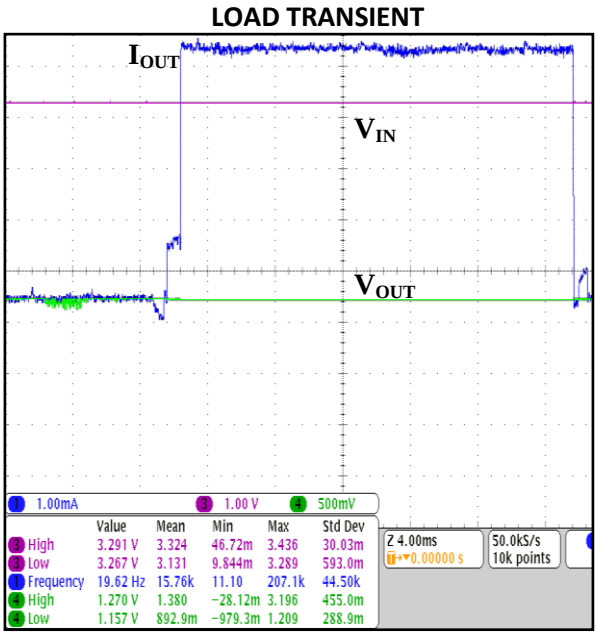

DAC 1 Output @ 0x7F
DAC1 Out (V)
1.0069
1.0068
1.0067
1.0066
1.0065
1.0064
1.0063
1.0062
1.0061
1.006
1.0059
REF_EXTIN = 1.65V
CIN = 1uF
-50 -25 0 25 50 75 100 125
Temperature (°C)


DAC 1 Output
DAC1 Out (V)
1.80
1.60
1.40
1.20
1.00
0.80
0.60
0.40
0.20
0.00
0xFF
0x7F
0x00
REF_EXTIN = 1.65V
CIN = 1uF
-50 -25 0 25 50 75 100 125
Temperature (°C)


EXTERNAL REFERENCE
DAC 1 Out (V)
2
1.6
1.2
0.8
0.4
0
REF_EXTIN = 1.65V
CIN = 1uF
y = 0.00498078x + 0.36929927
R² = 1.00000000
0 100 200 300
Steps

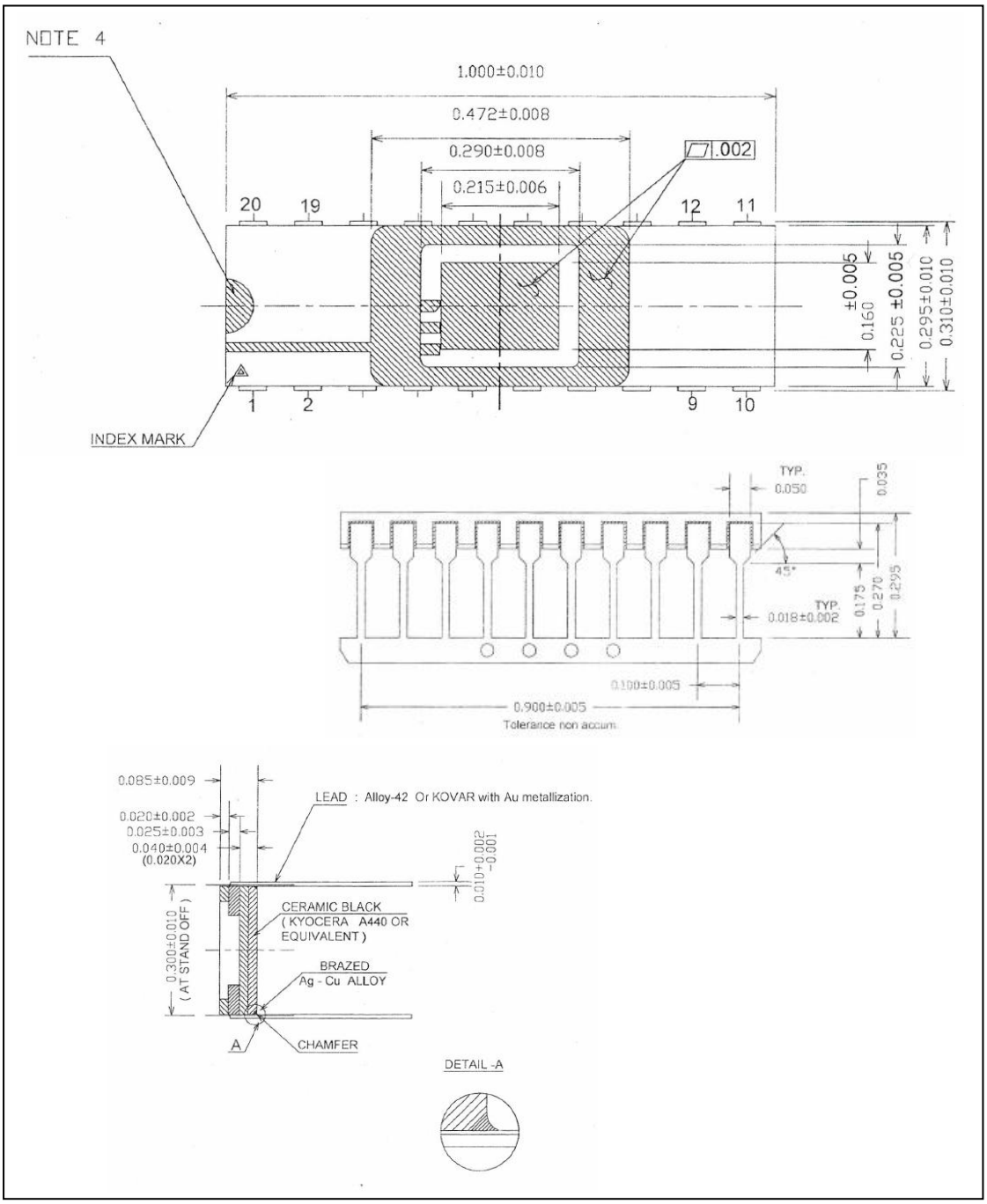

OUTPUT IMPEDANCE
ILOAD = 5mAPP
Output Impedance (Ω)
180
160
140
120
100
80
60
40
20
0
100 1000 10000 100000
Frequency (KHz)


LINE TRANSIENT
VIN
VOUT
200mV
500mV
Value Mean Min Max Std Dev
High 3.600 V 3.600 3.600 3.600 0.000
Low 3.200 V 3.200 3.200 3.200 0.000
Frequency 11.19kHz Low signal amplitude
High 1.280 V 1.282 1.280 1.284 1.748m
Low 1.268 V 1.267 1.265 1.270 1.787m
Z 4.00ms


LOAD TRANSIENT
IOUT
VIN
VOUT
1.00mA
1.00 V
500mV
Value Mean Min Max Std Dev
High 3.291 V 3.324 46.72m 3.436 30.03m
Low 3.267 V 3.131 9.844m 3.289 593.0m
Frequency 19.62 Hz 15.76k 11.10 207.1k 44.50k
High 1.270 V 1.380 -28.12m 3.196 455.0m
Low 1.157 V 892.9m -979.3m 1.209 288.9m
Z 4.00ms
50.0kS/s
10k points

PACKAGE DRAWING (20Lead Side Brazed):

NOTE: All linear dimensions are in inches.



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