DATA SHEET

SINGLE CHANNEL 14-BIT, 10MSPS CCD ANALOG SIGNAL PROCESSOR WITH ON CHIP VOLTAGE REFERENCE

SC1203-0

Version 2.0, September 2021

Semi–Conductor Laboratory
Government of India
S.A.S. Nagar, Punjab-160071
www.scl.gov.in

CCD Analog Signal Processor (SC1203-0)

PRODUCT DESCRIPTION:

This is fully integrated, high performance analog signal processor for CCD applications. It features a single channel architecture designed to sample and conditions the outputs of CCD arrays. Signal paths utilize Correlated Double Sampler (CDS), 6-bit Programmable Gain Amplifiers (PGA), and 9-bit offset correction DAC for black level correction of input. The PGA and offset DAC are programmed independently allowing unique values of gain and offset for inputs. The signals are then routed to a high performance high speed Analog-to-Digital Converter (ADC). The internal registers can be programmed through a 4-wire serial digital interface. A programmable feature includes gain adjustment, black level correction, programmable delay and input bandwidth control. The 14 bit 10MSPS is a monolithic CMOS analog-to-digital converter capable of converting analog input signals into 14-bit digital word at 10 Mega samples per second (MSPS) and designed for imaging applications. This converter uses a differential, pipeline architecture with digital error correction. The Power Down feature reduces power consumption to <30mW. The differential inputs provide a full scale differential input swing equal to 2 times of VREF (=CAPTE-CAPBE). Full scale input range is recommended for optimum performance. The ASIC is fabricated in 180nm SCL CMOS standard logic process.

FEATURES

- **Operating Voltage: 3.3V**
- **Resolution: 14Bits**
- **Data Rate: 10MSPS**
- **1Vp-p Differential /Single Ended Input**
- **On Chip Voltage References**
- **No Missing Code Guaranteed**
- **Output straight Binary Format**
- **Data Latency 9 Clock Cycles**
- **Power Consumption <150mW (For S2:S1:S0=111)**
- **Power Consumption <450mW (For S2:S1:S0=010)**
- **Power Down Mode**
- **64 PGA Gain Steps**
- **1 to 6 PGA Gain Ranges**
- **9 Bit Offset Correction DAC Resolution**
- **±60mV Offset Correction DAC Range**
- **Single event latch (SEL) immune up to 70 MeV-cm2/mg**
- **Single event upset (SEU) immune up to 70 MeV-cm2/mg**
- **100 PIN CQFJ Package**
- **θjc: 0.99°C/Watt**
- **180nm SCL's Standard CMOS Technology**

APPLICATIONS

- **Imaging applications**

BLOCK DIAGRAM:

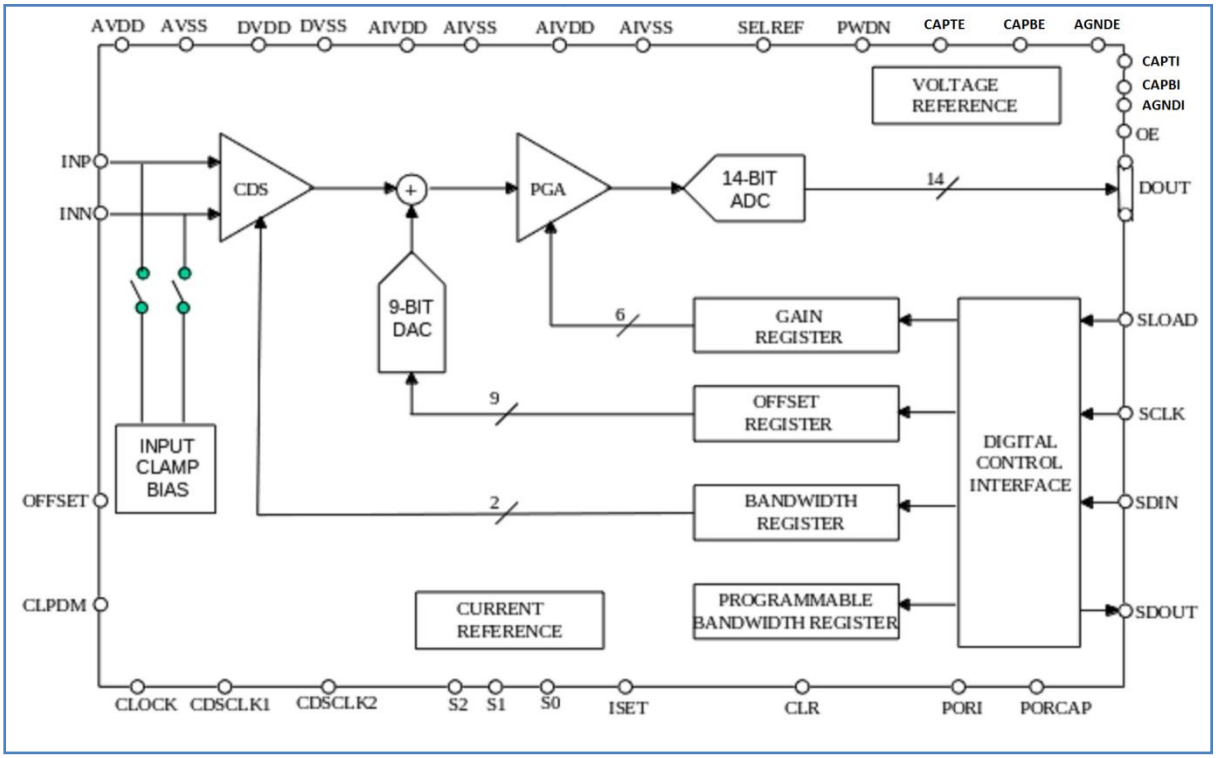

Figure-1: Device Block Diagram

DEVICE SUMMARY:

Table-1: Package Detail

Reference	Package	pins	Lead Finish	Description	Junction Temp. range
SC1203-0	CQFJ Package	100	Gold	Engineering Model	-55°C to +125°C

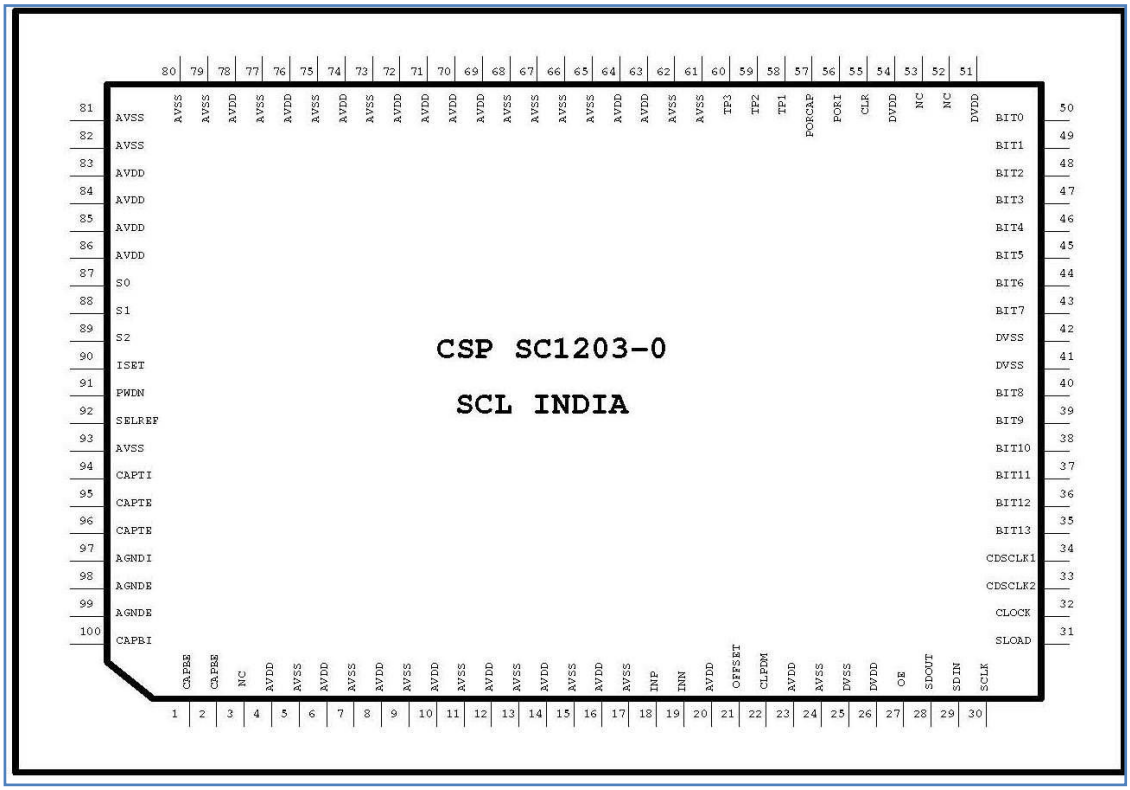

Figure-2: Pin Diagram

Table-2: Pin Configuration

Pin No.	Pin Name	Pin Type	Pin Description
4,6,8,10,12,14,16,20,23,63, 64,69,70,71,72,74,76,78,83,84 ,85,86	AVDD	AP	Analog Positive Supply (+3.3 V)
26,51,54	DVDD	DP	Digital positive Supply (3.3 V)
5,7,9,11,13,15,17,24,61,62, 65,66,67,68,73,75,77,79,80,81 ,82,93	AVSS	AP	Analog Negative Supply (0 V)
25,41,42	DVSS	DP	Digital Negative Supply (0 V)
95,96	CAPTE	AI	External Reference Voltage (1.9V,Typ)
98,99	AGNDE	AI	External Reference Voltage (1.65V,Typ)
1,2	CAPBE	AI	External Reference Voltage (1.4V,Typ)
94	CAPTI	AO	Internal Reference Voltage (1.9V,Typ)
97	AGNDI	AO	Internal Reference Voltage (1.65V,Typ)
100	CAPBI	AO	Internal Reference Voltage (1.4V,Typ)
18	INP	AI	Positive CCD signal input
19	INN	AI	Negative CCD signal input
21	OFFSET	AI	Clamp bias level
22	CLPDM	AI	Connect to AVSS

Pin No.	Pin Name	Pin Type	Pin Description
27	OE	DI	Output data enable Low :Normal operation High: Digital output high impedance state
28	SDOUT	DO	Serial Interface Data Output
29	SDIN	DI	Serial Interface Data Input
30	SCLK	DI	Serial Interface Clock
31	SLOAD	DI	Serial data latch (Active Low)
32	CLOCK	DI	CSP Sampling Clock
33	CDSCLK2	DI	CDS Data Level Sampling Clock (In Case of CCD input is applied differentially or at INN pin) CDS Reference Level Sampling Clock (In Case of CCD is input applied at INP) ***Please refer Figure 5,6,7***
34	CDSCLK1	DI	CDS Reference Level Sampling Clock((In Case of CCD input is applied differentially or at INN) CDS Data Level Sampling Clock((In Case of CCD input applied at INP) ***Please refer Figure 5,6,7***
55	CLR	DI	Clear signal to initialize all internal registers to default setting (Active Low). **Note1**
56	PORI	DO	Internally generated POR signal. **Note2**
57	PORCAP	AO	External capacitor can use to increase delay in generation of POR signal.
90	ISET	AO	Connect to AVSS directly or through 10KΩ
91	PWDN	DI	Power Down Mode. (Active Low). **Note3**
92	SELREF	DI	Select input for reference voltage selection High : Internal reference selected Low : External reference selected
35	BIT13	DO	ADC digital output Bit (MSB)
36	BIT12	DO	ADC digital output Bit
37	BIT11	DO	ADC digital output Bit
38	BIT10	DO	ADC digital output Bit
39	BIT9	DO	ADC digital output Bit
40	BIT8	DO	ADC digital output Bit
43	BIT7	DO	ADC digital output Bit
44	BIT6	DO	ADC digital output Bit
45	BIT5	DO	ADC digital output Bit
46	BIT4	DO	ADC digital output Bit

Pin No.	Pin Name	Pin Type	Pin Description
47	BIT3	DO	ADC digital output Bit
48	BIT2	DO	ADC digital output Bit
49	BIT1	DO	ADC digital output Bit
50	BIT0	DO	ADC digital output Bit (LSB)
87	S0	DI	The minimum power dissipation will be with 111. The maximum power dissipation will be with 000
88	S1	DI	
89	S2	DI	
58	TP1		Test Point
59	TP2		Test Point
60	TP3		Test Point
3,52,53	NC	NC	Internally Not Connected

- # PIN TYPE: AI = Analog Input, AO = Analog Output, DI = Digital Input, DO = Digital Output, AP = Analog Power, DP = Digital Power.
- **Note1.** Minimum 20 clock cycles are required for clear internal registers after power up.
- **Note2**. PORI is internally generated power on reset signal and it can be used as a clear signal to reset all internal programmable registers at the time of power on to its default setting by externally connecting PORI pin to CLR pin.
- **Note3**. In standby mode current of all analog section will be shut down, excluding voltage reference block. Settings of internal programmable registers will be retained.

ELECTRICAL SPECIFICATIONS:

All typical specifications are at T_A = 25°C, all power supply voltages = 3.3 V, and S2, S1, S0=3.3V, internal reference selected unless otherwise stated. All maximum specifications are assured across operating temperature and voltage ranges.

Table-3: Electrical Specifications

Parameters	Test Conditions	Min.	Typ.	Max.	Units
POWER SUPPLY					
AVDD Analog supply voltage		3.135	3.3	3.465	V
DVDD Digital supply voltage		3.135	3.3	3.465	V
AVDD operating current	1MSPS	27	30	34	mA
	5MSPS	32	34	40	mA
	10MSPS (S2,S1,S0=010)	108	114	127	mA
DVDD operating current	1MSPS	1	1.04	1.1	mA
	5MSPS	5	5.1	5.3	mA
	10MSPS (S2,S1,S0=010)	9	10	10.5	mA
POWER DISSIPATION	Normal Mode @1MSPS	95	102	117	mW
	Normal Mode @5MSPS	122	130	150	mW
	Normal Mode @10MSPS (S2,S1,S0=010)	390	410	450	mW
	Power Down Mode	10	24	30	mW
EXTERNALREFERENCE					
Positive reference voltage	CAPTE		1.9		V
Negative reference voltage	CAPBE		1.4		V
Common Mode Voltage	AGNDE		1.65		V
CURRENT REQUIREMENT					
Positive reference voltage	CAPTE	-100	50	100	µA
Negative reference voltage	CAPBE	-100	50	100	µA
Common Mode Voltage	AGNDE	-1	-2	-3.5	mA
JUNCTION TEMPERATURE					
		-55	25	125	°C
DIGITAL INPUT					
VIH : Logic-high input voltage		2.0		DVDD	V
VIL : Logic-low input voltage				0.8	V
IIH : Logic-high input current		-10		10	µA
IIL : Logic-low input current		-10		10	µA
Input capacitance			5		pF

Parameters	Test Conditions	Min.	Typ.	Max.	Units
DIGITAL OUTPUT					
VOH : Logic-high output voltage	@-20uA IOH	2.4		3.3	V
VOL : Logic-low output voltage	@20uA IOL	0		0.06	V
Output load capacitance	@10MHz		10		pF

ELECTRICAL SPECIFICATIONS (CONTINUED):

All typical specifications are at T_A = 25°C, all power supply voltages = 3.3 V, and S2, S1, S0= 3.3V, internal reference selected unless otherwise stated. All maximum specifications are assured across operating temperature and voltage ranges.

Parameters	Test Conditions	Min.	Typ.	Max.	Units
Resolution				14	Bits
Conversion rate				10	MSPS
Input Range				1Vpp	
No missing codes			Guaranteed		
Differential nonlinearity	1MSPS	-0.6	-0.44	0.8	LSB
	5MSPS	-0.78	-0.55	1.7	LSB
Data latency			9		Clocks
Offset Corrected		-60		60	mV
Gain		0.97		6.7	
Input referred noise	1MSPS			4.6	LSB
	5MSPS			7.1	LSB
	10MSPS (S2,S1,S0=010)			11	LSB
Effective resolution	1MSPS	11.7			Bit
	5MSPS	11.1			Bit
	10MSPS (S2,S1,S0=010)	10.3			Bit
Analog Input capacitance			10		pF

Table-4: Absolute Maximum Ratings*

Parameters	With respect To	Min.	Max.	Units
INP, INN, CAPTE, CAPBE,AGNDE	AVSS	-0.3	AVDD	V
DIGITAL INPUTS	AVSS	-0.3	AVDD	V
AVDD	AVSS	-0.3	3.9	V
DVDD	DVSS	-0.3	3.9	V
AVSS	DVSS	-0.3	0.3	V
DIGITAL OUTPUTS	DVSS	-0.3	DVDD	V
Storage Temperature		-65	150	ºC
Lead Temperature (10 Sec)			300	ºC
ESD Tolerance (HBM)**			> 1000	V
Latch Up Protection**			100	mA

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.
**These are target value. Characterization for this is in progress.

4-WIRES SERIAL DIGITAL INTERFACE

CSP is fully programmable via a serial interface. A simple (SCLK, SDIN, SDOUT and $\overline{SLOAD}$) serial interface is provided to allow reading/writing the internal registers of CSP. Serial interface block includes 2-bit bandwidth register, 9-bit offset register, 6-bit gain register and 5-bit programmable delays register. Serial data SDIN is 12-bit long; the MSB (Most Significant Bit) is set to '0' for writing in and '1' for reading from the internal register. Following this, there are two address bits for accessing and other nine data bits for writing to the particular register. During the read operation, data from the particular register is available on the SDIN pin. To enable serial read/write, $\overline{SLOAD}$ should be pulled low. Sending blocks of 12-bit data to SDIN can program multiple registers. The maximum frequency of SCLK is 20 MHz

To get the default setting of internal registers at the time of power-on, $\overline{CLR}$ signal is required. PORI can also be used as a $\overline{CLR}$ signal to reset all internal programmable registers to its default setting by externally connecting PORI pin to $\overline{CLR}$ pin.

Table-5: 4-Wire Serial Digital Interface

Pin Name	Pin Type	Pin Description
SDIN	DI	Serial Data Input
SDOUT	DO	Serial Data Output
SCLK	DI	Serial Data Clock
$\overline{SLOAD}$	DI	Serial Data Enable

Table-6: 12-bit Internal Register

SD11	**SD10**	**SD9**	**SD8**	**SD7**	**SD6**	**SD5**	**SD4**	**SD3**	**SD2**	**SD1**	**SD0**
RD/WR	A1	A0	D8	D7	D6	D5	D4	D3	D2	D1	D0

Table-7: Register Descriptions

Register Address		Register Name	Register Function
A1	A0		
0	0	Bandwidth Register	I/P Bandwidth Control
0	1	Offset Register	Offset Correction
1	0	Gain Register	PGA Gain Control
1	1	Programmable Delay Register	Programmable Delay

Table-8: Input Bandwidth Vs Bandwidth Register value

S. No.	Bandwidth Register	Input Signal Sample Rate
1	00	20 MHz
2	01	10 MHz
3	10	5 MHz
4	11	1MHz

Table-9: The default value of INTERNAL register

Register Name	Default Value
Bandwidth Register	D1 to D0 = (00)2
Offset Register	D8 to D0 = (100000000)2
Gain Register	D5 to D0 = (000000)2
Programmable Delay Register	D4 to D0 = (00000)2

SERIAL INTERFACE TIMINGS

Table-10: Serial Interface Timings

Symbol	Parameter	Typ	Units
t_{SCLK}	SCLK period	50	ns
t_{WSCLK}	SCLK high or low width	25	ns
t_{SLOADS}	SLOAD to SCLK setup time	5	ns
t_{SLOADH}	SLCLK to SLOAD hold time	2	ns
t_{DS}	Data setup time	5	ns
t_{DH}	Data hold time	2	ns

Standard functionality (Sample Data on rising Edge of SCLK), operation = Write

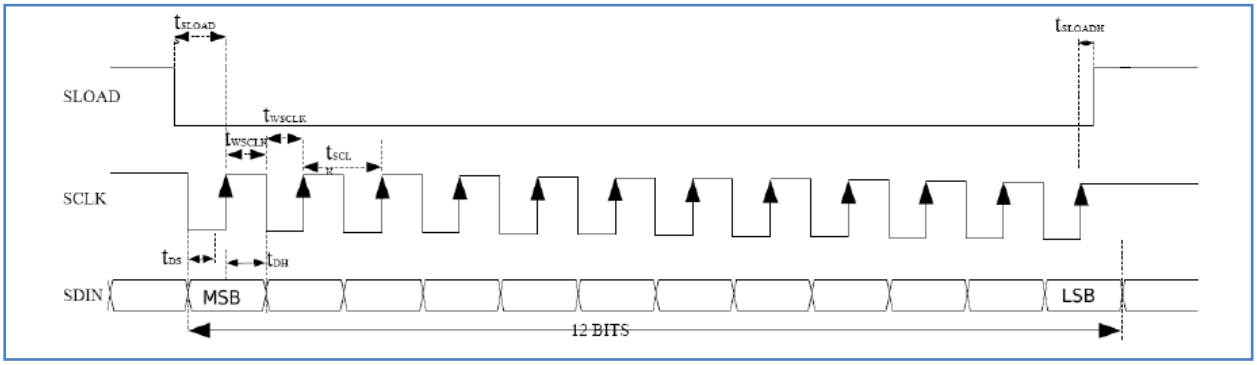

Figure-3: Serial Interface Timings for Write

(There must be high to low transition on SLOAD for minimum of one clock cycle for next register write)

Standard functionality (Sample Data on rising Edge of SCLK), operation = Read

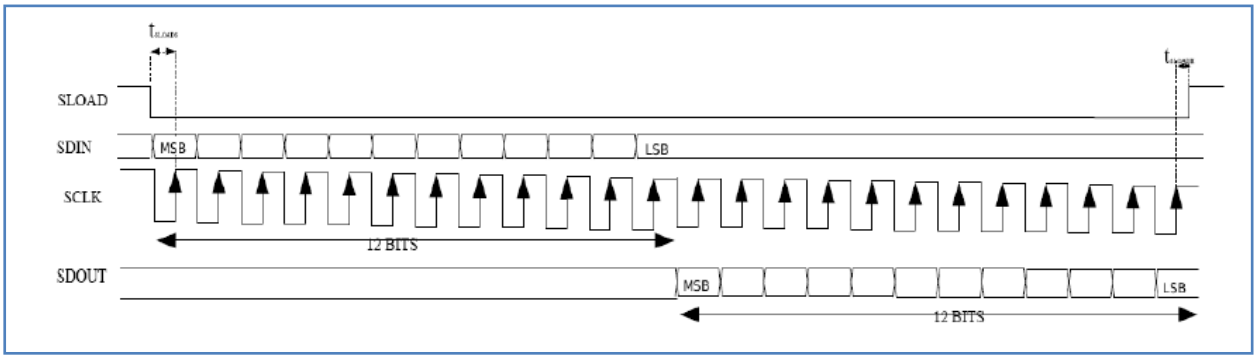

Figure-4: Serial Interface Timings for Read (Sample Data on rising Edge of SCLK), operation = Read

(There must be high to low transition on SLOAD for minimum of one clock cycle for next register write)

Default register values can be read back serially from the SDOUT pin. For serial data read, first send 12 bit DATA_REQUEST on the SDIN pin. The format is as follows:

Table-11: Data Request on SDIN pin

D11	D10-D9	D8-D0
logic'1'	Required register	Don't Care

Although the length of DATA request is 12 bits, the nine LSBs are don't cares. Also the D11 bit should be 1 for register read. The address portion DATA request is decoded and the register data value is available on the SDOUT pin at the rising edge of the clock if SLOAD is low at that time.

PROGRAMMABLE GAIN FUNCTIONALITY

PGA has an exponential gain control from gain 1 to 6 in 64 steps. In dB scale gain is varied from 0 to ~16.5 dB with ~0.258 dB per step.

Table-12: PGA Gain Vs Gain Register Value

Gain Register Value	Gain Value
000000 . . . 111111	1 . . . 6.7

OFFSET CORRECTION FUNCTIONALITY

DAC output varies from -60mV to +60mV when we move from all zero to all one code.

Table-13: Offset Register Description

Offset Register Value	Offset Value
0000000000 . . 100000000 . . 111111111	-60 mV . . 0 . . +60mV

PROGRAMMABLE DELAY REGISTER FUNCTIONALITY

The 5-bit Programmable delay Register will produce delay in CDSCLK1, CDSCLK2 and CLOCK individually in step of 1ns typical. First two bits are used to select the CDSCLK1, CDSCLK2 or CLOCK and remaining three bits provide delay in eight steps.

Table-14: 12-bit Serial Data

SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
RD/WR	Logic '1'	Logic '1'	X	X	X	X	D4	D3	D2	D1	D0

Table-15: Selection bits for Programmable Delay Register

SI NO	Programmable delay Register		Selection of the Line for delay
	D4	D3	
1	0	0	NO-Delay
2	0	1	CDSCLK1
3	1	0	CDSCLK2
4	1	1	CLOCK

Table-16: Programmable Delay Register setting for delay

SI NO	Programmable Delay Register		
	D2	D1	D0
1	0	0	0
2	0	0	1
3	0	1	0
4	0	1	1
5	1	0	0
6	1	0	1
7	1	1	0
8	1	1	1

Note4: D2, D1, D0 are not programmable in case of NO-Delay selection.

TYPICAL TIMING DIAGRAM

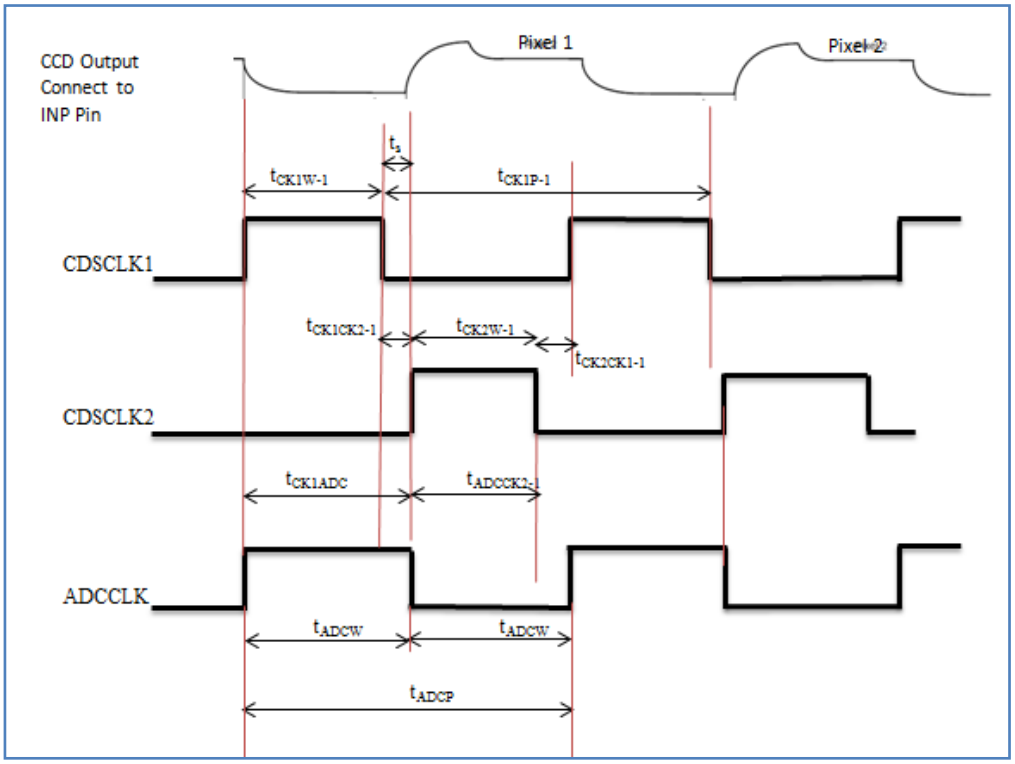

Figure-*5:* Typical timing diagram for CCD analog signal processor in case of **Single Ended Operation**
(CCD Output shown in the figure is connected to **INP** Pin of CSP ASIC)
(**INN** pin should be connected to AGND pin through 0.47uF AC coupling Capacitor)

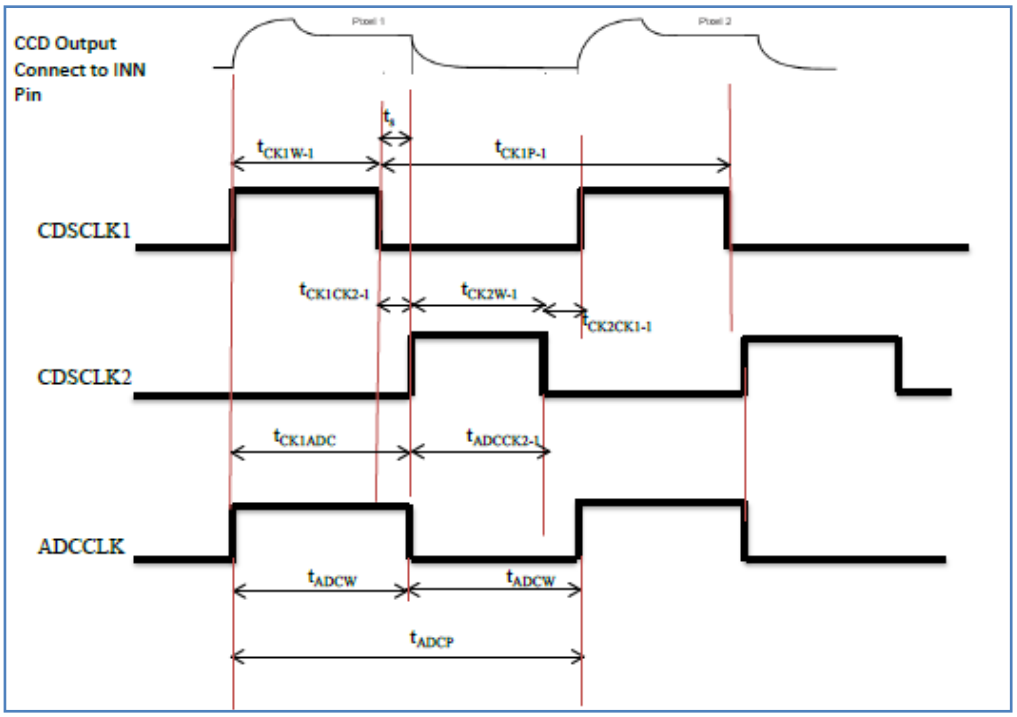

Figure-*6:* Typical timing diagram for CCD analog signal processor in case of **Single Ended Operation**
(CCD Output shown in the figure is connected to **INN** Pin of CSP ASIC)
(In this case of Single Ended **INP** pin should be connected to AGND pin through 0.47uF AC coupling Capacitor)

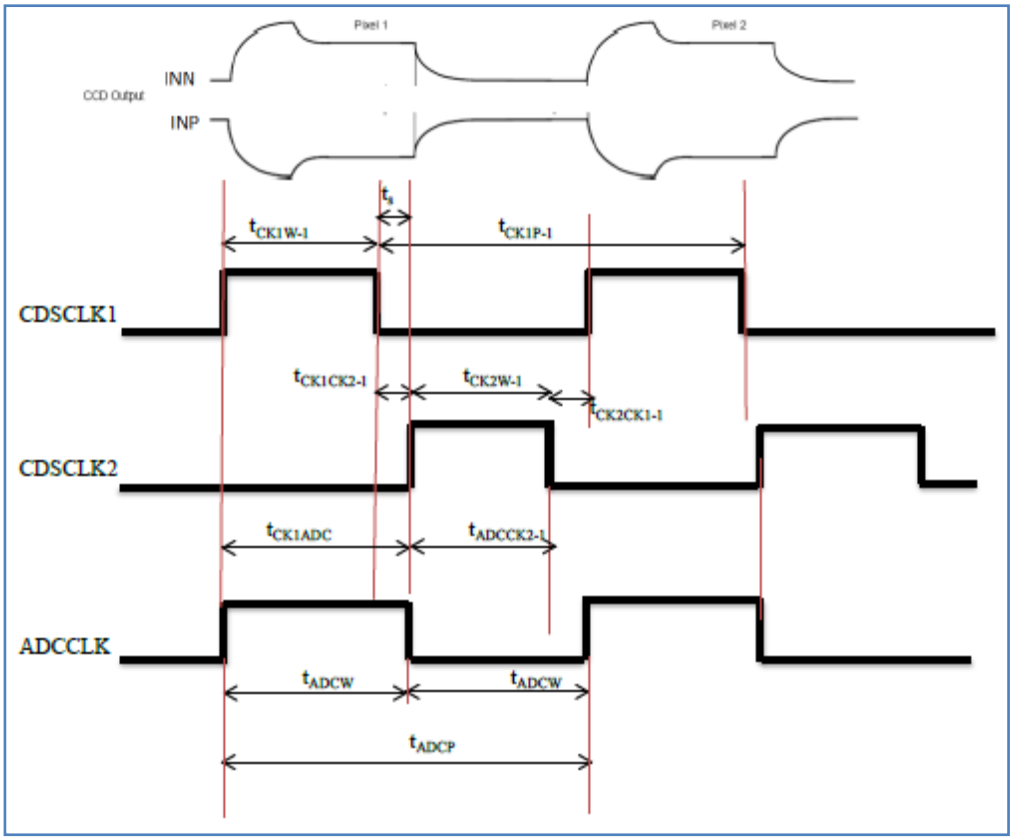

Figure-7: Typical timing diagram for CCD analog signal processor with CCD Output in **Differential Mode**

Note5: Please refer (Table 2 Pin Configuration, Page No 4) for CDSCLK1 and CDSCLK2 functionality for CCD input applied at INP or INN or in Differential mode.

Table-17: Typical timings for best performance with 10MSPS Data Rate

Symbol	Parameter	Min	Unit
t_{CK1P-1}	Conversion Rate	100	ns
t_{CK1W-1}	CDSCLK1 Pulse Width	40	ns
t_{CK2W-1}	CDSCLK2 Pulse Width	40	ns
$t_{CK1CK2-1}$	CDSCLK1 Falling to CDSCLK2 Rising	5	ns
$t_{CK2CK1-1}$	CDSCLK2 Falling to CDSCLK1 Rising	5	ns
t_{CK1ADC}	CDSCLK1 Rising to ADCCLK Falling	50	ns
$t_{ADCCK2-1}$	ADCCLK Falling to CDSCLK2 Falling	40	ns
t_{ADCW}	ADCCLK Pulse Width	50	ns
t_{ADCP}	ADCCLK Period	100	ns
t_S	Sampling Delay	5	ns

Total pipeline delay for CSP ASIC is 9 clock cycles (9T).

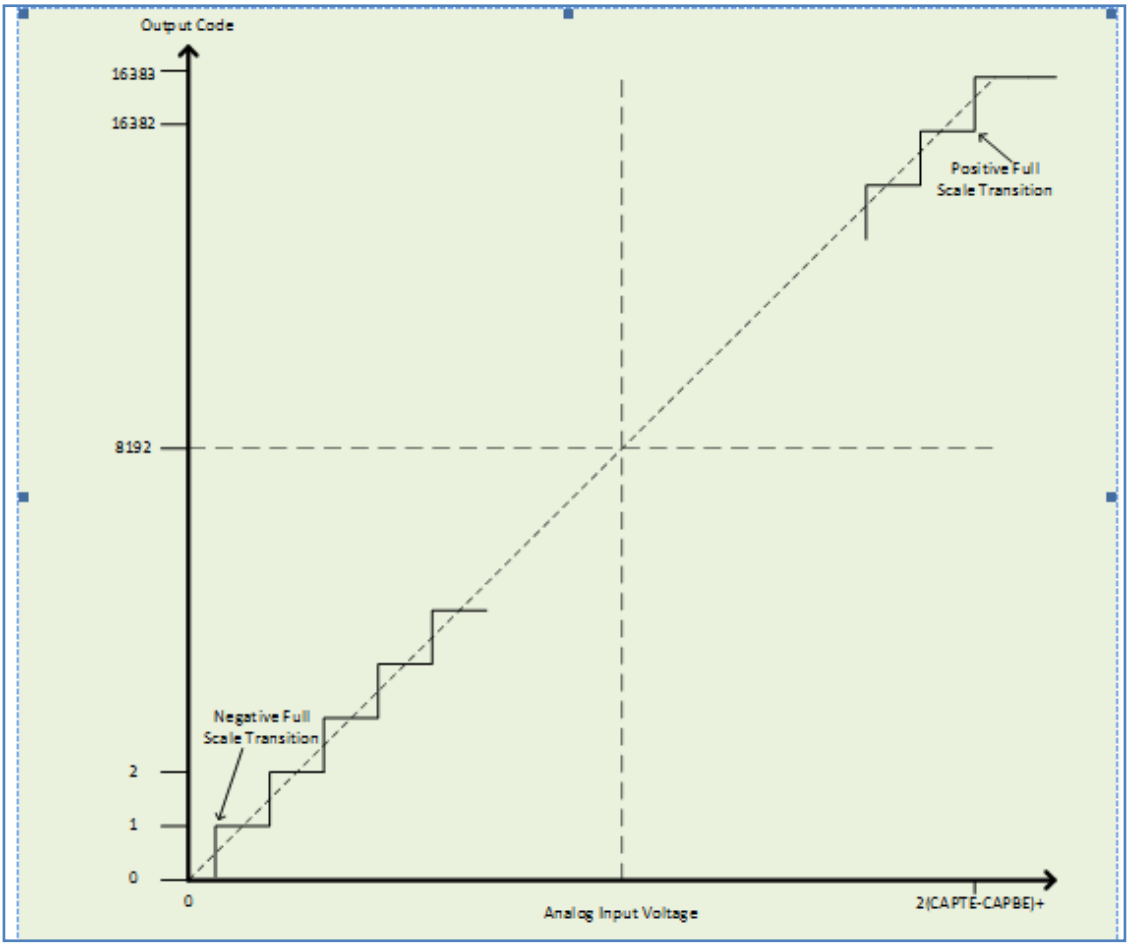

Figure-8: Transfer Characteristics of CSP ASIC

TYPICAL CHARACTERISTICS:

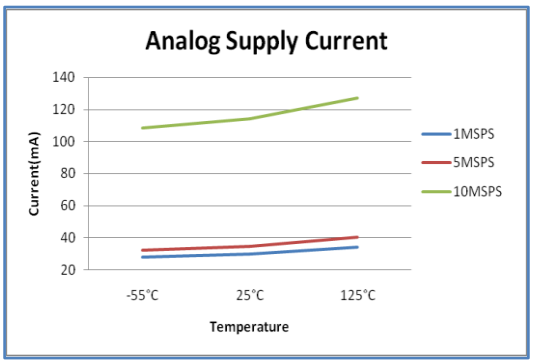

Figure-9: Dynamic Analog Supply Current

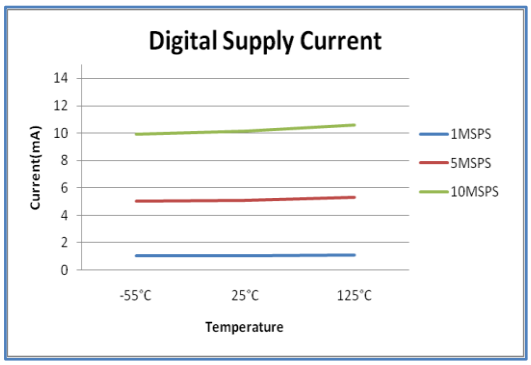

Figure-10:Dynamic Digital Supply Current

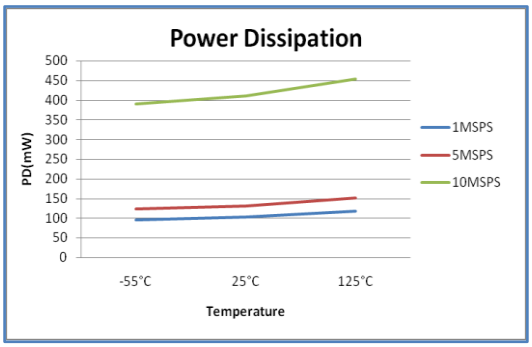

Figure-11: Dynamic Power Dissipation

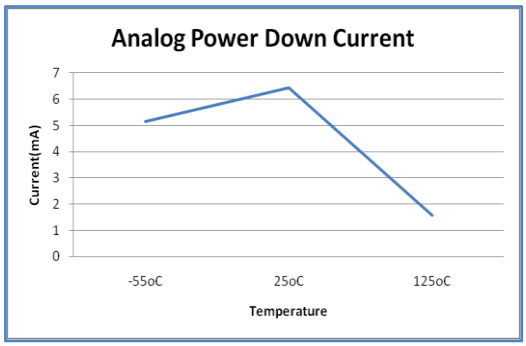

Figure-12: Power Down Analog Supply Current

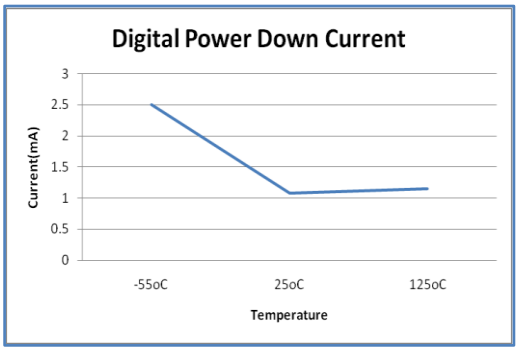

Figure-13: Power Down Digital Supply Current

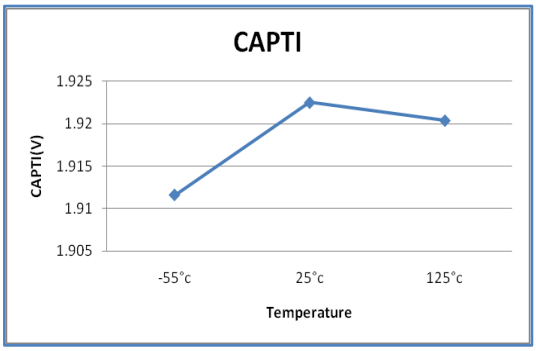

Figure-14: CAPTI Voltage

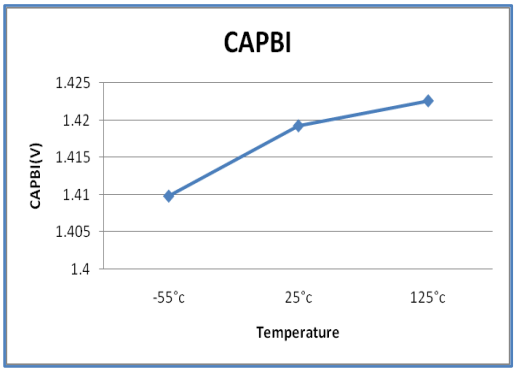

Figure-15: CAPBI Voltage

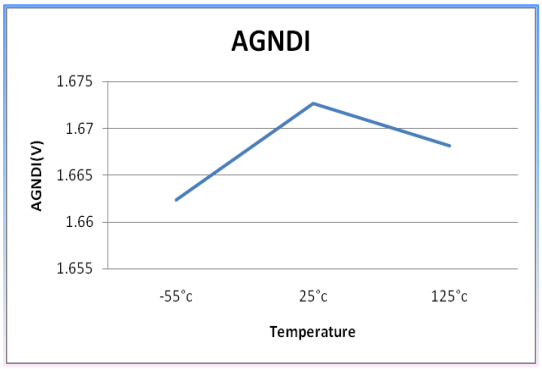

Figure-16: AGNDI Voltage

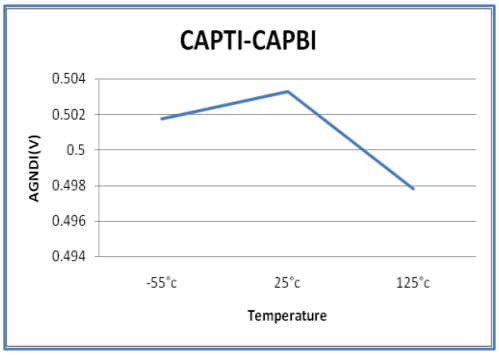

Figure-17: CAPTI-CAPBI

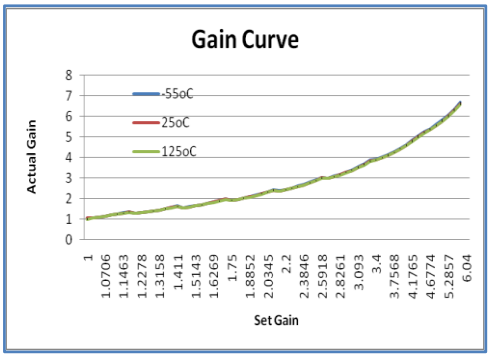

Figure-18: PGA Gain Curve

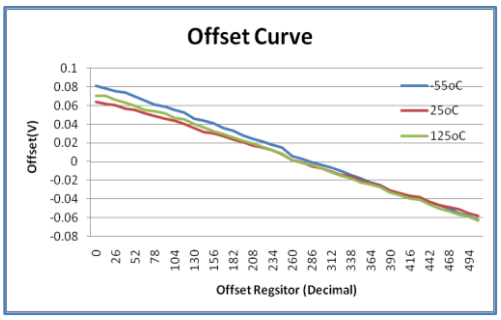

Figure-19: Offset Correction Curve

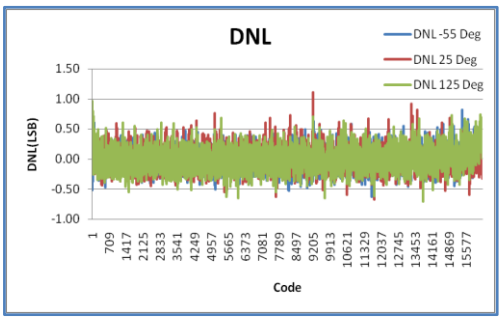

Figure-20:DNL Plot

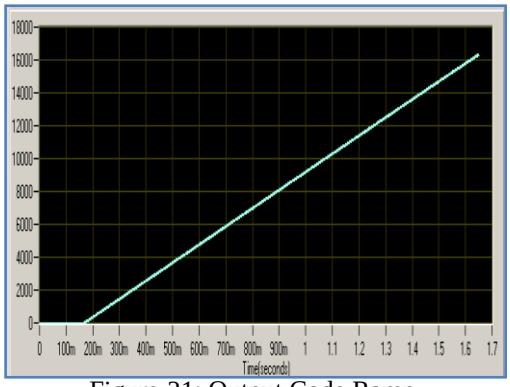

Figure-21: Output Code Ramp

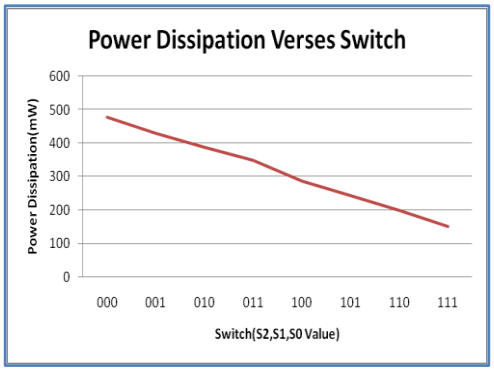

Figure-22: Power Dissipation Verses Switch Value

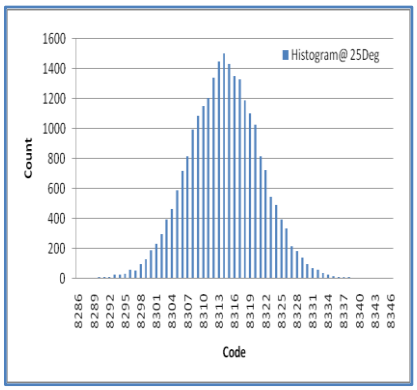

Figure-23:Histogram Plot of o/p with Analog Grounded i/p at 25°C

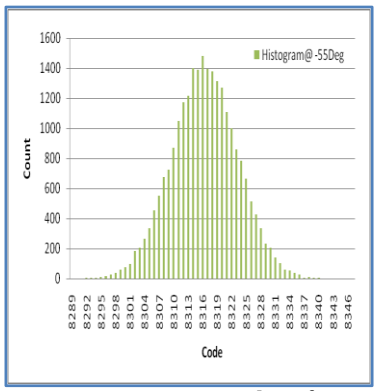

Figure-24:Histogram Plot of o/p with Analog Grounded i/p at -55°C

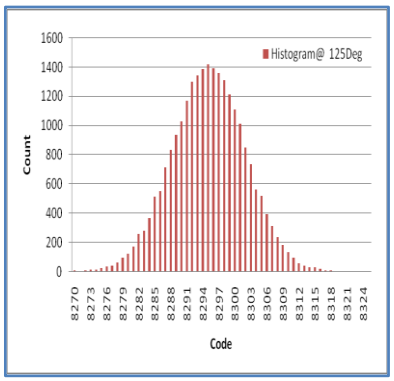

Figure-25:Histogram Plot of o/p with Analog Grounded i/p at 125°C

OVERVIEW:

A typical CCD analog signal processor (CSP) starts with an input clamp driven through an off chip coupling capacitor (CIN). AC coupling is recommended because the DC level of the CCD output signal is usually too high (several volts) for the CDS to work properly. The input clamp restores the dc level of the signal to an optimum point within the supply range of the CCD analog signal processor (CSP). A 0.47-µF capacitor is recommended for C_{IN}; however, it depends on the application environment. The analog input signal range at the CCD IN pin is 1 V_{P-P}, and the appropriate common mode voltage for the CDS is around 1.65V. A sampling function follows the input clamp. CSP is designed to work with CCD with correlated double sampler (CDS). The CDS takes two samples of each pixel, one at the reset level and one at the video level, and performs a differential measurement between the two. The CDS improves the signal-to-noise ratio (SNR) by eliminating the correlated noise associated with the output stage of the CCD, and by attenuating low frequency drift. A black-level offset-correction stage is integrated with the CDS. A programmable- gain amplifier (PGA) follows the CDS to amplify the signal to better utilize the full dynamic range of the A/D converter (ADC). If the black-level offset correction is not performed ahead of the PGA, the dynamic range of the imaging system will suffer. A high performance high-speed ADC (13 stage pipeline architecture) converts the conditioned analog signal to the digital domain, allowing for additional processing by another digital ASIC. The CSP is programmed via a 4-wire serial interface (up to 20MHz).

ANALOG INPUT (INP, INN):

In differential ended 1Vpp input range means INP will vary from 1.65 to 2.15 and at the same time INN will vary from 1.65 to 1.15V. In Single ended 1Vpp input range means INP will vary from 1.15 to 2.15 (if common mode level is 1.65V) and at the same time INN will connect to common mode level of 1.65V.

DEFINITIONSOF KEY SPECIFICATIONS:

• **Differential Nonlinearity (DNL):** An ideal CSP exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Therefore, every code must have a finite width. No missing codes guaranteed to 14-bit resolution indicate that all 16384 codes must be present overall operating conditions.

• **Input Referred Noise:** The noise is measured using histogram techniques. The standard deviation of the CSP output codes is calculated in LSB and represents the rms noise level of the total signal chain . The noise can be converted to an equivalent voltage, using the relationship

$$1\ \text{LSB} = (\text{ADC full scale} / 2^N\ \text{codes})$$

Where N is the bit resolution of the CSP. 1 LSB is approximately 61.0µV.

• **Effective Resolution:** The ratio of the full-scale input range to the rms input noise (from grounded input histogram test) is called as effective resolution.

$$\textit{Effective resolution} = \log_2\left(\frac{2^N}{\textit{rms input noise}\,(\textit{LSBs})}\right)$$

RMS Input Noise = Standard deviation from Grounded input Histogram Curve

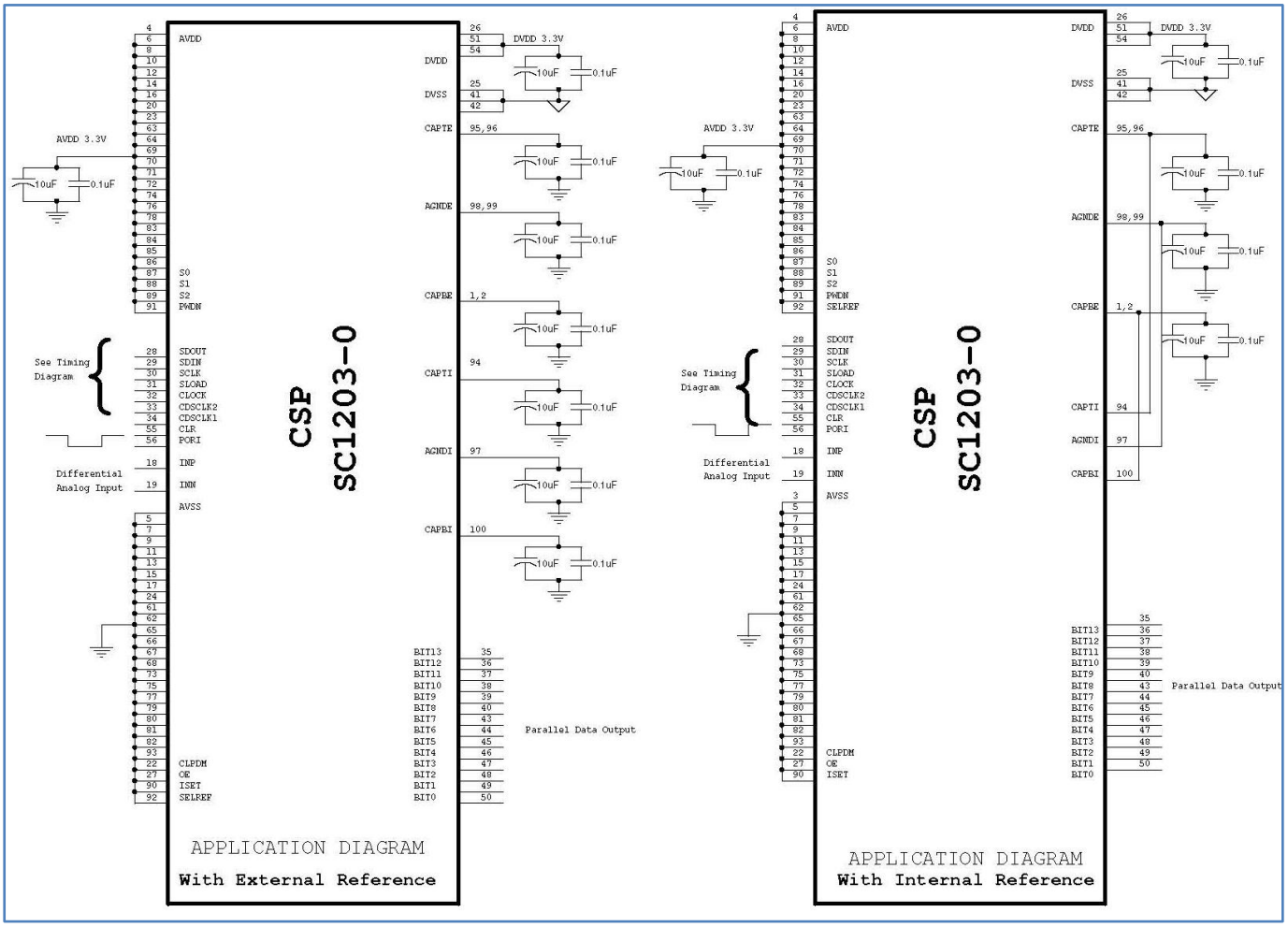

Figure-26: Application Diagram

Note6: S2,S1,S0=Logic 1 for data rate up to 5MSPS
: S2,S1,S0=Logic 010 for data rate > 5MSPS

PACKAGE DRAWING (100 Pin CQFJ):

Note7: All linear dimensions are in inches (mm.)

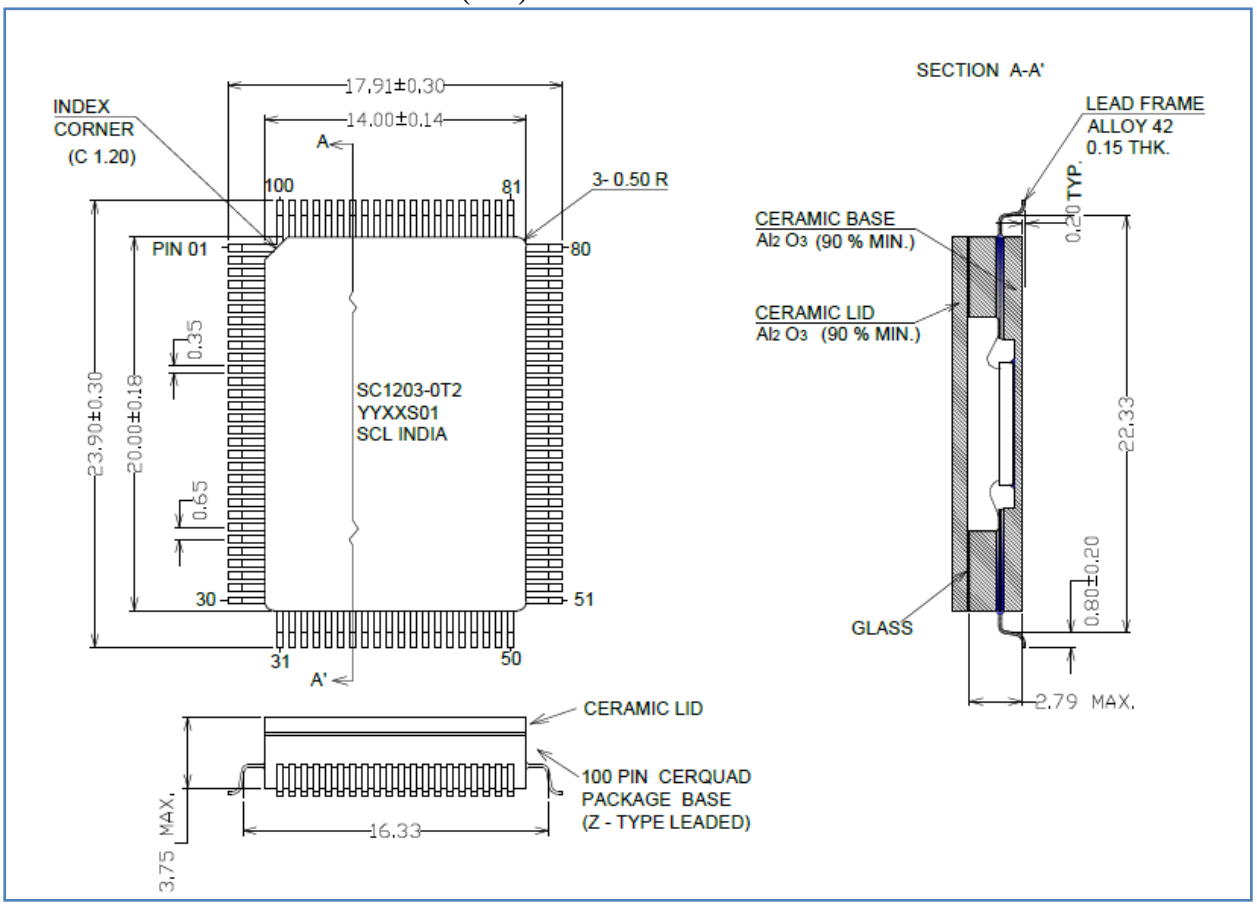

Figure-27: Package Drawing

Revision History			
S.No.	**Version**	**Date of release**	**Description**
1	1.0	September 20, 2020	
2	2.0	September 20, 2021	1. Programmable delay Register Functionality added. 2. Timing diagrams for single ended operation at INP and INN pin added.
3			
4			

DISCLAIMER