QUAD 2-INPUT NAND

SCHMITT-TRIGGER (5V)

<u>SC1125-0</u>

(Radiation Hardened)



DATA SHEET (Version 1.0, March 2020)



Semi–Conductor Laboratory Government of India S.A.S. Nagar, Punjab-160071 www.scl.gov.in



PRODUCT DESCRIPTION:

SC1125 is a Radiation Hardened Quad Two input NAND gate with Schmitt trigger action on both inputs. Schmitt trigger is a comparator which triggers at different points for positive and negative going signals and the difference between positive voltage (V_T^+) and negative voltage (V_T^-) is the Hysteresis voltage (V_H). All outputs have equal source and sink currents.

APPLICATIONS:

- Wave and pulse shapers
- High-noise-environment systems
- Monostable multivibrators
- Astable multivibrators
- NAND logic

FEATURES:

- Operating Supply Voltage 5V ± 0.5V
- Schmitt-trigger on each input with no external components.
- Noise immunity greater than 50%
- Equal source and sink currents
- No limit on input rise and fall time
- Hysteresis voltage $V_H = 1.6V (V_{DD} = 5.0V)$ $T_A = 25^{\circ}C (Typical)$
- Operating Temperature: -55°C to 125°C
- Radiation Hardened up to 200 KRad TID
- SET/SEL immune up to 50 MeV-cm²/mg
- 14 Pin CSOP / 14 pin CDIP / Customized package options / Die
- Thermal Resistance (CSOP), $\Theta_{\rm JC}$ = 7.47 °C/ W
- Pin compatible with CD4093
- ESD Sensitivity Level: Class 0 (< 250V) HBM
- SCL's 180nm CMOS Technology

DEVICE PIN CONFIGURATION:





PIN DESCRIPTION:

PIN NUMBER	PIN NAME	DESCRIPTION
14	V _{DD}	Positive Power Supply
7	V _{ss}	Ground
1, 2, 5,6, 8,9, 12, 13	A, B, C, D, E, F, G, H	Input
3,4,10, 11	J, K, L, M	Output

FUNCTIONAL TABLE:

TRUTH TABLE OF NAND GATE				
INPUT-1 (A, C, E, G)	INPUT-2 (B, D, F, H)	OUTPUT (J, K, L, M)		
1	1	0		
1	0	1		
0	1	1		
0	0	1		

ABSOLUTE MAXIMUM RATINGS (1):

Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage	-0.5 to 6.5	V
V _{I/O}	Voltage at any Pin	-0.5 to 6.5	V
TJ	Max. Junction Temperature	150	°C
T _{STG}	Storage Temperature	-65 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS:

Symbol	Parameter	Value	Unit	
V _{DD}	Supply Voltage	4.5 to 5.5	V	
V _{IN}	Input Voltage	0 to V_{DD}	v	
I _{OH}	High level output current (Source)	-3.5	m A	
I _{OL}	Low level output current (Sink)3.5		IIIA	
T _A	Operating Temperature	-55 to 125	°C	



DC ELECTRICAL CHARACTERISTICS

Test condition: $V_{DD} = 5V \pm 0.5V$, $V_{SS} = 0V$, $T_{AMB} = -55^{\circ}C$ to $+125^{\circ}C$ (unless otherwise specified)

	D	Test Cardttes	Test Limits			
Symbol	Parameter	l est Condition	Min.	Typ. ¹	Max.	Unit
I _{DD}	Static Supply Current	$V_{IN} = V_{SS}$ or V_{DD}	-	0.1	3.0	uA
I _{IL}	Input Gate Leakage Current Low	$V_{DD}=5.5V$ $V_{IN}=V_{SS}$	-	±20	-100	nA
I _{IH}	Input Gate Leakage Current High	V_{DD} =5.5V $V_{IN} = V_{DD}$	-	±20	100	nA
Vor	V _{OL} Output Voltage Level Low	V _{DD} =5.0V (No Load)	-	0.01	0.05	V
• OL		$V_{DD}=5.0V$ (I _{OL} = 3.5mA)	-	0.2	0.4	V
V	Output Voltage	V _{DD} =5.0V (No Load)	4.95	4.99	V _{DD}	V
Vон Level High	Level High	$V_{DD}=5.0V$ ($I_{OH}=-3.5mA$)	4.6	4.75	V _{DD}	V
V _{T+}	Positive going threshold voltage ¹	$V_{DD} = 5.0V$ $V_{IN1} = V_{RAMP} (0 \text{ to } V_{DD})$	2.2	3.2	3.6	V
V _{T-}	Negative going threshold voltage ¹	$w_{DD} to 0)$ $V_{IN2} = V_{DD}$ and	0.9	1.5	2.8	V
V _H	Hysteresis Voltage ² $V_{H} = (V_{T+}-V_{T-})$		0.6	1.6	2.0	V
Functional	Verify Truth Table without Load	$\begin{split} V_{DD} = 5V \pm 0.5V \\ Functional Verification at 1 MHz \\ V_{IL} = 0V, V_{IH} = V_{DD} \\ V_{OH} \ge V_{DD} - 0.5V, V_{OL} \le 0.5V \end{split}$				

¹ Typical Values are measured at V_{DD} =5.0V, T_{AMB} = 25°C

 2 IN1 = B, D, F and H and IN2 = A, C, E and G.



AC ELECTRICAL SPECIFICATIONS:

Test condition: $V_{DD}=5.0V$, $V_{IL}=0V$, $V_{IH}=5V$, (t_R and $t_F \le 15$ ns), Duty Cycle = 50%, $T_{AMB} = -55$ °C to 125 °C, Load: $C_L=30$ pf

Symbol	Parameter	Test Results			
Symbol		Min.	Typ. ³	Max.	Units
t _{PHL}	Propagation Delay Time (High to Low)	-	15	50	ns
t _{PLH}	Propagation Delay Time (Low to High)	-	15	50	ns
T _{THL}	Output Transition Time (High to Low)	-	5	-	ns
T _{TLH}	Output Transition Time (Low to High)	-	5.5	-	ns

³ Typical Values are measured at V_{DD} =5.0V, T_{AMB} = 25°C

TEST CIRCUIT AND SWITCHING WAVEFORM:



HYSTERESIS CURVE:

Test Conditions:

 V_{DD} =5V, V_{IN1} =5V & V_{IN2} = Square wave (20 ns rise / fall time), freq. = 1MHz, Amplitude = 5 V_{PP}





ELECTRICAL CHARACTERISTICS:





RADIATION CHARACTERISTICS:



Total Ionization Dose (TID)

TID Test Conclusion:

- No significant change in supply current observed upto 100 Krad. Typical I_{DD} remains within 500 nA at 200 Krad which is well within specifications.
- There is no substantial change in device parameters (leakages, output levels, hysteresis voltage) up to 200KRad.
- The device is fully functional up to 200 Krad.

Single Event Effect (SEE)

Single Event Effects	LET in Si (MeV-cm2/mg)		
Single Event Effects	22.9	50.7	
Transient (SET)	PASS	PASS	
Latch-Up (SEL)	PASS	PASS	

SEE Test Conclusion:

- SEE testing of Quad 2-Input NAND Schmitt Trigger (SC1125-0) is done at two different LET 22.9 & 50.7 MeV-cm2/mg for a fluence of 10⁶ ions/cm².
- No transient and Latch-up observed during irradiation.
- The Device is passed in SET, SEL up to LET of 50 MeV-cm2/mg.





MECHANICAL DRAWING OF PACKAGE (14 PIN FLAT PACKAGE)

IMPORTANT NOTICE

Semi Conductor Laboratory (SCL) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and specifications, and to discontinue any product. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. Reproduction of significant portions of SCL information in SCL data sheets is permissible only if reproduction is without alteration and is accompanied by all associated conditions, limitations, and notices. SCL is not responsible or liable for such altered documentation.