16-BIT TRANSCEIVER 3-STATE OUTPUT (COLD SPARING, HOT INSERTION & 5V TOLERANT INPUT) (SC1124-0)

(Radiation Tolerant)

DATA SHEET

Version 1.1, Dec' 2020

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PRODUCT DESCRIPTION:

SC1124-0 16-bit Transceiver is designed for low-voltage (V_{DD} =3.3V) operation, but with the capability to provide a TTL interface to a 5V system environment. These devices can be used as two 8-bit Transceivers or one 16-bit Transceiver. These devices provide true outputs and symmetrical active-low output-enable ($\overline{OEB}$) inputs.

The A port outputs includes equivalent 22 Ω series resistors to reduce overshoot and undershoot.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pull down resistors with the bus-hold circuitry is not recommended.

When V_{DD} is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down.

However, to ensure the high-impedance state above 1.5 V, ($\overline{OEB}$) should be tied to V_{DD} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for hot-insertion applications using Ioff and power-up 3-state. The I_{OFF} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

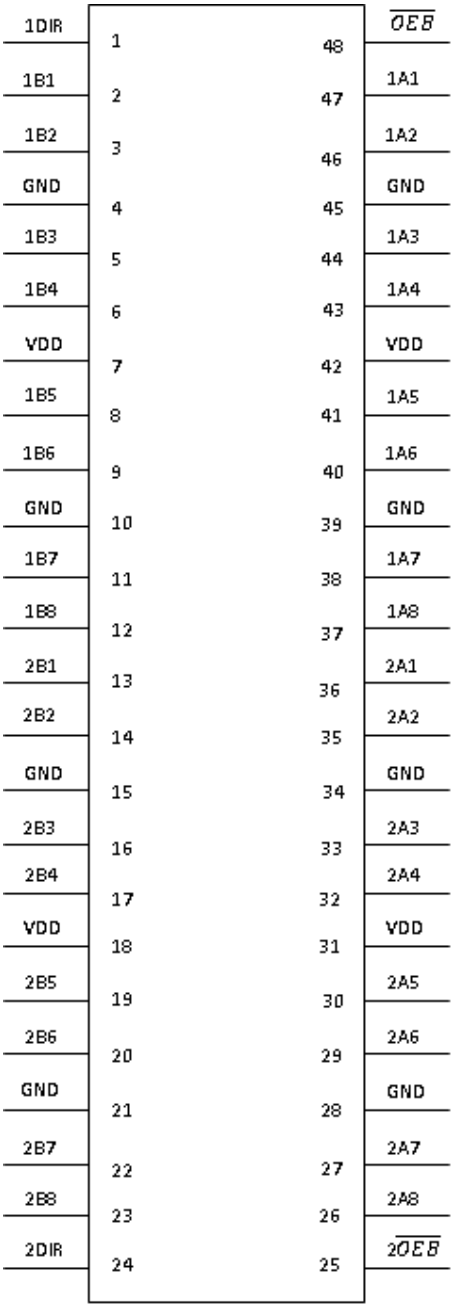
FEATURES:

- **Operating Power Supply 3.3V ±0.3V**
- **Cold sparing feature at I/O**
- **A port outputs have equivalent 22 Ω series resistors, so no external resistors are required.**
- **5V tolerant inputs for interfacing 5V logic with 3.3V V_{DD}**
- **I_{OFF} and power-up 3-state support hot Insertion**
- **Bus Hold on data inputs eliminates the need for external pull-up / pull-down resistors**
- **Distributed V_{DD} and GND pins minimize high-speed switching noise**
- **Flow-through architecture optimizes PCB layout**
- **6.0 ns typical propagation delay**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{DD} = 3.3 V, T_A = 25°C**
- **Low power dissipation (<1mW at 3.6V static)**
- **Operating Temperature: -55ºC to 125ºC.**
- **Radiation Tolerant up to 100 KRad**
- **SET/SEL immune up to 50 MeV.cm²/mg**
- **48 Pin CDFP /Customized package /Die**
- **Pin compatible with LVTH162245.**
- **Package Θ_{JC} = 2.7ºC/Watt**
- **ESD Sensitivity Level: HBM Class 1A (250V to 499V), passed up to 300V**
- **SCL's 180nm CMOS Technology**

PIN CONFIGURATION:

Pin no.	Signal	Pin no.	Signal
1	1DIR	**25**	$2\overline{OEB}$
2	1B1	**26**	2A8
3	1B2	**27**	2A7
4	GND	**28**	GND
5	1B3	**29**	2A6
6	1B4	**30**	2A5
7	VDD	**31**	VDD
8	1B5	**32**	2A4
9	1B6	**33**	2A3
10	GND	**34**	GND
11	1B7	**35**	2A2
12	1B8	**36**	2A1
13	2B1	**37**	1A8
14	2B2	**38**	1A7
15	GND	**39**	GND
16	2B3	**40**	1A6
17	2B4	**41**	1A5
18	VDD	**42**	VDD
19	2B5	**43**	1A4
20	2B6	**44**	1A3
21	GND	**45**	GND
22	2B7	**46**	1A2
23	2B8	**47**	1A1
24	2DIR	**48**	$1\overline{OEB}$

Package Pin Details



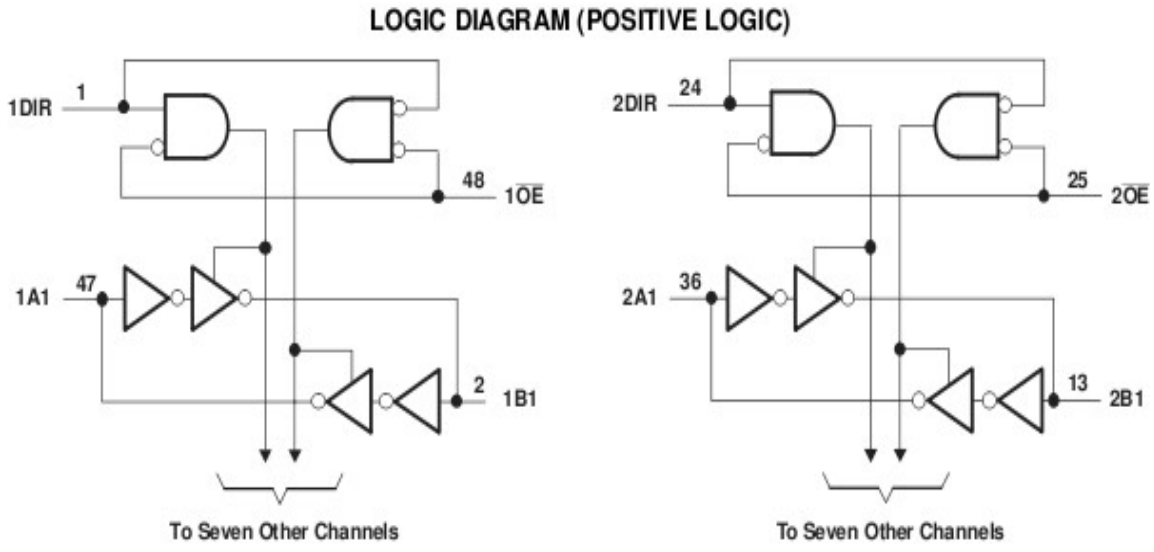
Device Package View

FUNCTIONAL TABLE:

CONTROL INPUTS		OUTPUT CIRCUITS		OPERATION
$\overline{OEB}$	DIR	A PORT	B PORT	
L	L	Enabled	Hi-Z	B data to A bus
L	H	Hi-z	Enabled	A data to B bus
H	X	Hi-z	Hi-Z	Isolation

Truth table

LOGIC DIAGRAM (POSITIVE LOGIC):



Device Logic Diagram

ABSOLUTE MAXIMUM RATINGS (1):

Over operating free-air temperature range (unless otherwise noted),

PARAMETER	UNIT
Supply Voltage Range (V_{DD})	–0.5 V to 4.3V
Input Voltage Range (V_{IN})	–0.5 V to 6.5V
Output Voltage Range In High Impedance or Power Off (V_{OUT})	–0.5 V to 4.3V
Output Voltage Range Applied In High State (V_{OUT})	–0.5 V to V_{DD} + 0.5 V
Max. Junction Temperature (T_J)	150°C
Storage Temperature Range (T_{STG})	–65°C to 150°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS:

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage		3.0	3.3	3.6	V
V_{IH}	High level input voltage		2.0	-	5.5	V
V_{IL}	Low level input voltage		0	-	0.8	V
I_{OH}	High-level output current	PORT A	-	-	-12	mA
		PORT B	-	-	-24	mA
I_{OL}	Low-level output current	PORT A	-	-	12	mA
		PORT B	-	-	24	mA
$\Delta t/\Delta V_{DD}$	Power up ramp rate		200	-	-	usec/V
T_A	Ambient Temperature range		-55	-	125	ºC

DC ELECTRICAL SPECIFICATIONS:

Table below shows eelectrical test conditions, test limits and typical measured values.

Test condition: V_{DD}=3.3 ± 0.3V, T_A = -55°C to +125°C

Symbol	Parameter		Test Conditions		V_{DD}	Test Limits			Units
						MIN.	TYP.	MAX.	
I_{IN}	Input Current	Control Pins	V_{IN} = V_{SS} or V_{DD}		3.6V	-	-	±1	µA
			V_{IN} = 5.5V			-	-	±10	
			V_I = 0V or 5.5V		0V		-	±10	
		A or B Ports	V_{IN} = V_{SS} or V_{DD}		3.6V	-	-	±5	µA
			V_{IN} = 5.5V			-	-	±10	
I_{IN} (hold)	Input Bus Hold Current	A or B Ports	V_{IN} = V_{IL} = 0.8V		3.0V	-	120	±200	µA
			V_{IN} = V_{IH} = 2.0V			-	-147	±200	µA
V_{OH}	High Level output Voltage	A Port	V_{IH} = 2V	I_{OH} = -100uA	3.0V	2.8	2.99	-	V
				I_{OH} = -12mA		2.0	2.43	-	
		B Port	V_{IH} = 2V	I_{OH} = -100uA	3.0V	2.8	2.97	-	
				I_{OH} = -8mA		2.4	2.74	-	
				I_{OH} = -24mA		2.0	2.38	-	
V_{OL}	Low Level output Voltage	A Port	V_{IL} = 0.8V	I_{OL} = 100uA	3.0V	-	0.003	0.2	V
				I_{OL} = 12mA		-	0.450	0.8	
		B Port	V_{IL} = 0.8V	I_{OL} = 100uA	3.0V	-	0.005	0.2	
				I_{OL} = 12mA		-	0.314	0.5	
				I_{OL} = 24mA		-	0.641	0.8	
I_{OZH}	Three-State Output Leakage Current High	A Port	$\overline{OEB}$ = Disabled V_O = 3V		3.6V	-	-	±5	µA
		B Port				-	-		
I_{OZL}	Three-State Output Leakage Current Low	A Port	$\overline{OEB}$ = Disabled V_O = 0.5V		3.6V	-	-	±5	µA
		B Port				-	-		
I_{OFF}	Power Off Input Leakage Current	A or B Ports	V_I = 0V or 4.5V		0V	-	-	±50	µA
	Power Off Output Leakage Current	A or B Ports	V_O = 0V or 4.5V		0V	-	-	±50	µA
I_{DD}	Static Supply Current (No Load, Iout =0A)	A Port I/P	V_{IN} = V_{DD} or V_{SS}	Outputs High	3.3± 0.3V	-	0.140	0.25	mA
				Outputs Low		-	0.139		
				Outputs Disabled		-	0.139		
		B Port I/P	V_{IN} = V_{DD} or V_{SS}	Outputs High		-	0.140		
				Outputs Low		-	0.136		
				Outputs Disabled		-	0.139		
ΔI_{DD}	Static Supply Current delta	A Port	One input at V_{DD} – 0.6V Other input at V_{DD} or V_{SS}		3.0 V and 3.6 V	-	24.9	100	uA
		B Port				-	24.3	100	
Basic Functional Test		A Port	V_{IL}=0.8V, V_{IH}=2.0V V_{OL} ≤0.4V, V_{OH} ≥2.4V		3.3 ± 0.3V	-	-	1	Mhz
		B Port							
Functional Test 5V Tolerant		A Port	V_{IL}=0V, V_{IH}=5.5V V_{OL} ≤0.4V, V_{OH} ≥2.4V		3.0V	-	-	1	Mhz
		B Port							

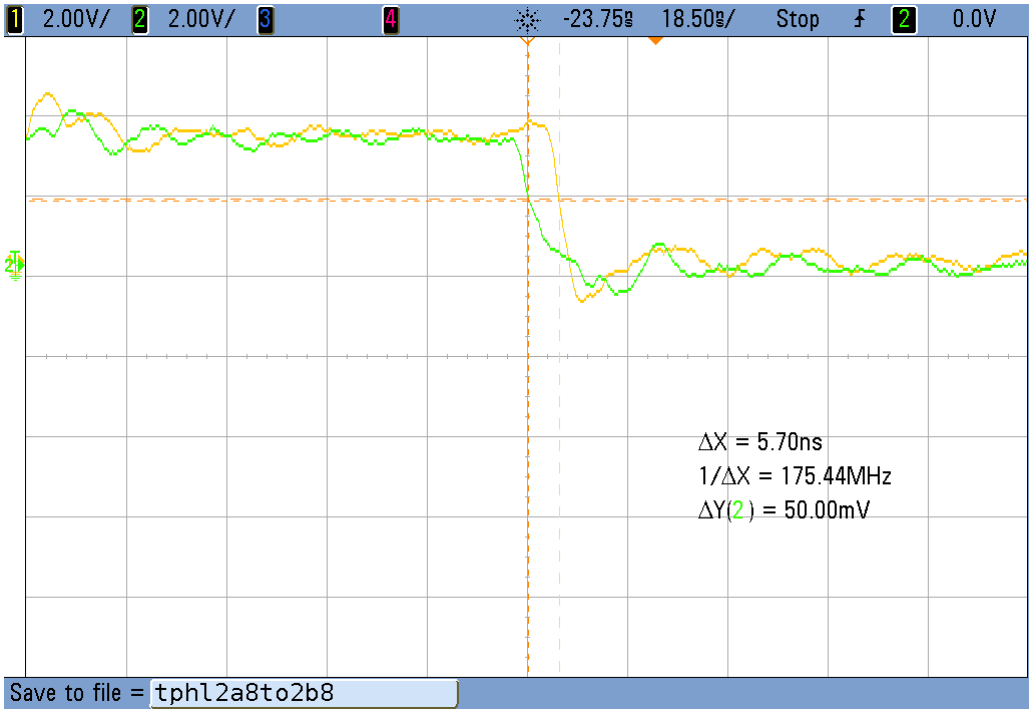
DC Electrical Specification

AC ELECTRICAL SPECIFICATIONS:

Test condition:

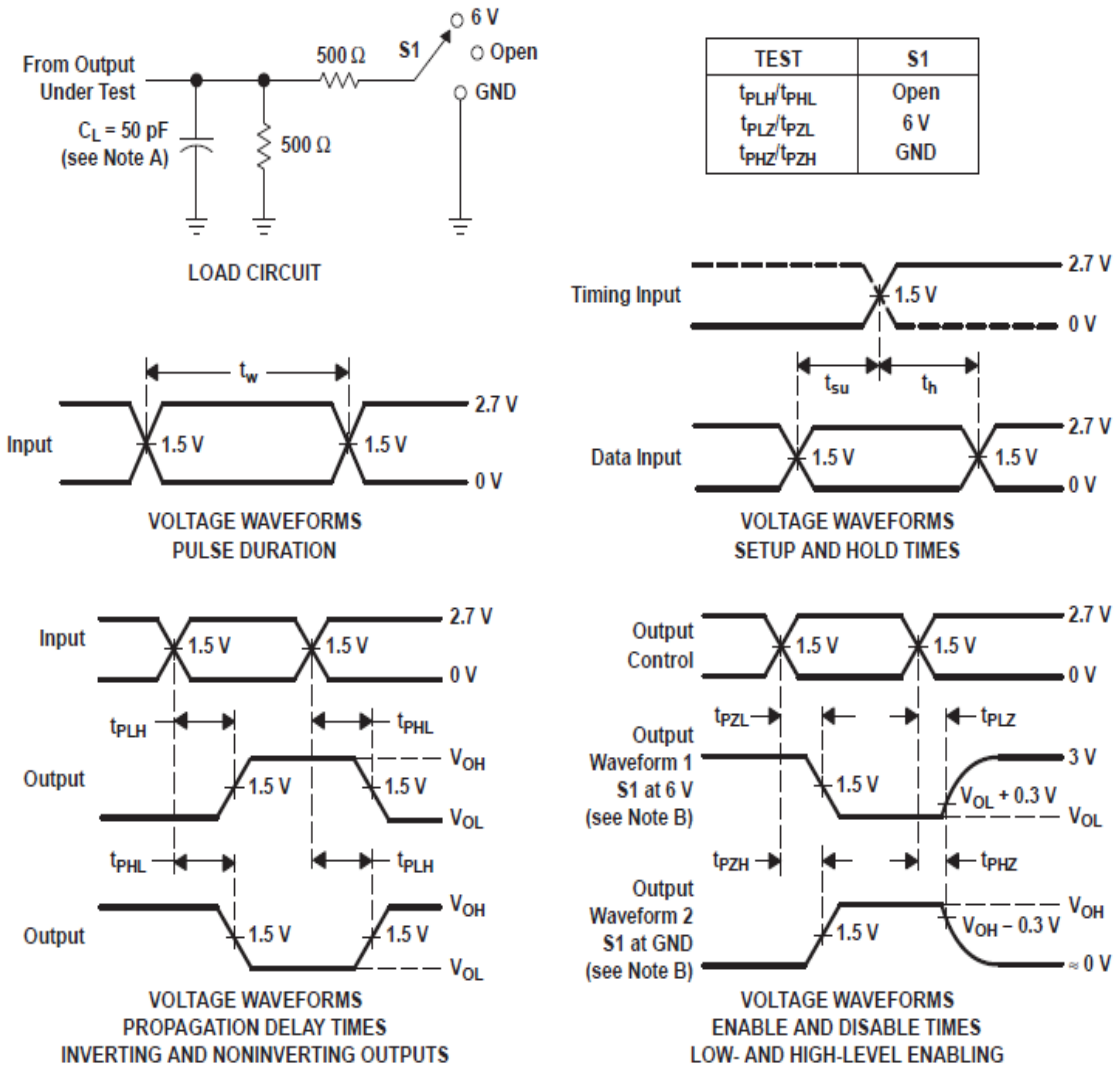
V_{DD}=3.3V, V_{IN} = 0V or 3.3V @1 MHz, R_L=500Ω, C_L = 50pF, T_A = 22 ± 3°C

Parameter	From	To	V_{DD} = 3.3 V			Units
			Min.	Typ.	Max.	
t_{PLH}	A	B	-	5.23	10	ns
t_{PHL}			-	5.30	10	ns
t_{PLH}	B	A	-	6.24	10	ns
t_{PHL}			-	6.31	10	ns
t_{PZH}	$\overline{OEB}$	B	-	5.22	-	ns
t_{PZL}			-	4.86	-	ns
t_{PHZ}			-	4.16	-	ns
t_{PLZ}			-	4.68	-	ns
t_{PZH}	$\overline{OEB}$	A	-	5.74	-	ns
t_{PZL}			-	5.20	-	ns
t_{PHZ}			-	5.02	-	ns
t_{PLZ}			-	5.51	-	ns



Propagation Delay (A to B) t_{PHL}

TEST CIRCUIT AND SWITCHING WAVEFORM:



AC parameter measurement information

NOTES:

A: CL includes probe and jig capacitance
B: Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

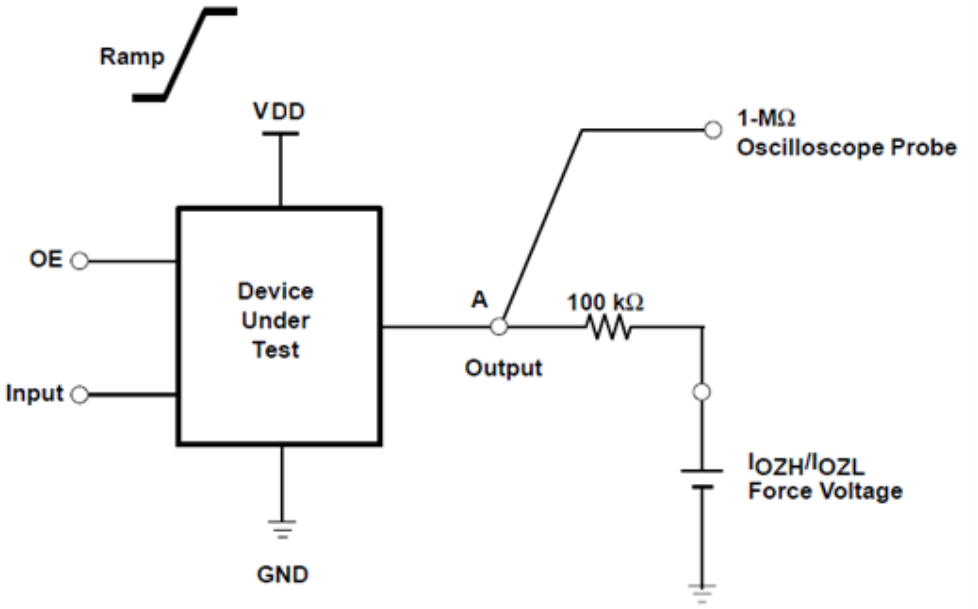
COLD SPARING (IOFF) TEST:

In cold sparing I/O when V_{DD} is down to zero volt, I/Os will go in the high-impedance state so that damage to the device does not occur.
Ioff protection circuitry ensures that no excessive current is drawn from or to an input, output, or combined I/O that is biased to a specified voltage while the device is powered down. This condition can occur when subsections of a system are powered down (partial power down) to reduce energy consumption. All standard logic devices with the I_{OFF} specification allow only 100 uA of maximum current. Any current in excess of this amount (for example, a forward-biased p-n junction) is not considered normal leakage current.

PU3S (Power Up Tri State) HOT INSERTION TEST:

Testing of power-up three-state (PU3S) circuits was done at nominal temperature and voltage. All devices tested have a nominal V_{DD} of 3.3 V.

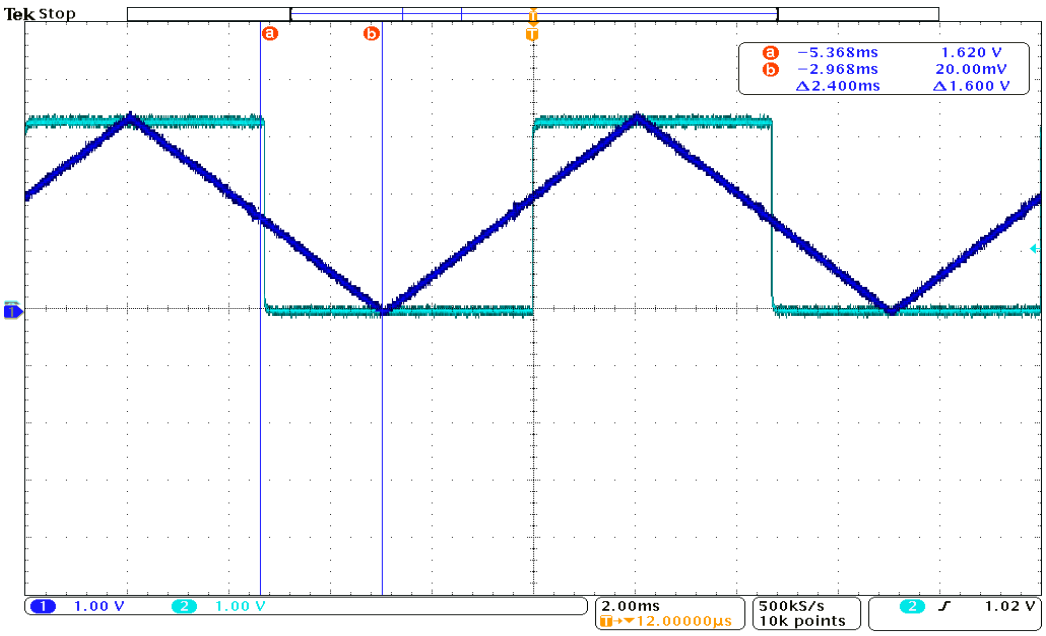
The test setup is shown below. The V_{DD} was ramped at ramp rate (> 200usec / V) to determine the effect of the V_{DD} ramp rate on the device output or I/O structure. I_O was not measured directly; instead the voltage was measured at the output or I/O terminal (terminal A in Figure 1) with a 1-MΩ oscilloscope probe.

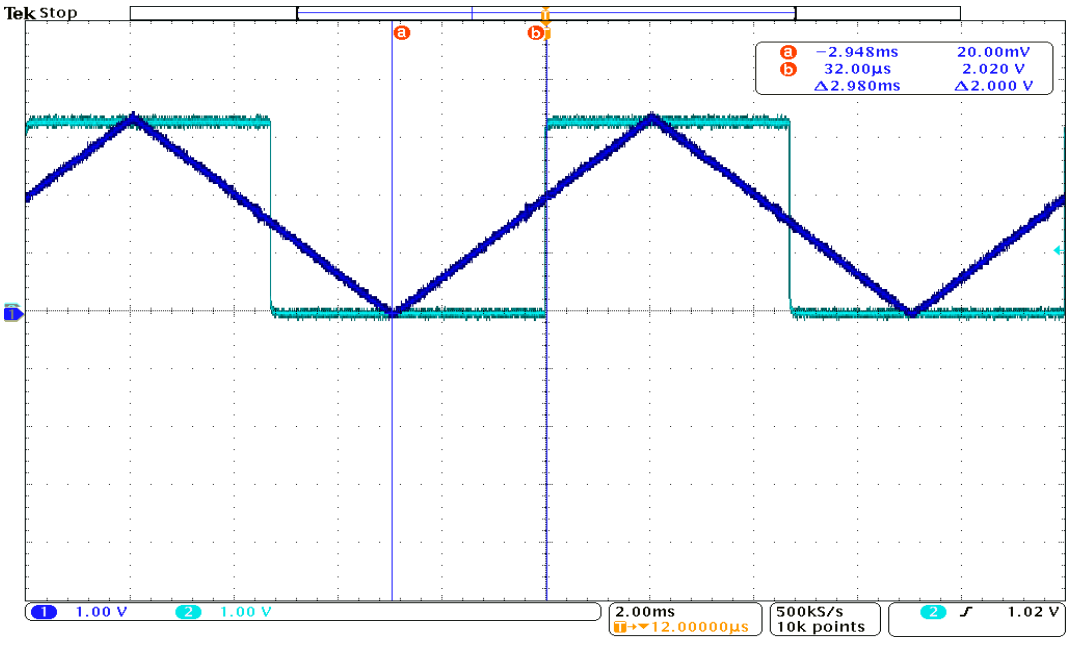


Test circuit (PU3S)

HOT INSERTION TEST

Conditions: $\overline{OEB}$ = LOW (Enable), I/P = Low (0V), O/P = 3.3V through 1KΩ resistor





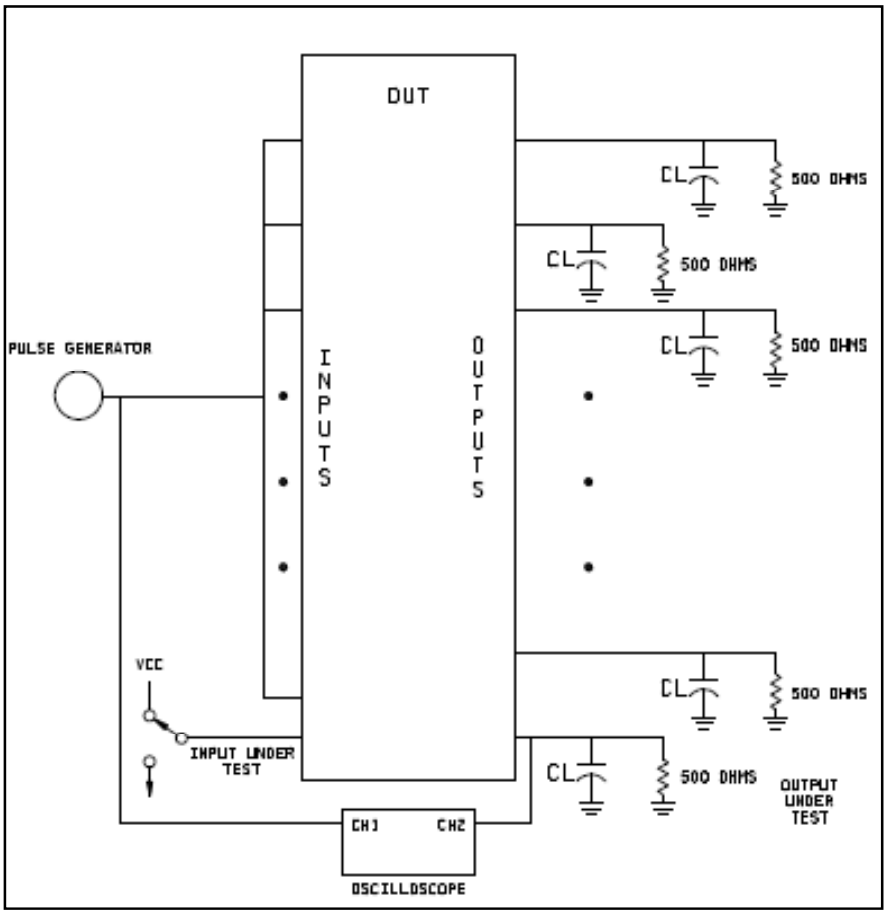
V_{OZH} at supply V_{DD} (ramp rate: 1msec/V), O/P is in HighZ with V_{DD} <1.5V

GROUND BOUNCE AND V_{DD} BOUNCE:
(MIL-STD-883E METHOD 3024)

A. **Ground bounces noise:** The voltage amplitude (peak) of extraneous signals present on a low-level non-switching output with a specified number of other outputs switching. Ground bounce noise on a logic low output can be of sufficient amplitude to exceed the high level threshold of a receiver, or cause latch-up on unprotected CMOS inputs.

B. **V_{DD} bounce noise:** The voltage amplitude (peak) of extraneous signals present on a high-level non-switching output with a specified number of other outputs switching. VCC bounce on a logic high output can be of sufficient amplitude to exceed the low level threshold of a receiver, or cause latch-up on unprotected CMOS inputs.

Ground bounce and V_{DD} bounce tests were done at nominal temperature and voltage.
All devices tested have a nominal V_{DD} of 3.3 V. The output condition for pin under test is to a low level for Ground bounce and to a high level for V_{DD} bounce test and the other outputs were switching. The test setup is shown below;

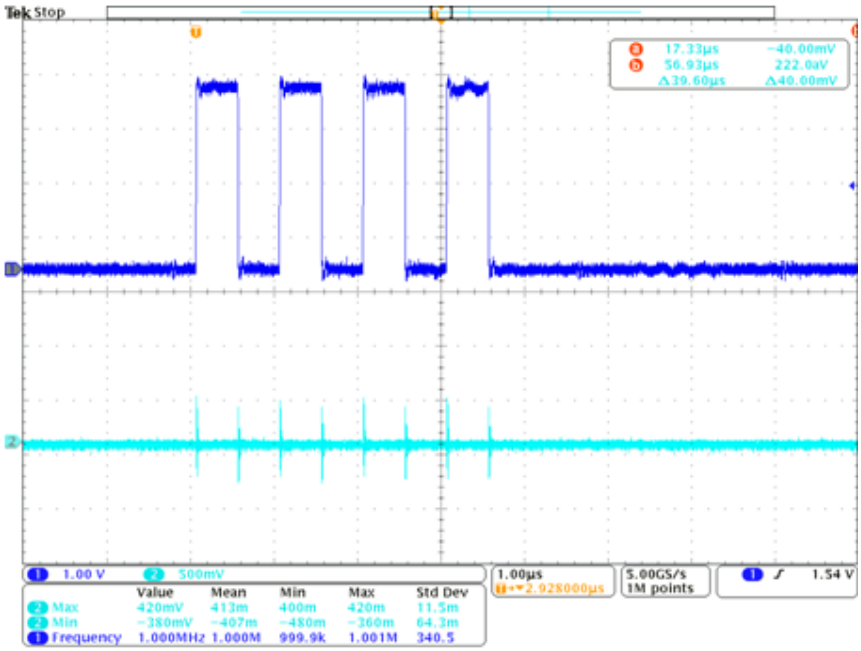


Test Circuit (Ground /VDD Bounce)

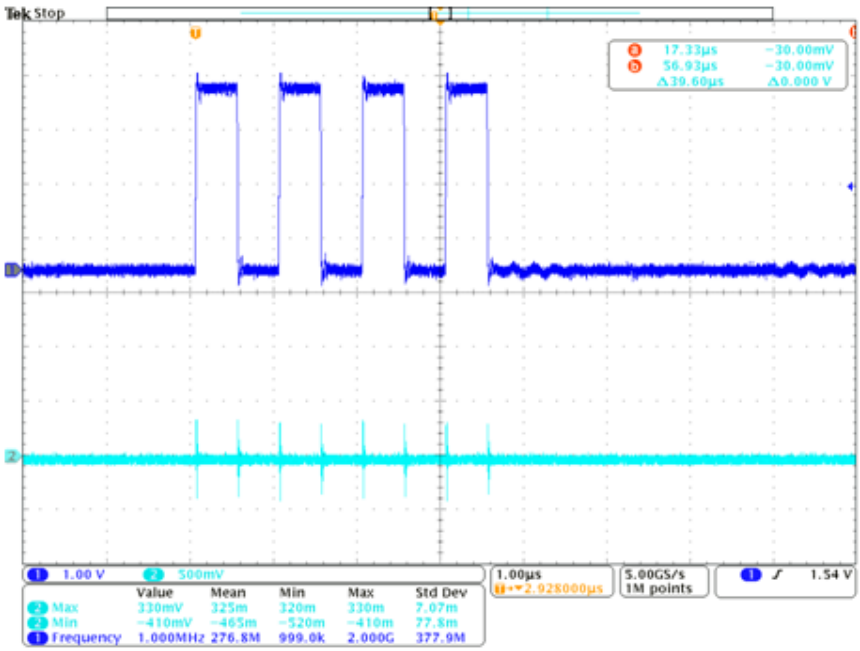
GROUND BOUNCE TEST:

Conditions: $\overline{OEB}$ = LOW (Enable), I/P corresponding to output under test = Low (0V), other inputs = Switching, O/P under test = through 500Ω resistor

i) Direction: A to B



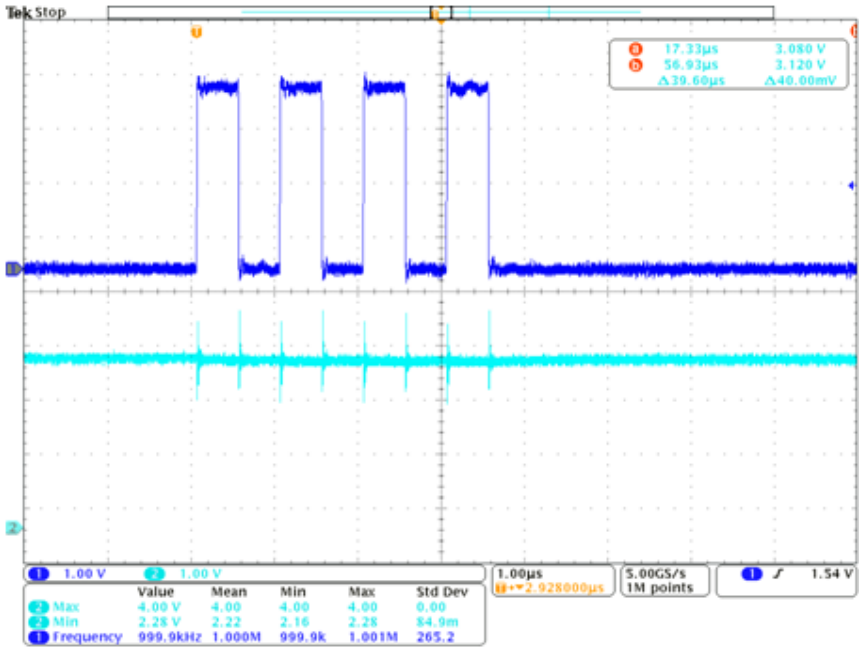
ii) Direction: B to A



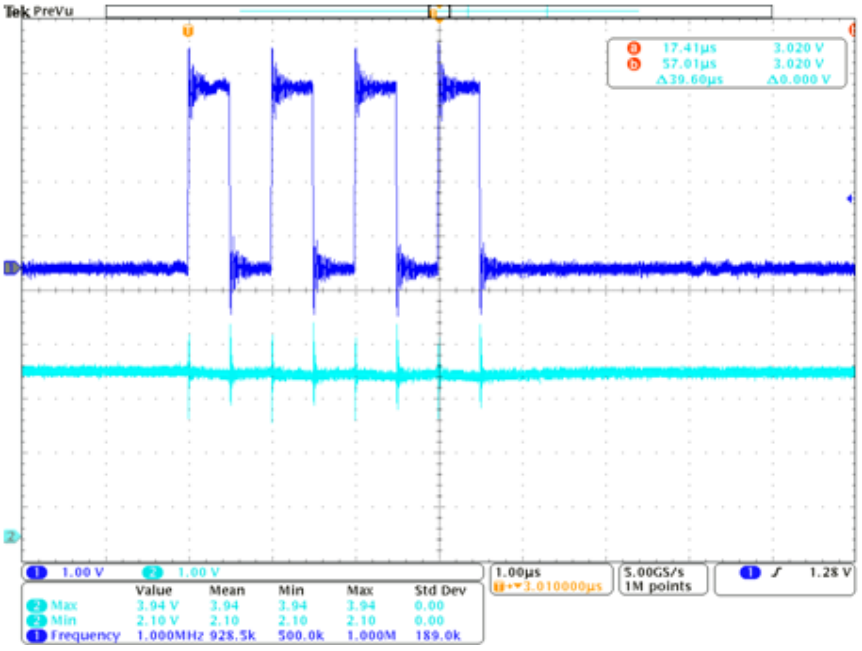
V_{DD} BOUNCE TEST:

Conditions: $\overline{OEB}$ = LOW (Enable), I/P corresponding to output under test = High (3.3V), other inputs = Switching, O/P under test = through 500Ω resistor

i) Direction: A to B



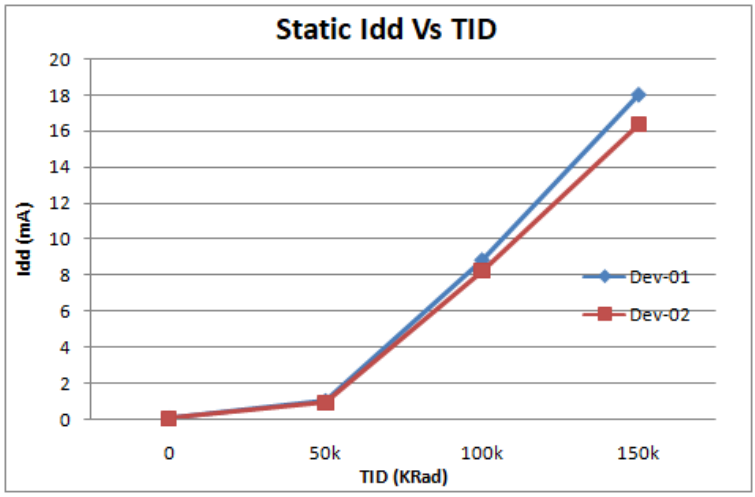
ii) Direction: B to A



RADIATION CHARACTERISTICS:

❖ Total Ionization Dose (TID) Testing

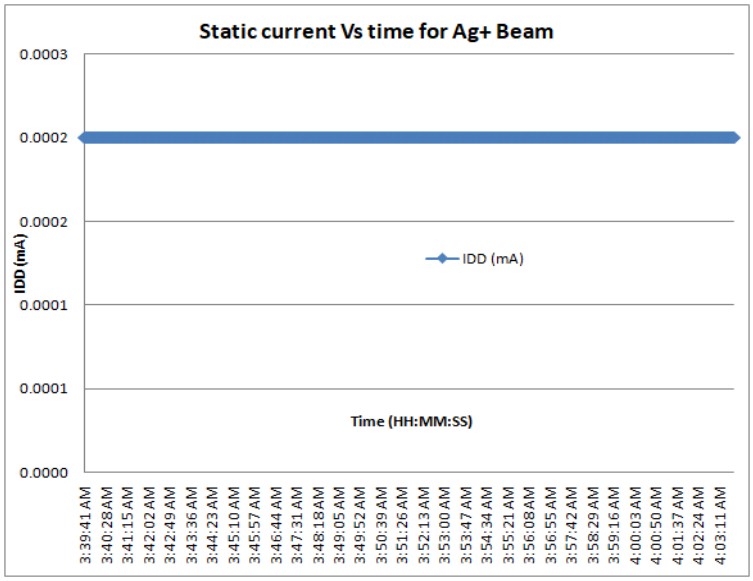
- TID testing of 16 Bit Transceiver (SC1124-0) is performed for radiation level up to 150 KRad.
- No functional degradation and no significant change in device parameters such as IIL, IIH, VOL & VOH was observed up to 100KRad.
- Static supply current increases with radiation dose, shown in figure below.



❖ Single Event Effect (SEE) Testing

SEE testing of 16 Bit Transceiver (SC1124-0) is performed at two different LET energy ion beams Ti+ (20 MeV-cm2/mg) and Ag+ (50 MeV-cm2/mg) for a Fluence of 10^6 ions/cm^2.

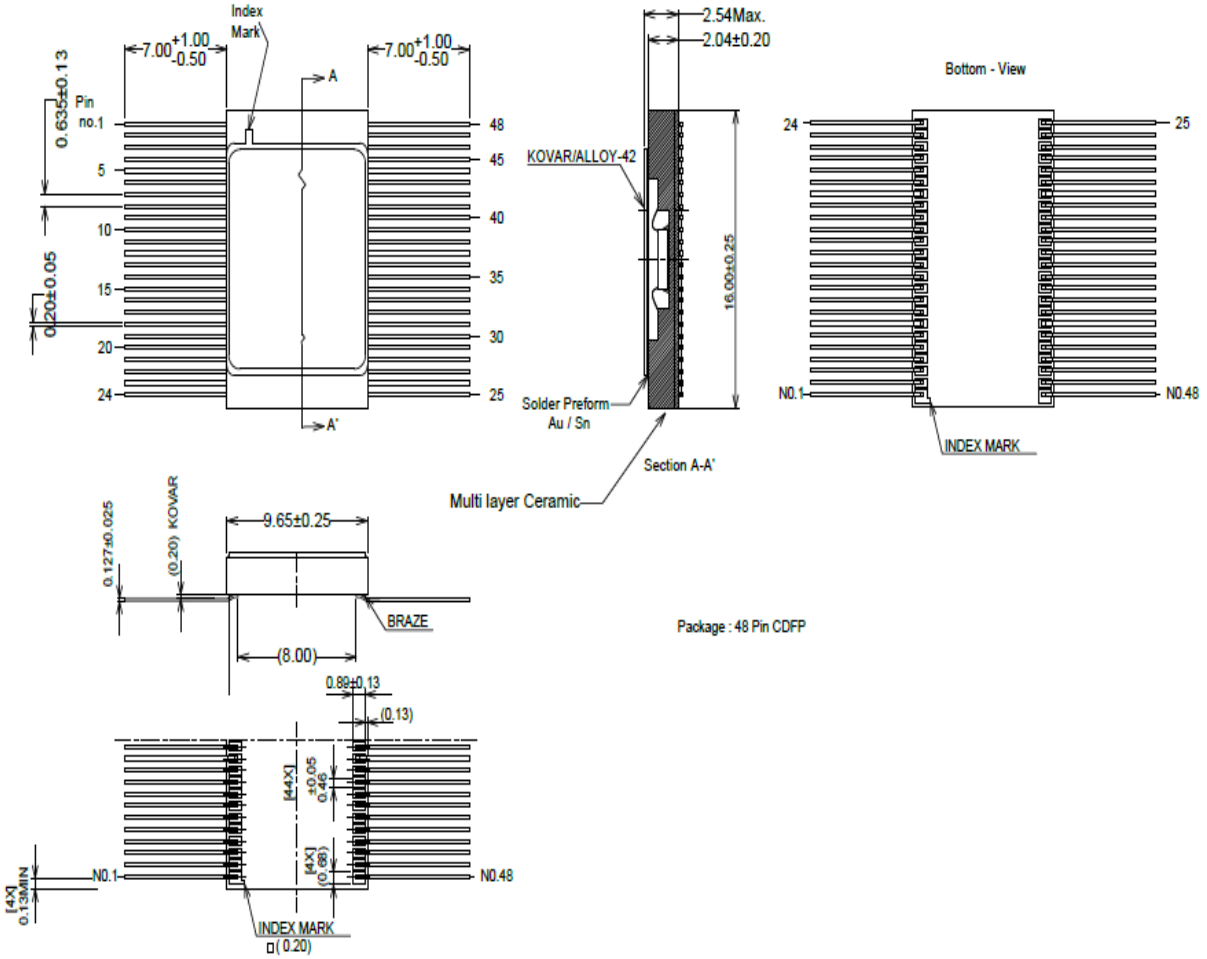
- No Single Event latch-up (SEL) was observed up to LET of 50 MeV-cm2/mg. Supply current (I_{DD}) remains within specification throughout testing.
- No Single Event transient (SET) was observed up to LET of 50 MeV-cm2/mg.



REVISION HISTORY

S. No.	Version	Date of release	Description
1	1.0	26th March 2019	New
2	1.1	December 2020	Revised

PACKAGE DRAWING (48 Pin Ceramic Dual Flat Pack):



NOTE: All linear dimensions are in inches (mm.)