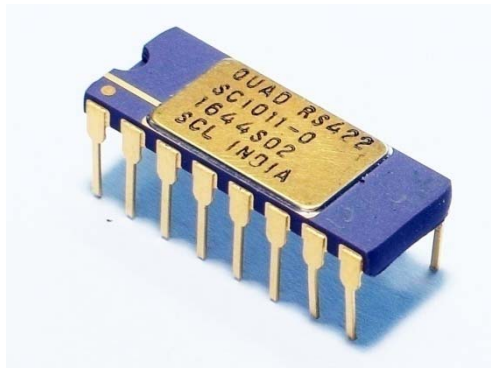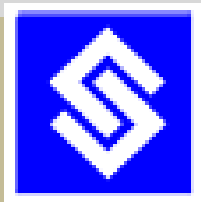**Quad RS-422**

SC1011-0

DATA SHEET

Feb 2022

Semi–Conductor Laboratory

Government of India

PRODUCT DESCRIPTION:

Quad RS-422 (SC1011-0) is a differential line driver. The enable function is common to all four drivers and offers a choice of active-high or active-low inputs. Each driver has a separate input and output pins for full-duplex bus communication designs. The device is designed for balanced bus transmission at switching rates up to 5 MHz

FEATURES:

- **Operates From Single 3.3V V_{CC}**
- **Switching Rates up to 5 MHz**
- **Transmission Rate to 10 Mbps**
- **Differential-State Outputs**
- **Designed for Multipoint Bus Transmission**
- **Common Mode Output Voltage Range: 0V to 3V**

DEVICE SUMMARY:

Reference	Package	Pins	Lead Finish
SC1011-0	DIP	16	Gold

Table 1: Device Summary

PIN CONFIGURATION:
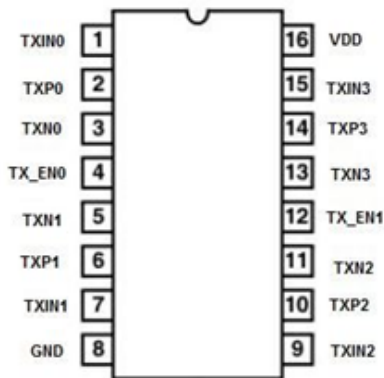
Figure-1: Device Pin Diagram

LOGIC DIAGRAM:
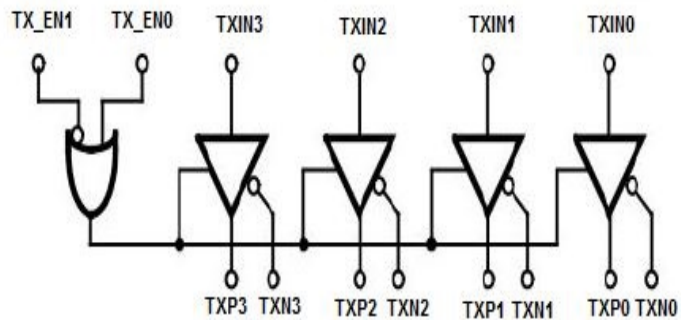
Figure-2: Device Logic Diagram

PIN DESCRIPTION:

SYMBOL	PIN	PIN DESCRIPTION
VDD	16	Supply Voltage (3.3V)
TXIN0, TXIN1, TXIN2, TXIN3	1,7,9,15	Inputs
TXP0, TXP1, TXP2, TXP3	2,6,10,14	Positive Outputs
TXN0, TXN1, TXN2, TXN3	3,5,11,13	Complementary Outputs
TX_EN0, TX_EN1	4,12	Enable Pins
GND	8	Ground (0V)

Table-2: Device Pin Description

FUNCTIONAL TABLE:

Device Power ON/OFF	INPUTS			OUTPUTS	
	Enable	Enable	IN	OUT	OUT
ON	L	H	X	HI-Z	HI-Z
ON	H	X	L	L	H
ON	X	L	L	L	H
ON	H	X	H	H	L
ON	X	L	H	H	L
OFF (0V)	X	X	X	HI-Z	HI-Z

Table 3: Truth Table

BASIC DC-PARAMETER TESTING & TEST CONDITIONS:

Test name	Test Parameter	Pins Tested	Force	Min	Typ.	Max	Unit
ESD Diode Test	Positive Diode	All Input / Output Pins	100uA	413.728		465.736	mV
	Negative Diode		-100uA	-521.587		-473.758	
Input Gate Leakage Test (VDD = 3.3V)	IIL	All Inputs	VIN = 0V	-56.2		52.2	nA
	IIH		VIN = 3.3V	-9.4		1.1	
Supply current	I_{DD}	All inputs Low	VDD = 3.3V VIL=0V	-	4.5	5.0	mA
		All Inputs High	VDD = 3.3V VIH=3.3V	-	4.0	5.0	

DRIVER ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Condition		Min	Typical	Max	Unit
|V$_{OD (SS)}$|	Steady-State differential output voltage	R$_L$ = 100 Ω Refer Figure10	Driver Input = 0V		-2.2449		V
			Driver Input = 3.3V		2.4419		
		V$_{CM}$ = 0V to 3V Refer Figure11	Driver Input = 0V		-2.4505		
			Driver Input = 3V		2.4460		
Δ|V$_{OD (SS)}$|	Change in magnitude of Steady-State differential output voltage between states	R$_L$ = 100 Ω Refer Figure10	Driver Input = 0V		0.01679		
			Driver Input = 3.3V		0.01374		
V$_{OD (RING)}$	Differential output voltage overshoot and undershoot	R$_L$ = 100 Ω C$_L$ = 50 pF Input PRR=500KHz, 50% Duty Cycle Refer Figure 13	Positive Overshoot		24.91		%
			Negative Overshoot		24.43		
V$_{OC (PP)}$	Peak-to-peak common-mode output voltage	Refer Figure 13			0.3		V
V$_{OC (SS)}$	Steady-state common-mode output voltage	Refer Figure 13		1.5		1.8	V
ΔV$_{OC (SS)}$	Change in Steady-state common-mode output voltage	Refer Figure 13			-		
V$_{OH}$	Output Voltage High	R$_L$ = 100 Ω	Driver Input = 0V		0.6984		V
			Driver Input = 3.3V		3.14057		
V$_{OL}$	Output Voltage Low	R$_L$ = 100 Ω	Driver Input = 0V		3.12683		
			Driver Input = 3.3V		0.681609		
I$_{DD}$ (D)	Dynamic Current Supply Test	V$_{DD}$ = 3.3V Input Pulse Rate = 5 MHz			4		mA
I$_{Z(Z)}$ or I$_{Y(Z)}$	High-impedance state output current	TX_EN0 = 0, TX_EN1 = 1 Driver Input = 0/1			650	750	μA
I$_{Z(S)}$ or I$_{Y(S)}$	Short-circuit output current	Driver Input = 0	TXP		-172		mA
			TXN		155		
		Driver Input = 1	TXP		3.18		
			TXN		168		

DRIVER SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Condition	Min	Typical	Max	Unit
t$_{PLH}$	Propagation delay time, low-to-high-level output	R$_L$ = 100 Ω C$_L$ = 50 pF		24		ns
t$_{PHL}$	Propagation delay time, high-to-low-level output			22		
t$_r$	Differential output signal rise time			9		
t$_f$	Differential output signal fall time			10		
T$_{sk(p)}$	Pulse skew (|t$_{PHL}$-t$_{PLH}$|)			2		

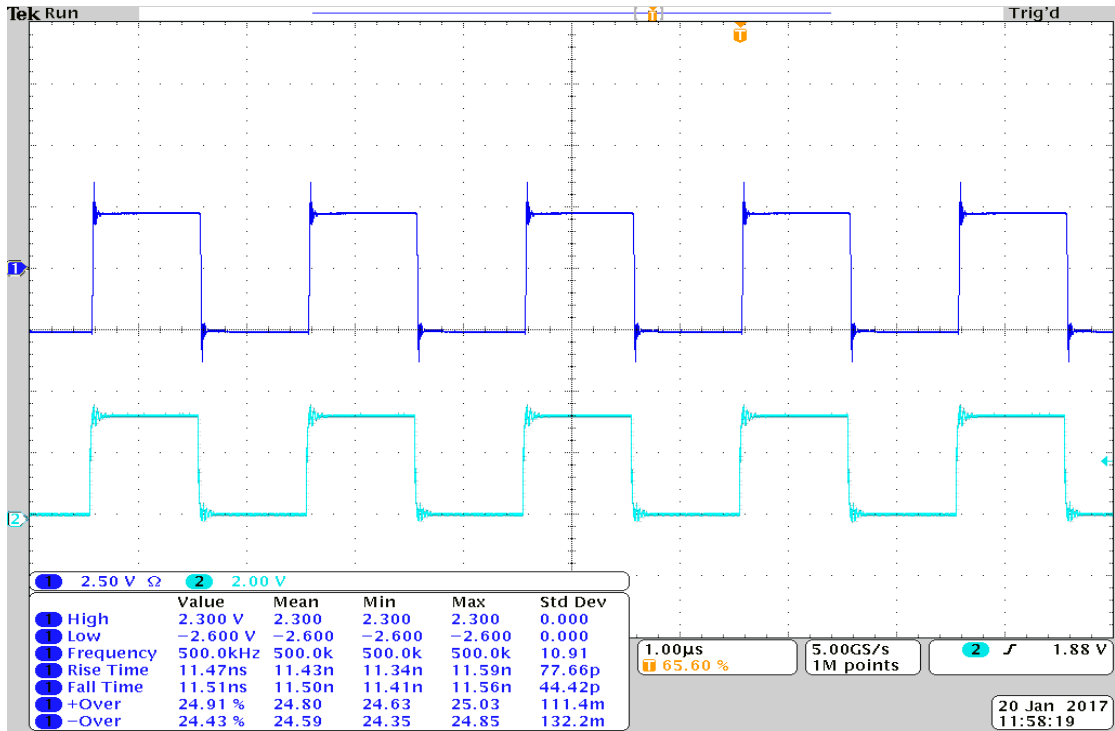**TYPICAL CHARACTERISTICS:**

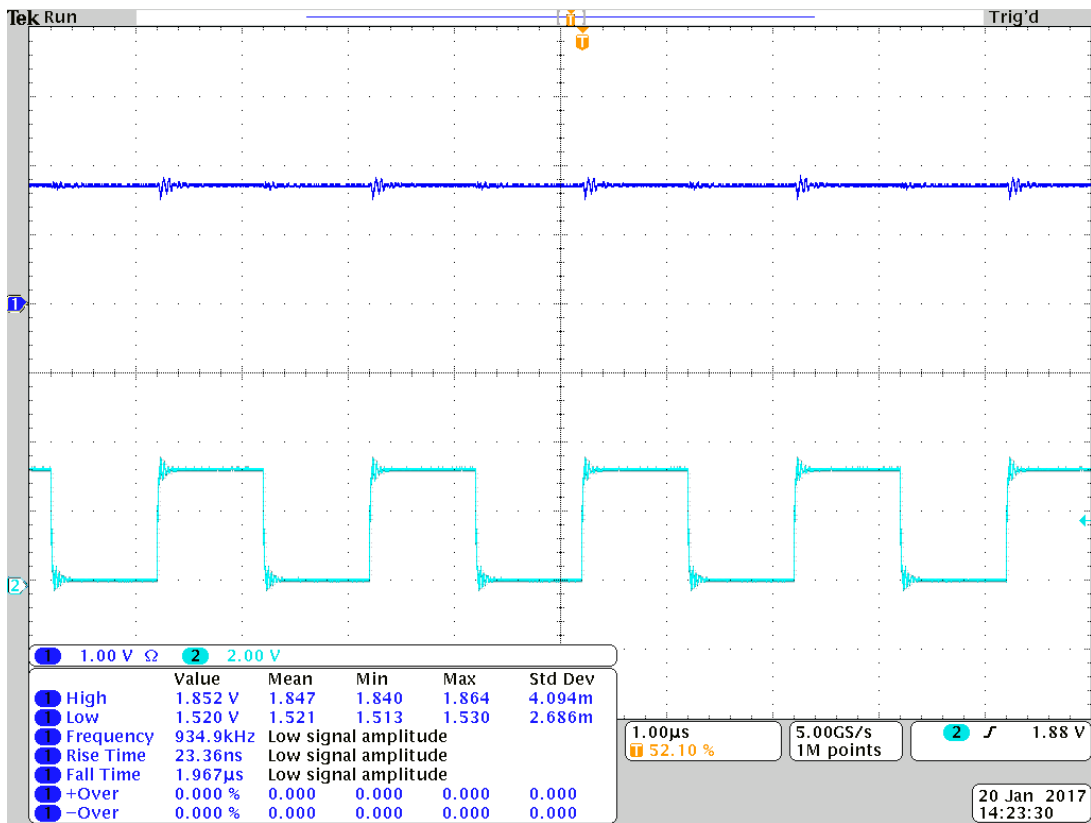**Figure3**: The Driver Output Overshoots

Figure4: The Driver Common-Mode Output Voltage
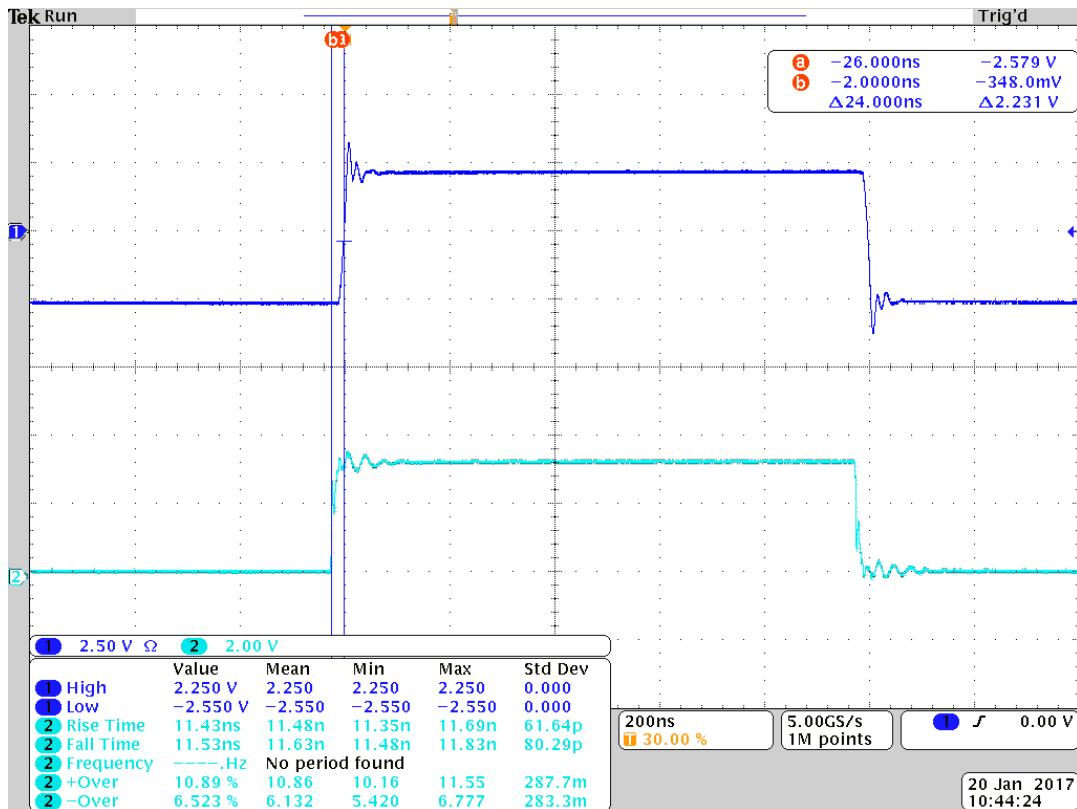
Figure5: Propagation Delay Time, Low-to-High-Level Output
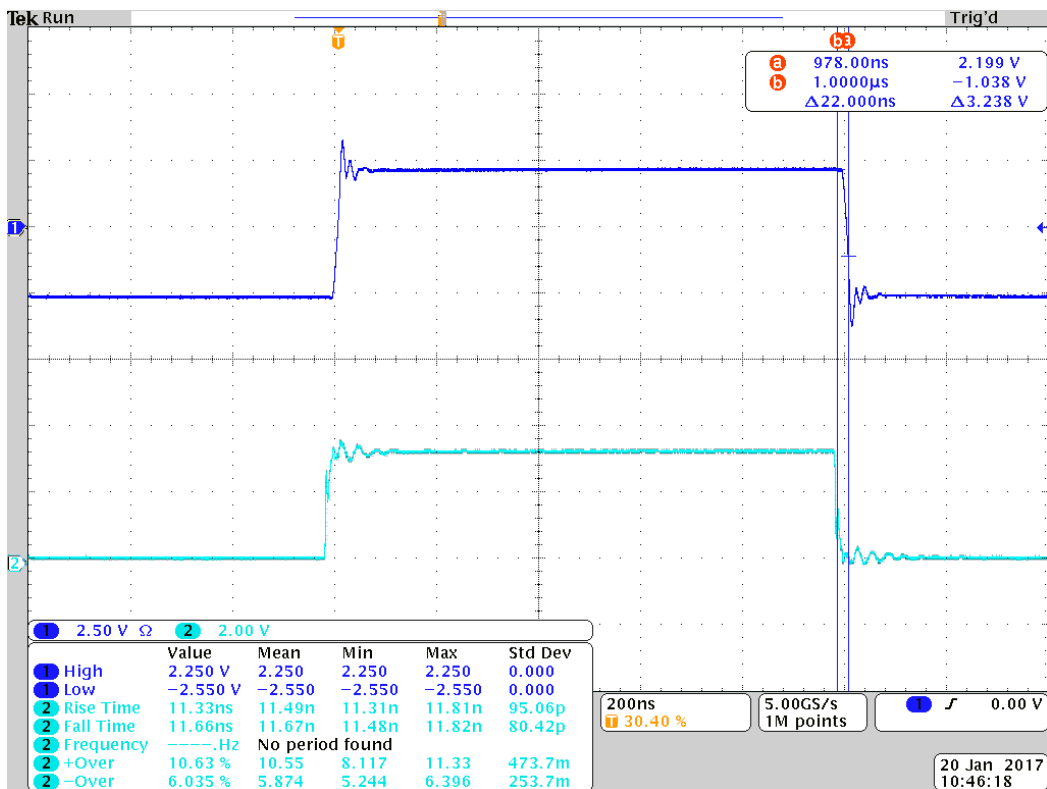

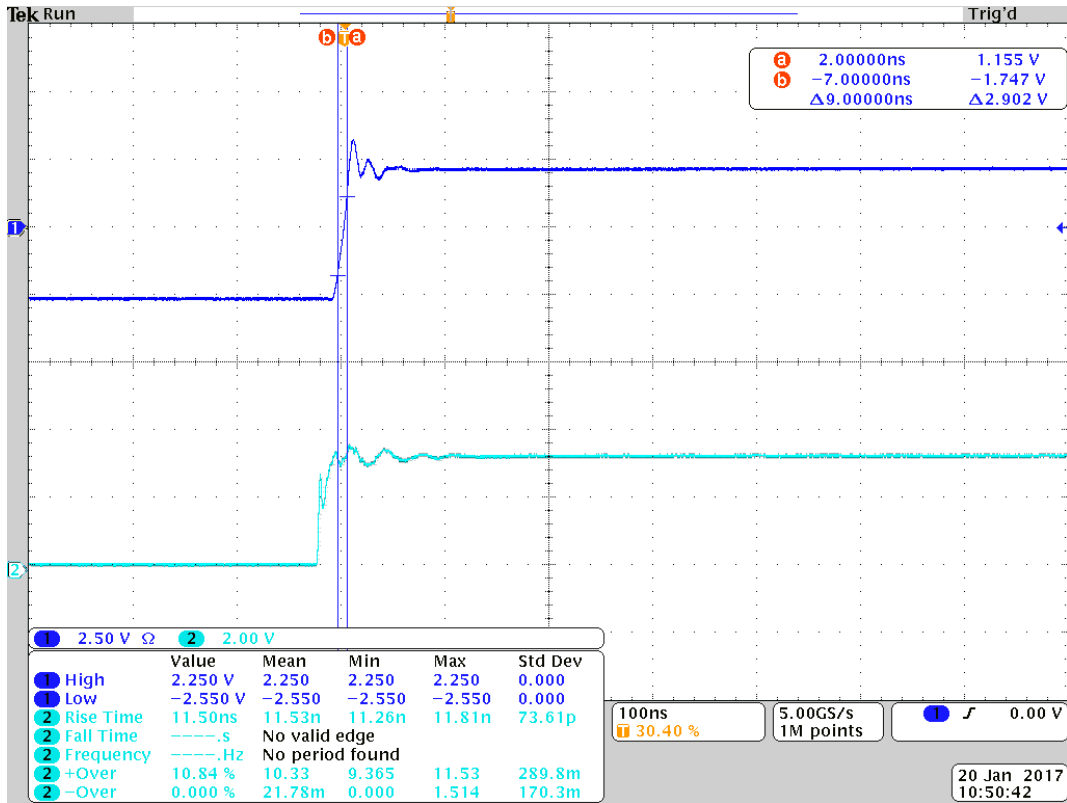
Figure6: Propagation delay time, high-to-low-level output
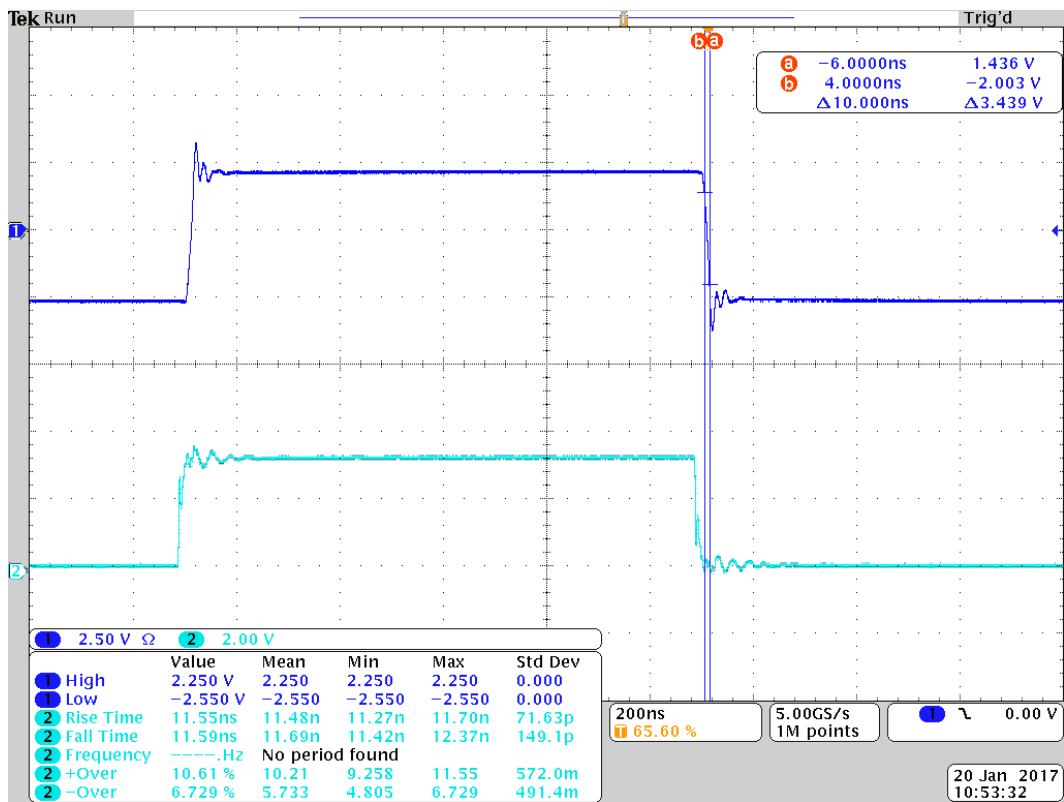
Figure7: Differential output signal rise time

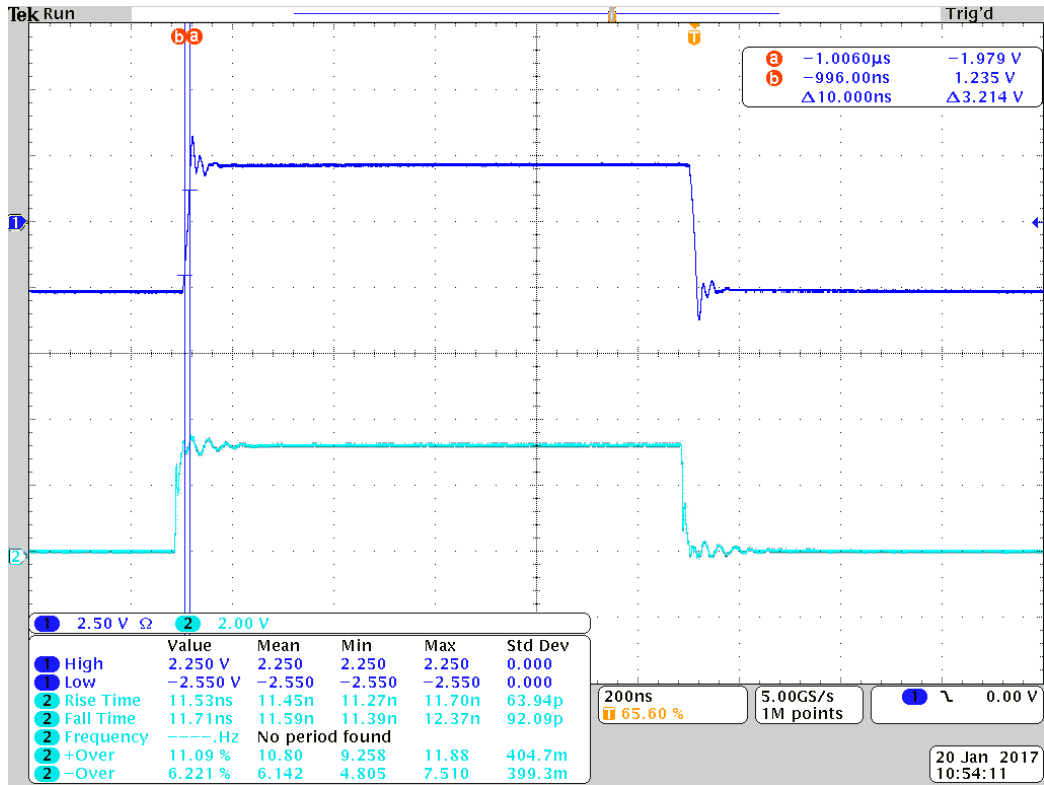**Figure8:** Differential output signal fall time

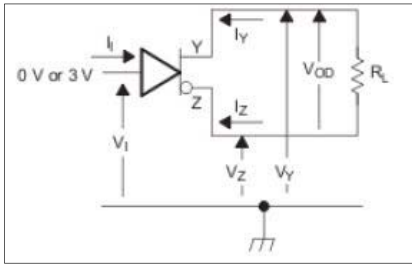**Figure9:** Pulse Skew ($|t_{PHL}-t_{PLH}|$)

TEST CIRCUIT AND SWITCHING WAVEFORMS:
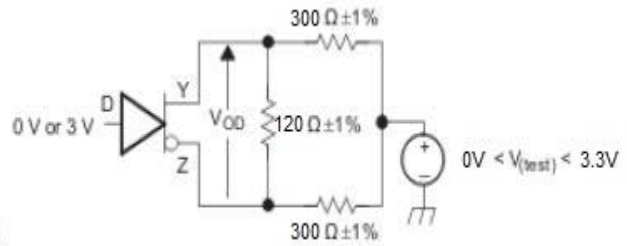

Figure10: Driver V$_{OD}$, Voltage, Current

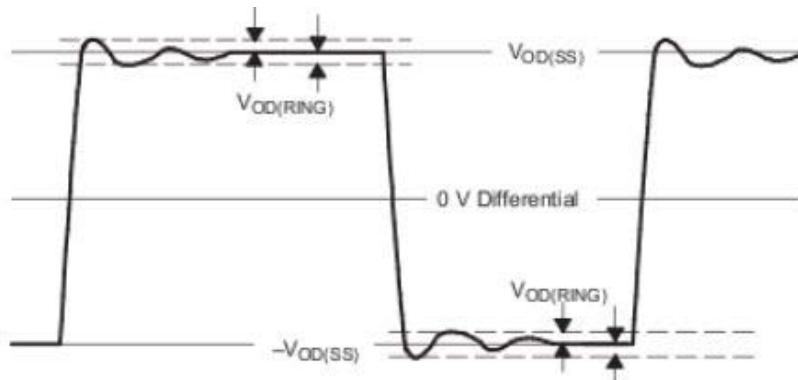**Figure11:** Driver V$_{OD}$ Common Mode Loading

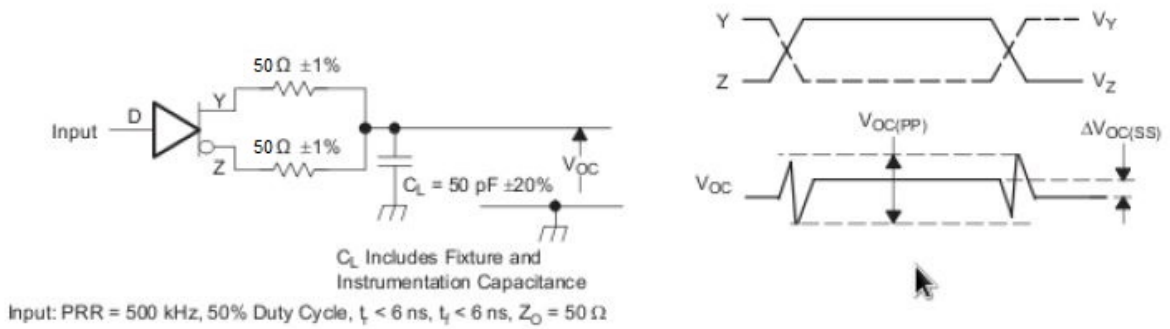**Figure12:** Driver V$_{OD\ (RING)}$ Waveform and Definitions

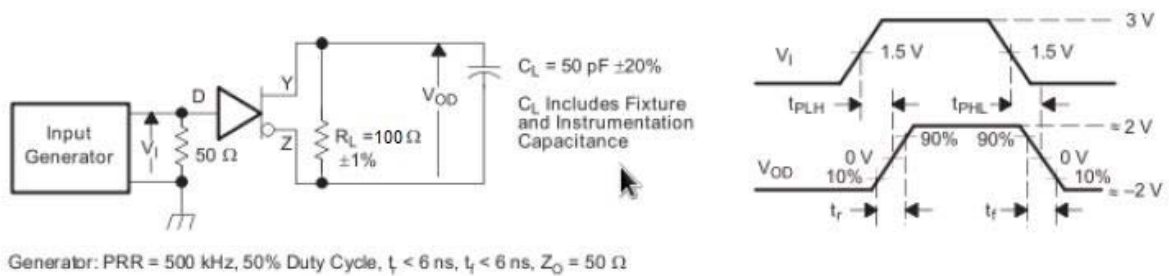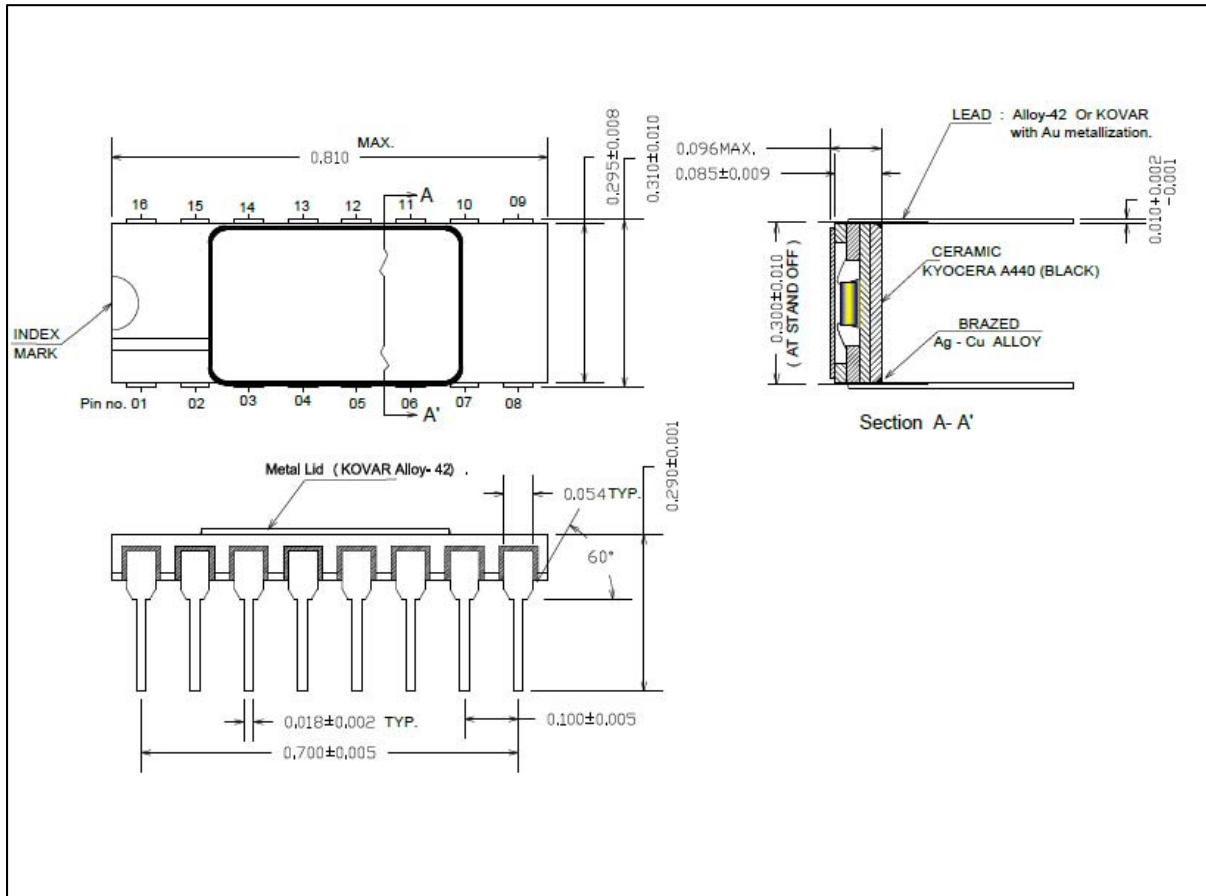**Figure13:** Driver Common-Mode Output Voltage

Figure14: Driver Switching and Voltage Waveforms

PACKAGE INFORMATION:

16 PIN CDIP

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