16-BIT BUFFER 3-STATE OUTPUT (COLD SPARING, HOT INSERTION & 5V TOLERANT INPUT) (SC1004-2) (Radiation Tolerant)

DATA SHEET

Version 1.1, May'2020

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PRODUCT DESCRIPTION:

SC1004-2 16-bit buffer and line driver is designed for low-voltage (V_{DD} =3.3V) operation, These devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. These devices provide true outputs and symmetrical active-low output-enable ($\overline{OE}$) inputs.

The outputs, which are designed to source or sink up to 7mA, include equivalent small series resistors to reduce overshoot and undershoot.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pull down resistors with the bus-hold circuitry is not recommended.

When V_{DD} is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down.

However, to ensure the high-impedance state above 1.5 V $\overline{OE}$ should be tied to V_{DD} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for hot-insertion applications using I_{OFF} and power-up 3-state. The I_{OFF} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

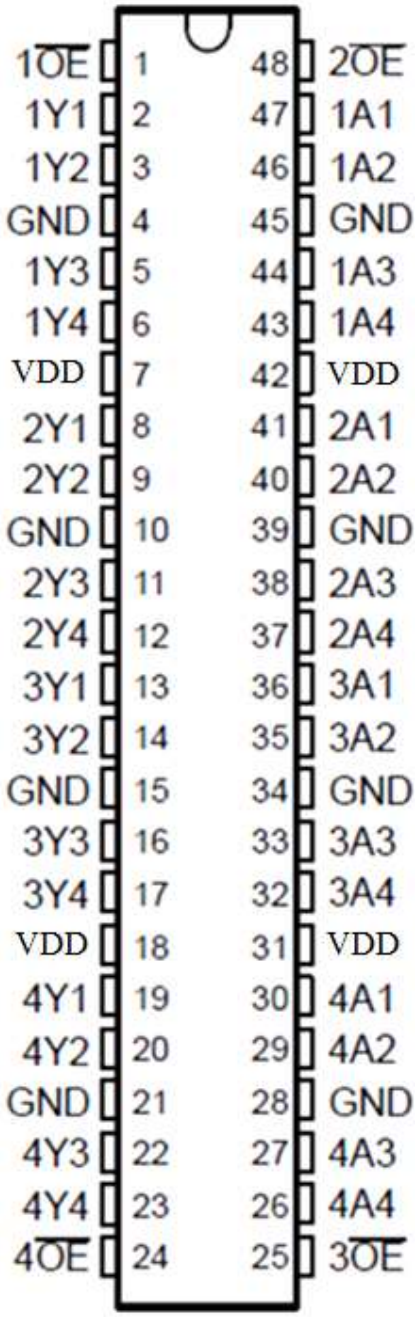
FEATURES:

- **Operating Power Supply 3.3V ±0.3V**
- **Cold sparing feature at I/O**
- **Output Ports Have Equivalent 22-W Series Resistors, so No External Resistors are required.**
- **5V tolerant inputs for interfacing 5V logic with 3.3V V_{DD}**
- **I_{OFF} and power-up 3-state support hot Insertion**
- **Bus Hold on data inputs eliminates the need for external pull-up / pull-down resistors**
- **Distributed V_{DD} and GND pins minimize high-speed switching noise**
- **Flow-through architecture optimizes PCB layout**
- **6.5 ns typical propagation delay**
- **Low power dissipation (<2mW at 3.6V static)**
- **Operating Temperature: -55ºC to 125ºC.**
- **Radiation Tolerant up to 100 KRad**
- **SET/SEL immune up to 50 MeV.cm²/mg**
- **48 Pin CDFP /Customized package /Die**
- **Pin compatible with LVTH162244.**
- **Package Θ_{JC} = 2.7ºC/Watt**
- **ESD Sensitivity Level: HBM Class 1B (500V to 999V), passed up to 750V**
- **SCL's 180nm CMOS Technology**

PIN CONFIGURATION:

Pin no.	Signal	Pin no.	Signal
1	$\overline{1OE}$	**25**	$\overline{3OE}$
2	1Y1	**26**	4A4
3	1Y2	**27**	4A3
4	GND	**28**	GND
5	1Y3	**29**	4A2
6	1Y4	**30**	4A1
7	V_{DD}	**31**	V_{DD}
8	2Y1	**32**	3A4
9	2Y2	**33**	3A3
10	GND	**34**	GND
11	2Y3	**35**	3A2
12	2Y4	**36**	3A1
13	3Y1	**37**	2A4
14	3Y2	**38**	2A3
15	GND	**39**	GND
16	3Y3	**40**	2A2
17	3Y4	**41**	2A1
18	V_{DD}	**42**	V_{DD}
19	4Y1	**43**	1A4
20	4Y2	**44**	1A3
21	GND2	**45**	GND
22	4Y3	**46**	1A2
23	4Y4	**47**	1A1
24	$\overline{4OE}$	**48**	$\overline{2OE}$

Package Pin Details



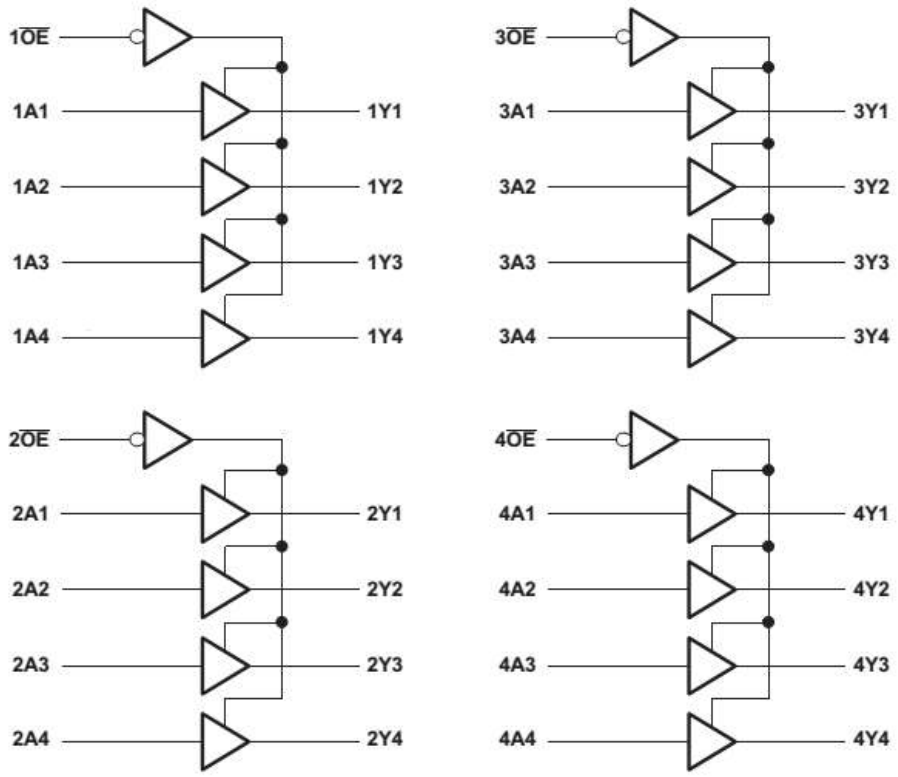
Device Package View

FUNCTIONAL TABLE (EACH 4-BIT BUFFER):

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

Truth table

LOGIC DIAGRAM (POSITIVE LOGIC):



Device Logic Diagram

ABSOLUTE MAXIMUM RATINGS (1):

Over operating free-air temperature range (unless otherwise noted),

PARAMETER	UNIT
Supply Voltage Range (V_{DD})	–0.5 V to 4.3V
Input Voltage Range (V_{IN})	–0.5 V to 6.5V
Output Voltage Range In High Impedance or Power Off (V_{OUT})	–0.5 V to 4.3V
Output Voltage Range Applied In High State (V_{OUT})	–0.5 V to V_{DD} + 0.5 V
Max. Junction Temperature (T_J)	150°C
Storage Temperature Range (T_{STG})	–65°C to 150°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS:

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	3.0	3.3	3.6	V
V_{IH}	High Level Input Voltage	2.0	-	5.5	V
V_{IL}	Low Level Input Voltage	0	-	0.8	V
I_{OH}	High-level output current	-	-	-10	mA
I_{OL}	Low-level output current	-	-	7	mA
$\Delta t/\Delta V_{DD}$	Power Up Ramp Rate	200	-	-	usec/V
T_A	Operating Free Air Temperature	-55	-	+125	ºC

DC ELECTRICAL SPECIFICATIONS:

Test condition: V_{DD}=3.3 ± 0.3V, V_{SS} = 0V, T_A = -55°C to +125°C

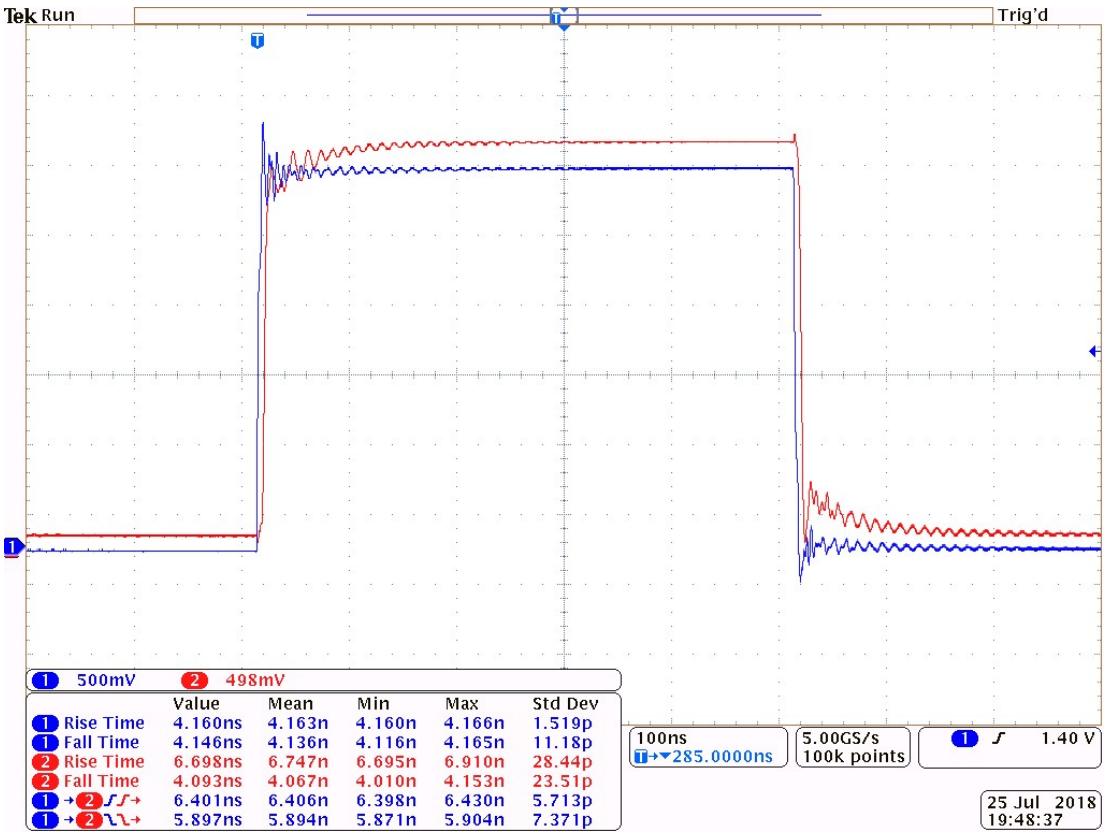
Symbol	Parameter	Test Conditions	Test Results			Units
			Min.	Typ.	Max.	
I_I	Control Inputs Leakage Current V_{DD} = 3.6V	I_{IL} (V_{IN} = V_{SS}) I_{IH} (V_{IN} = V_{DD})	-	-	±1	µA
		I_{IH} (V_{IN} = 5.5V)	-	-	±10	µA
	Data Inputs Leakage Current V_{DD} = 3.6V	I_{IL} (V_{IN} = V_{SS}) I_{IH} (V_{IN} = V_{DD})	-	-	±1	µA
		I_{IH} (V_I = 5.5V)	-	-	±10	µA
I_I (Hold)	Data Inputs Hold Current V_{DD} = 3.0V	V_{IN} = 0.8V (sink)	75	31	-	µA
		V_{IN} = 1.5V	-75	-17.4	-	µA
		V_I = 2.0V (Source)	-75	-0.5	-	µA
V_{OH}	High Level Output Voltage V_{DD} = 3.0V, V_{IH} = 2.0V	I_{OH} = -20uA	2.9	2.96	V_{DD}	V
		I_{OH} = -4mA	2.0	2.63		
		I_{OH} = -8mA		2.51		
		I_{OH} = -10mA		2.26		
V_{OL}	Low Level Output Voltage V_{DD} = 3.0V, V_{IL} = 0.8V	I_{OL} = 20uA	V_{SS}	0.01	0.1	V
		I_{OL} = 4mA		0.27	0.8	
		I_{OL} = 7mA		0.51		
I_{OZH}	High Impedance Output Current With Output High	V_{DD} = 3.6V, V_{OUT} = 3.0V	-	-	5.0	µA
I_{OZL}	High Impedance Output Current With Output Low	V_{DD} = 3.6V, V_{OUT} = 0.5V	-	-	-5.0	µA
I_{OFF}	Power Off Input Leakage Current	V_{DD} = 0V, $\overline{2OE}$= 0 V_I = 0V or 5.5V	-	-	±1	µA
	Power Off Output Leakage Current	V_{DD} = 0V, $\overline{2OE}$= 0 V_O = 0V or 3.6V	-	-	±1	µA
I_{DD}	Static Supply Current V_{DD} = 3.6V V_I = V_{SS} or V_{DD}	All Outputs Low/High	-	0.1	0.2	mA
		All Outputs Disabled	-	0.1	0.2	mA
ΔI_{DD}	Increase in supply current with V_{DD} change for given input condition	V_{DD} = 3 V to 3.6 V One input at V_{DD} – 0.6 V, Other input at V_{DD} or 0V	-	0.02	0.2	mA
Basic Functional Test V_{DD} = 3.3 ± 0.3V		V_{IL}=0.8V, V_{IH}=2.0V V_{OL} ≤0.4V, V_{OH} ≥2.4V	-	-	1	MHz
Functional Test 5V Tolerant V_{DD} = 3.0V		V_{IL}=0V, V_{IH}=5.5V V_{OL} ≤0.4V, V_{OH} ≥2.4V	-	-	1	MHz

AC ELECTRICAL SPECIFICATIONS:

Test condition: (Propagation Delay)

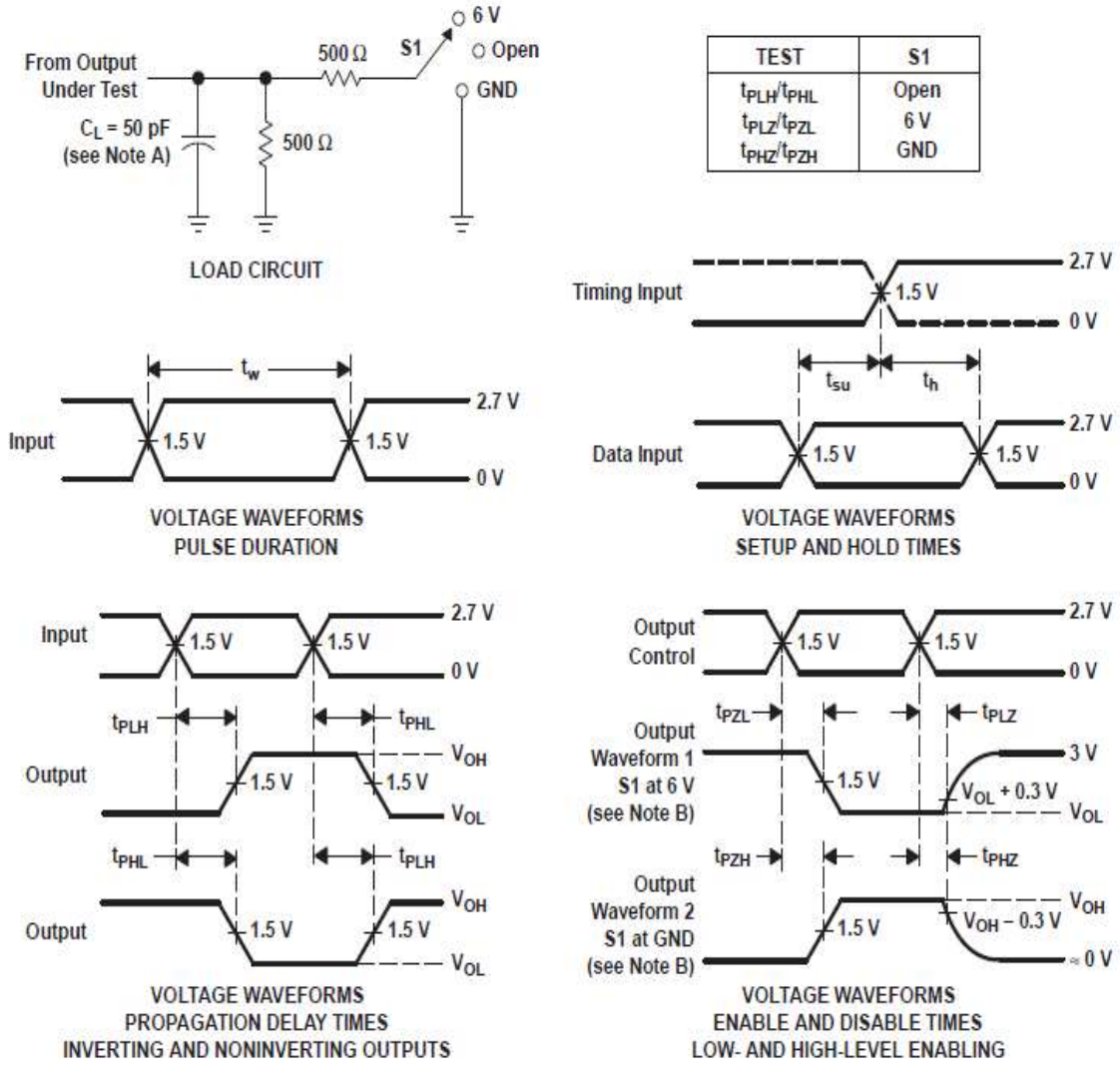
V_{DD}=3.3V, V_{IN} = 0V or 3.3V @1 MHz, C_L = 50pF, T_A = -55ºC to 125ºC,

Parameter	From	To	Test Results			Units
			Min.	Typ.	Max.	
t_{PLH}	A	Y	1	6.5	15	ns
t_{PHL}			1	6.1	15	ns
t_{PZH}	$\overline{OE}$	Y	-	11.6	-	ns
t_{PZL}			-	8.4	-	ns
t_{PHZ}	$\overline{OE}$	Y	-	10	-	ns
t_{PLZ}			-	7.8	-	ns



Delay (A to Y) t_{PHL}, t_{PLH}

TEST CIRCUIT AND SWITCHING WAVEFORM:



AC parameter measurement information

NOTES:
A: CL includes probe and jig capacitance
B: Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

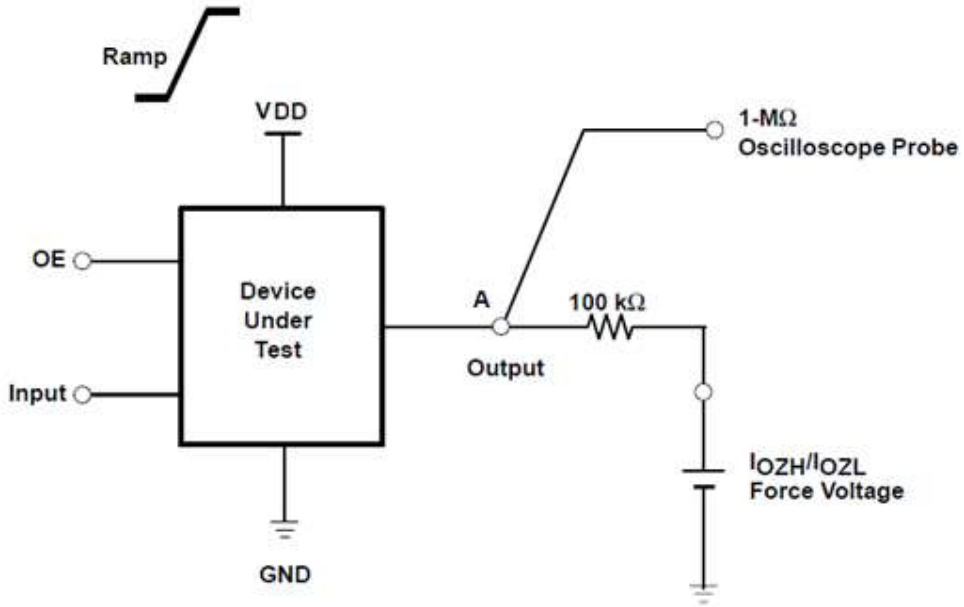
COLD SPARING (I_{OFF}) TEST:

In cold sparing I/O when V_{DD} is down to zero volts, I/Os will go in the high-impedance state so that damage to the device does not occur.
I_{OFF} protection circuitry ensures that no excessive current is drawn from or to an input, output, or combined I/O that is biased to a specified voltage while the device is powered down. This condition can occur when subsections of a system are powered down (partial power down) to reduce energy consumption. All standard logic devices with the Ioff specification allow only 100 uA of maximum current. Any current in excess of this amount (for example, a forward-biased p-n junction) is not considered normal leakage current.

PU3S (Power Up Tri State) HOT INSERTION TEST:

Testing of power-up three-state (PU3S) circuits was done at nominal temperature and voltage.
All devices tested have a nominal V_{DD} of 3.3 V.

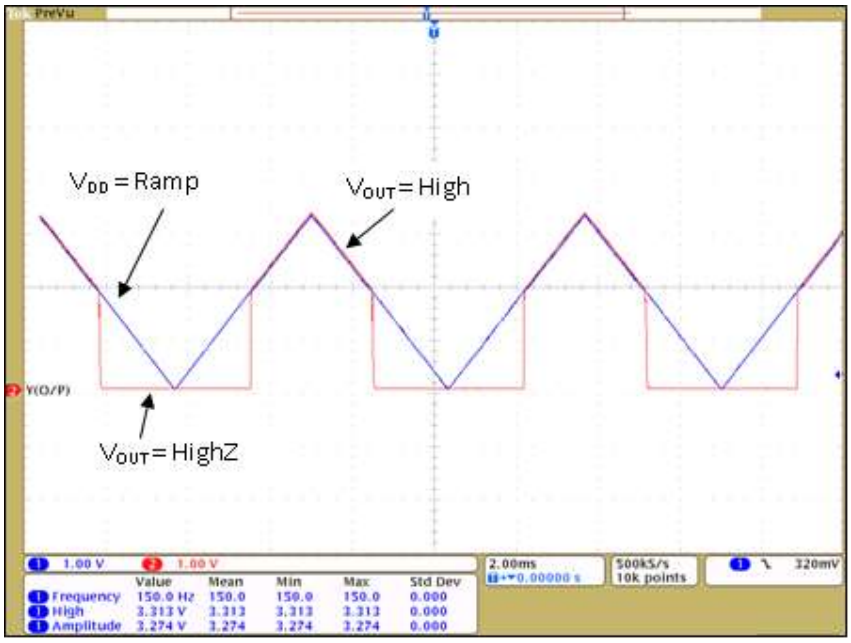
The test setup is shown in Figure 1. The V_{DD} was ramped at ramp rate (> 200usec / V) to determine the effect of the V_{DD} ramp rate on the device output or I/O structure. I_O was not measured directly; instead the voltage was measured at the output or I/O terminal with a 1-MΩ oscilloscope probe.



Test circuit (PU3S)

CASE1:

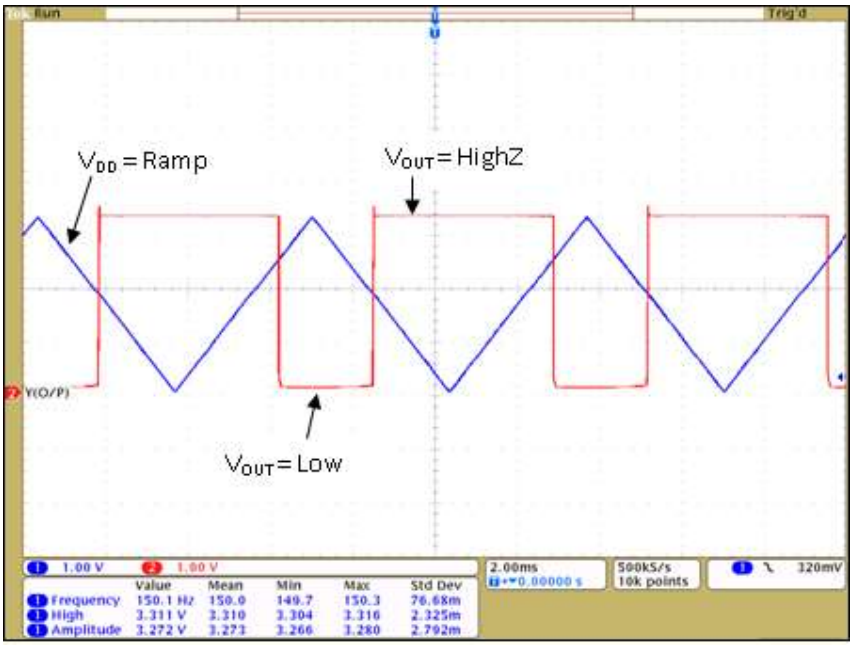
$\overline{OE}$ = LOW (Enable), Input = High (3.3V), Output = V_{SS} through 500ohm resistor



V_{OZL} at supply V_{CC} (ramp rate: 1msec/V), O/P is in HighZ with V_{CC} <1.5V

CASE2:

$\overline{OE}$ = LOW (Enable), Input = Low (0V), Output = 3.3V through 500ohm resistor



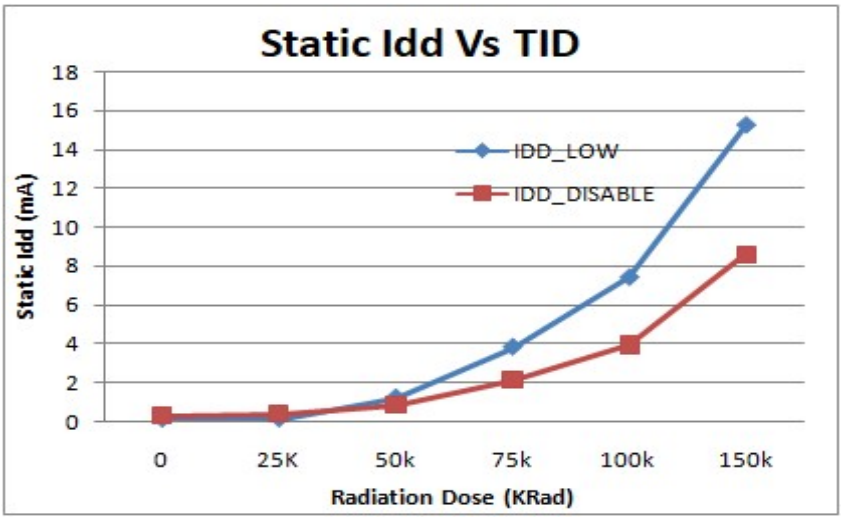
V_{OZH} at supply V_{DD} (ramp rate: 1msec/V), O/P is in HighZ with V_{DD} <1.5V

RADIATION CHARACTERISTICS:

❖ **Total Ionization Dose (TID) Testing**

TID testing of 16 Bit Buffer (SC1004-2) is performed for radiation level up to 150KRad.

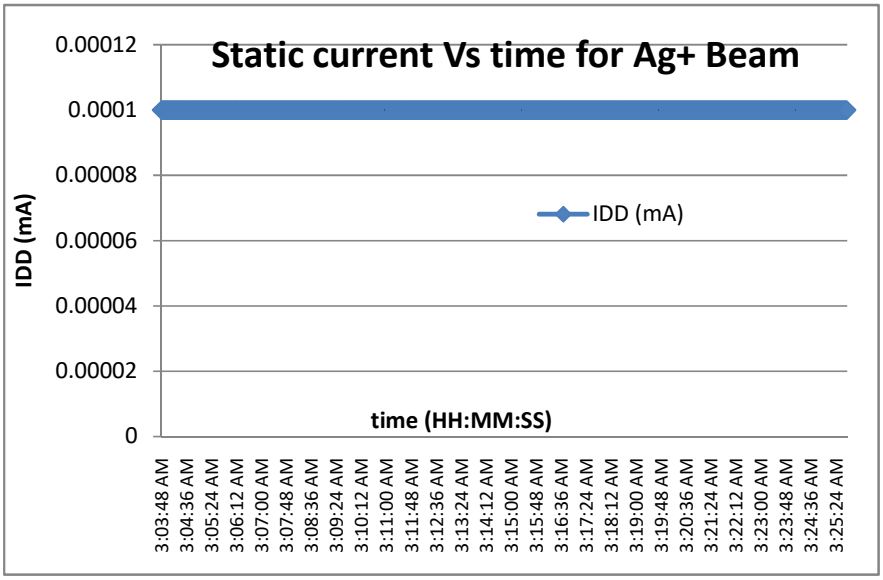
- No functional degradation and no significant change in device parameters such as IIL, IIH, VOL & VOH was observed up to 100KRad.
- Static supply current increases with radiation dose, shown in figure below.



❖ **Single Event Effect (SEE) Testing**

SEE testing of 16 Bit Buffer (SC1004-2) is performed at three different LET energy ion beams Ti+ (21 MeV-cm2/mg), Ni+ (30 MeV-cm2/mg) and Ag+ (50 MeV-cm2/mg) for a Fluence of 10^6 ions/cm^2.

- No Single Event latch-up (SEL) was observed up to LET of 50 MeV-cm2/mg. Supply current (I_{DD}) remains within specification throughout testing.
- No Single Event transient (SET) was observed up to LET of 50 MeV-cm2/mg.

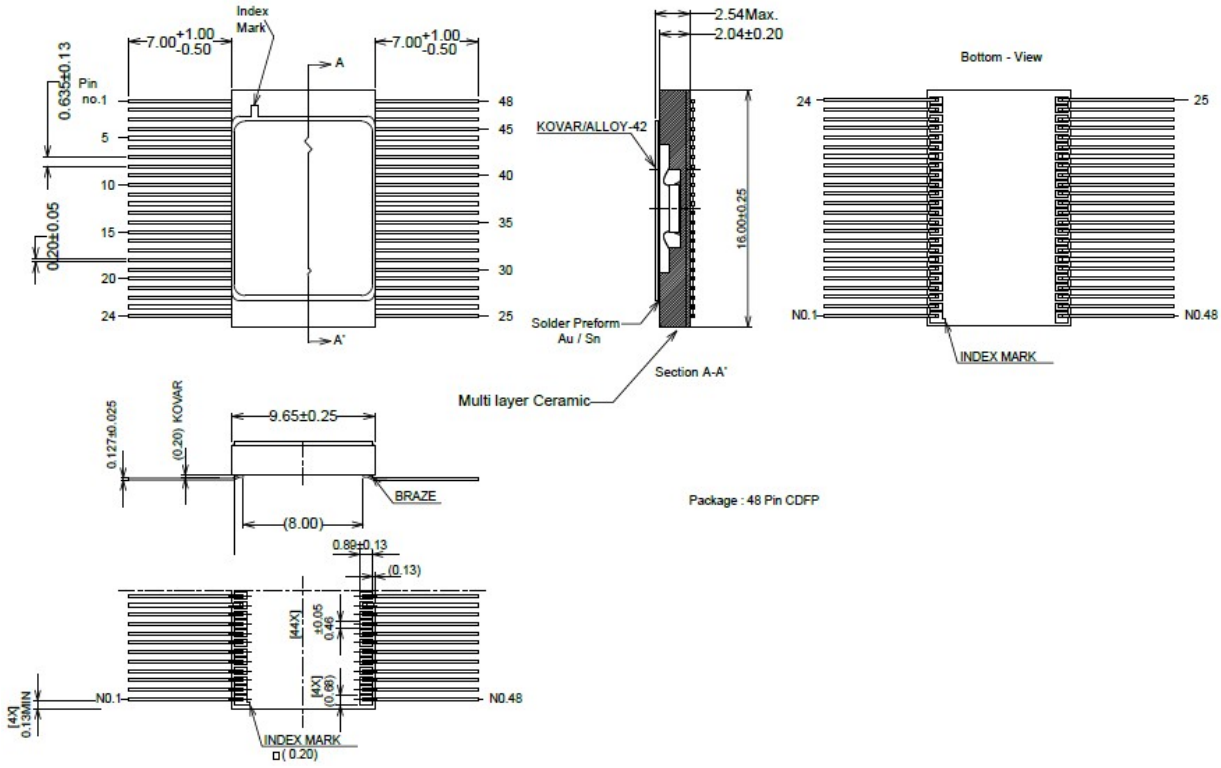


REVISION HISTORY

S. No.	Version	Date of release	Description
1	1.0	August' 2019	New
2	1.1	May' 2020	Revised

PACKAGE DRAWING (48 Pin Ceramic Dual Flat Pack):

NOTE: All linear dimensions are in inches (mm.)



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