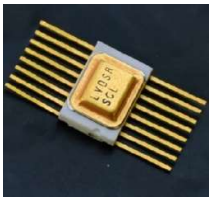
HIGH SPEED

QUAD LVDS RECEIVER

(SC1003-1)

(Radiation Tolerant)



DATA SHEET

Version 1.0, March 2019

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PRODUCT DESCRIPTION:

The SC1003-1 is a quad, low-voltage, differential signaling (QLVDS) line receiver specifically designed and packaged for use in aerospace environments in a low-power and fast point-to-point baseband data transmission standard.

Any of the four differential receivers provides a valid logical output state with a ±100mV differential input voltage within the input common-mode voltage range.

The circuit features an internal fail safe function to ensure a known output state in case of an input short circuit or floating.

The intended application of these devices and signaling technique is point-to-point data transmission over controlled impedance media of approximately 100 ohm. The transmission media may be printed-circuit board traces, backplanes or cables.

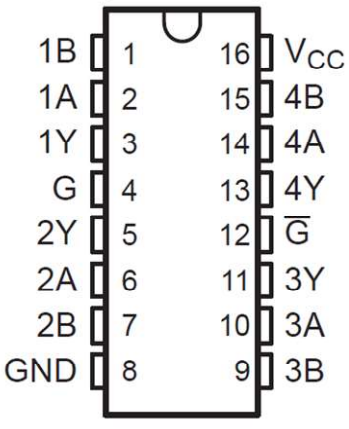
FEATURES:

- **Operating Power Supply 3.3V ±0.3V**
- **Cold Sparing at LVDS input pins**
- **LVDS input levels and CMOS logic output levels**
- **Compatible with ANSI/TIA/EIA-644 LVDS standard**
- **400 Mbps (200 MHz) switching rates**
- **Differential input thresholds ± 100mV**
- **Open circuit fail safe function**
- **Power dissipation 76 mW Typical per receiver at 200MHz (V_{DD}=3.3V)**
- **Propagation delay ≤ 5 nsec.**
- **Operating Temperature Range: -55ºC to 125ºC**
- **16 Pin CSOP /Customized package /Die**
- **Radiation Tolerant up to 200 KRad**
- **SET/SEL immune up to 50 MeV.cm²/mg**
- **Pin compatible with QLVDS receiver LVDS32**
- **ESD protection level: HBM class-1 (< 1999V)**
- **Latch up current protection ±100mA**
- **Θ_{JC} = 3.1ºC/Watt**
- **SCL's 180nm CMOS Technology**

PIN CONFIGURATION:

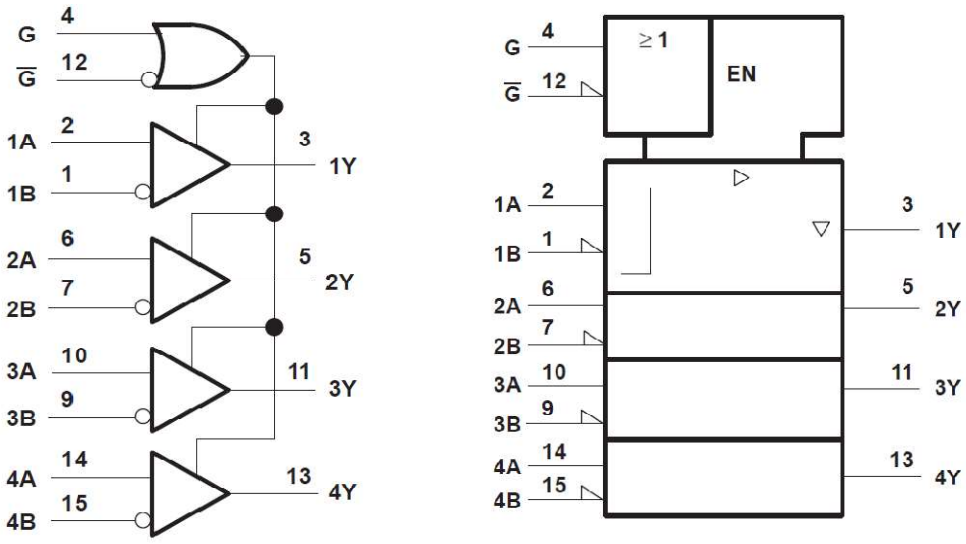
Pin No.	Pin Name	Description
16	V_{DD}	+3.3V Supply
8	GND	Supply Ground
4,12	G / $\bar{G}$	Control inputs
1,7,9,15	(1,2,3,4) B	receiver input pin (Inverting)
2,6,10,14	(1,2,3,4) A	receiver input pin (Non-inverting)
3,5,11,13	(1,2,3,4) Y	Driver o/p pin, TTL/CMOS compatible

Device Pin Description



Device Pin Diagram

FUNCTIONAL DESCRIPTION:



Logic Diagram and Logic Symbol

Differential Input	Enable		Outputs
A , B	G	$\bar{G}$	Y
VID ≥ 100mV	H	X	H
	X	L	H
-100mV > VID >100mV	H	X	?
	X	L	?
VID ≤ -100mV	H	X	L
	X	L	L
OPEN	H	X	H
	X	L	H
Don't care (X)	L	H	Z
L=low level, H=high level, X=irrelevant, Z=high impedance, ?=indeterminate			

Functional Truth Table

ABSOLUTE MAXIMUM RATINGS (1):

Over operating free-air temperature range (unless otherwise noted)

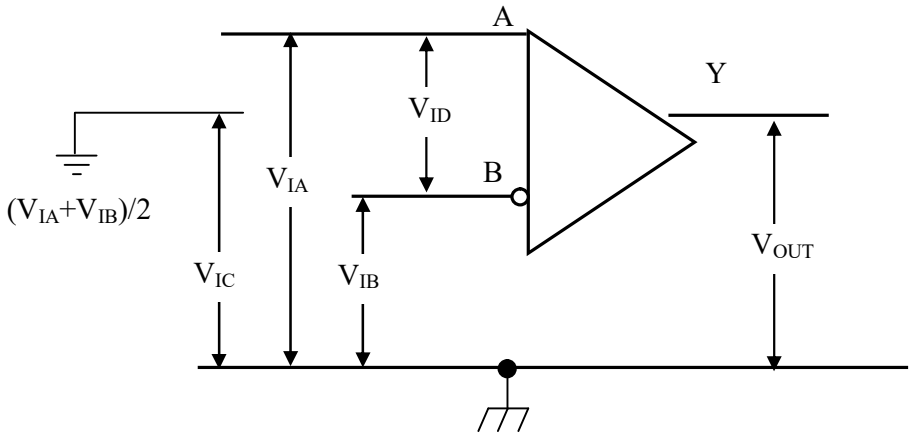
PARAMETER		UNIT
Supply Voltage Range (V_{DD})		–0.5V to 4.3V
Voltage Range (V_I)	Enables and Output	–0.5V to V_{DD} + 0.5V
	A or B	–0.5 V to 4.0 V
Max. Junction Temperature (T_J)		150°C
Storage Temperature Range (T_{STG})		–65°C to 150°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS:

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	3	3.3	3.6	V
V_{IH}	High Level Input Voltage (G / $\bar{G}$)	2.0	-	-	V
V_{IL}	Low Level Input Voltage (G / $\bar{G}$)	-	-	0.8	V
$\|V_{ID}\|$	Magnitude Of Differential Input Voltage	0.1	-	0.6	V
V_{IC}	Common Mode Input Voltage Range	$\|V_{ID}\|$ / 2	-	2.4 – ($\|V_{ID}\|$ / 2)	V
T_A	Operating Free Air Temperature	-55	-	+125	ºC

TEST CIRCUIT:



DC ELECTRICAL SPECIFICATIONS:

Test condition: V_{DD} =3.3V±0.3V, T_{AMB} = -55ºC to 125ºC

Symbol	Parameters	Test Conditions	Pin	Min.	Typ.	Max.	Units
V_{ITH+}	Input Voltage High	V_{IC} = 1.2V	A, B	-	-	100	mV
V_{ITH-}	Input Voltage Low	V_{IC} = 1.2V		-100	-	-	mV
V_{OH}	Output Voltage High	I_{OH} = -8mA	Y	2.4	3.1	-	V
V_{OL}	Output Voltage Low	I_{OL} = +8mA		-	0.13	0.4	V
I_{IH}	High Level Input Current	V_{IH} = 2.0V	G, $\bar{G}$	-	-	±20	uA
I_{IL}	Low Level Input Current	V_{IL} = 0.8V		-	-	±20	uA
I_{IN}	Receiver Input Current	V_{IN}=0 or 2.4V	A, B	-	-8.5	±20	uA
I_{OZ}	High-impedance output current	V_O=0 or V_{DD}	Y	-	-	±10	uA
$I_{I(OFF)}$	Power-off Input Current (Cold Spare Leakage)	V_{DD} = 0V, V_I = 0 or V_{DD}	A, B	-	8.0	±20	uA
I_{DD} (static)	I_{DDNL} (Driver Enabled)	No Load, Inputs = open/steady state	V_{DD}	15	30.0	50	mA
	I_{DDZ} (Driver Disabled)	No Load, Inputs = open/steady state		0.2	0.75	3.3	mA

AC ELECTRICAL SPECIFICATIONS:

Test condition: V_{DD} = 3.3V, Freq. @ 1 MHz, C_L=10pF, T_{AMB} = -55ºC to 125ºC

Symbol	Parameter	Min.	Typical	Max.	Units
t_r	Output signal rise time (20% to 80%)	-	0.738	1.5	ns
t_f	Output signal fall time (20% to 80%)	-	0.568	1.5	ns
t_{PHLD}	propagation delay	1.0	2.82	5	ns
t_{PLHD}	propagation delay	1.0	2.86	5	ns
$T_{SKD} = \lvert t_{PHLD} - t_{PLHD} \rvert$	skew in delay	-	0.05	0.5	ns
t_{PHZ}	Delay, high-level-to-high-impedance output	-	4.5	15	ns
t_{PLZ}	Delay, low-level-to-high-impedance output	-	4.8	15	ns
t_{PZH}	Delay, high-impedance-to-high-level output	-	4.4	15	ns
*t_{PZL}	Delay, high-impedance-to-low-level output	-	**1.6**	-	**us**

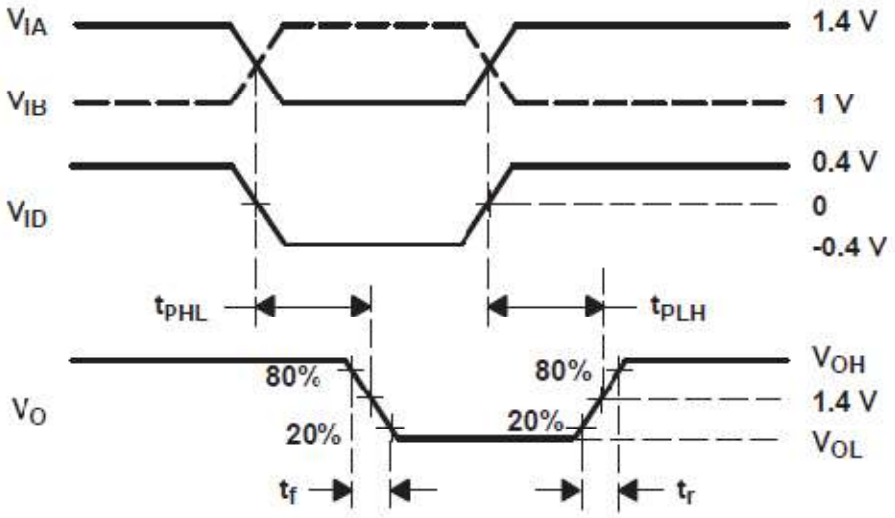
*High Value Of t_{PZL} observed at receiver output due To high Voltage Spike at output

RECEIVER THRESHOLD TEST VOLTAGES:

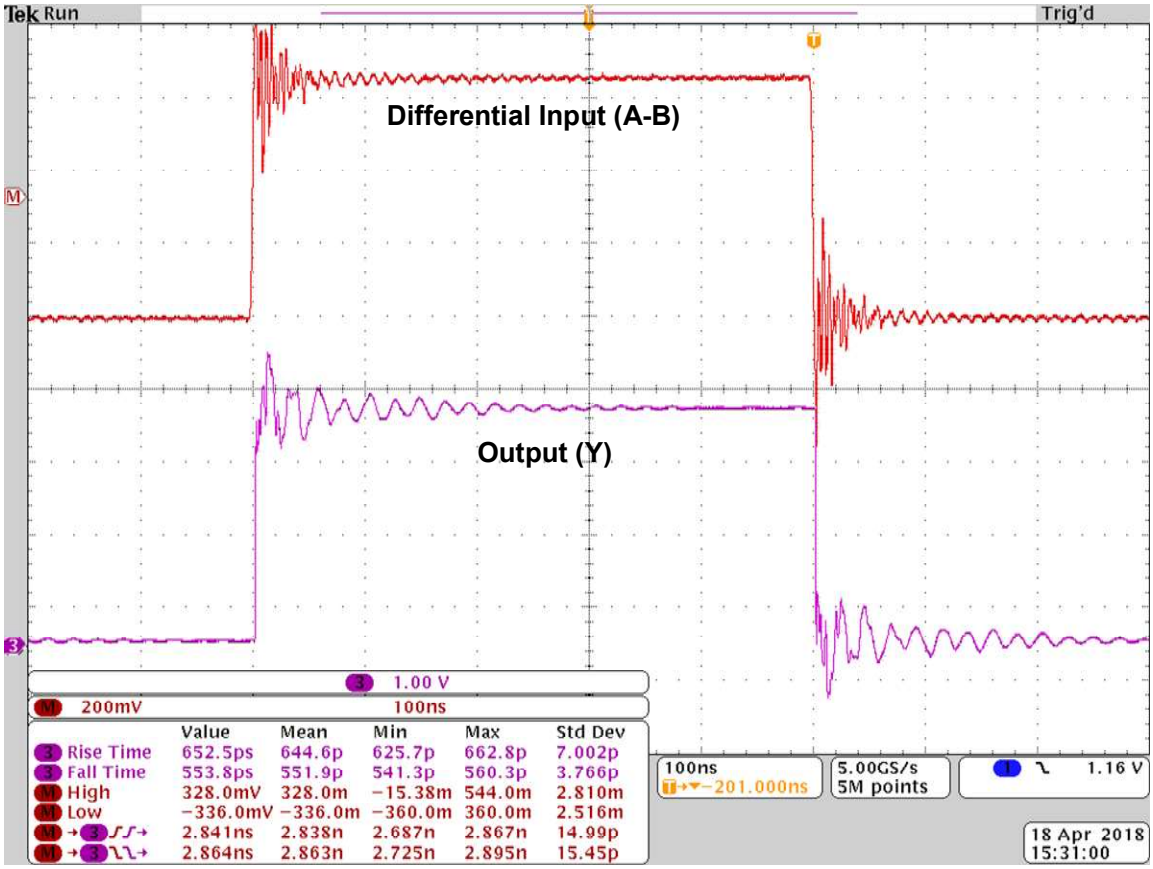
Applied Input Voltages		Resulting Differential Input Voltages	Resulting Common Mode Input Voltages	Expected Output Voltage
V_{IA} (V)	V_{IB} (V)	V_{ID} (mV)	V_{IC} (V)	V_{OY} (V)
1.25	1.15	+100	1.20	V_{DD}
1.15	1.25	-100	1.20	V_{SS}
2.40	2.30	+100	2.35	V_{DD}
2.30	2.40	-100	2.35	V_{SS}
0.10	0.00	+100	0.05	V_{DD}
0.00	0.10	-100	0.05	V_{SS}
1.5	0.9	+600	1.20	V_{DD}
0.9	1.5	-600	1.20	V_{SS}
2.4	1.8	+600	2.10	V_{DD}
1.8	2.4	-600	2.10	V_{SS}
0.6	0.0	+600	0.30	V_{DD}
0.0	0.6	-600	0.30	V_{SS}

Receiver Minimum and Maximum Input Threshold Test Voltages

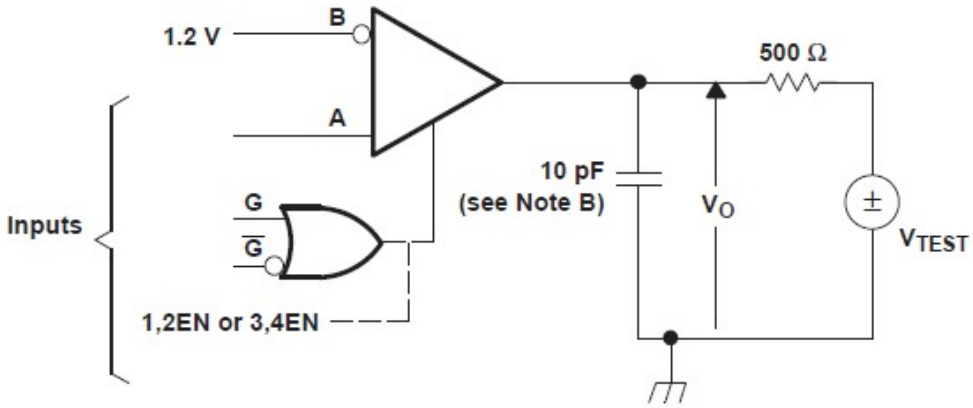
SWITCHING WAVEFORM:

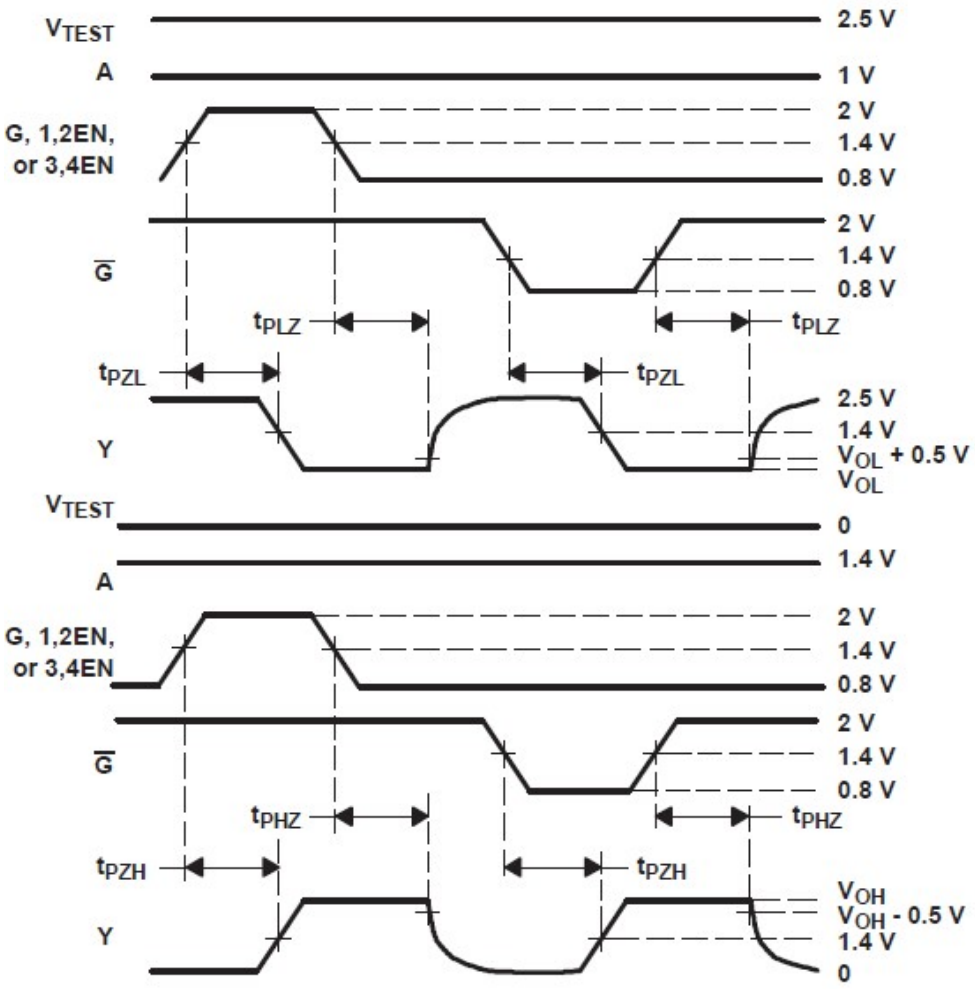


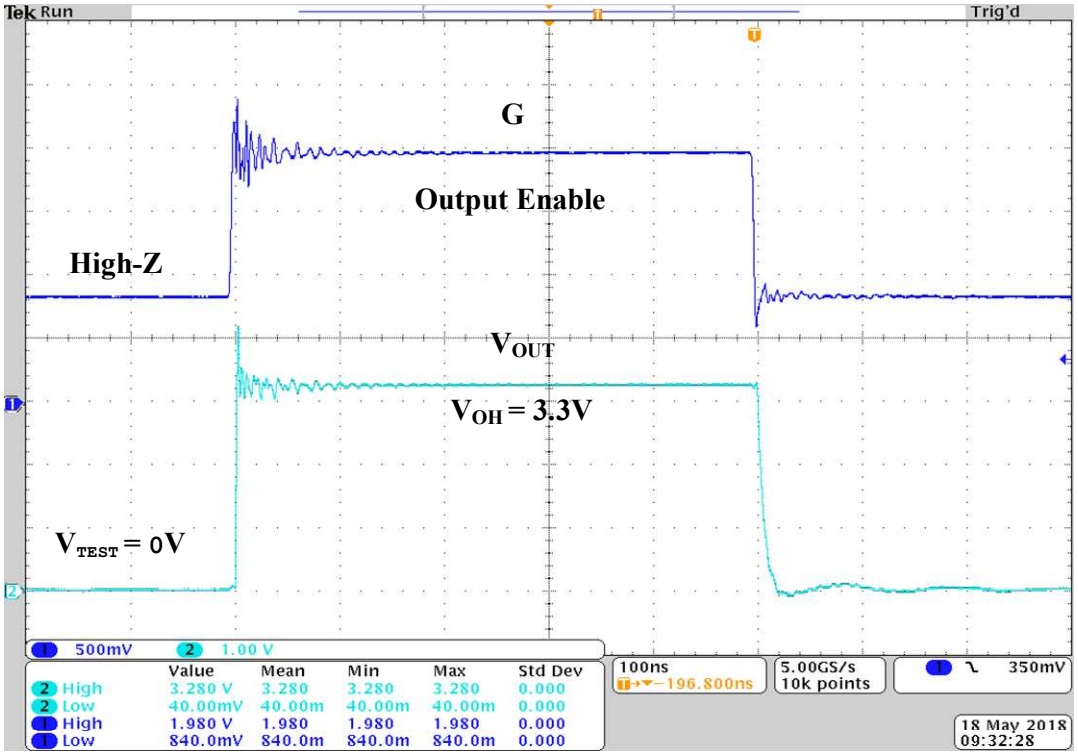
Switching Waveforms



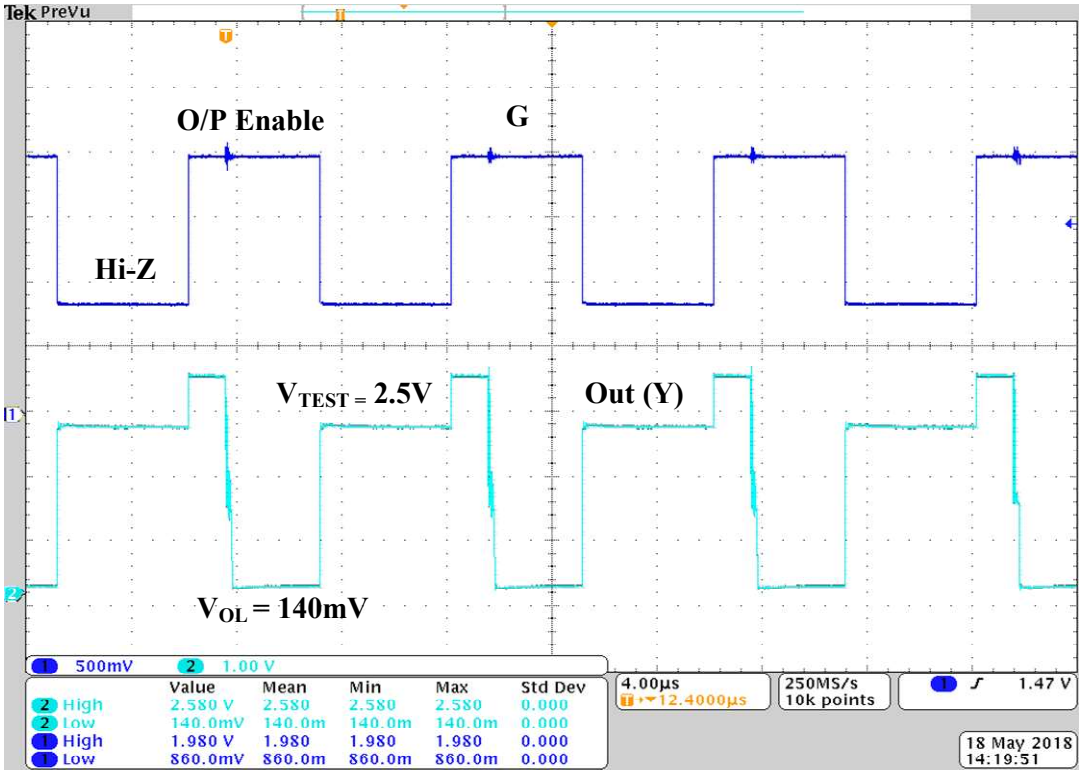
Test Circuits for High Impedance Switching Parameter Measurement



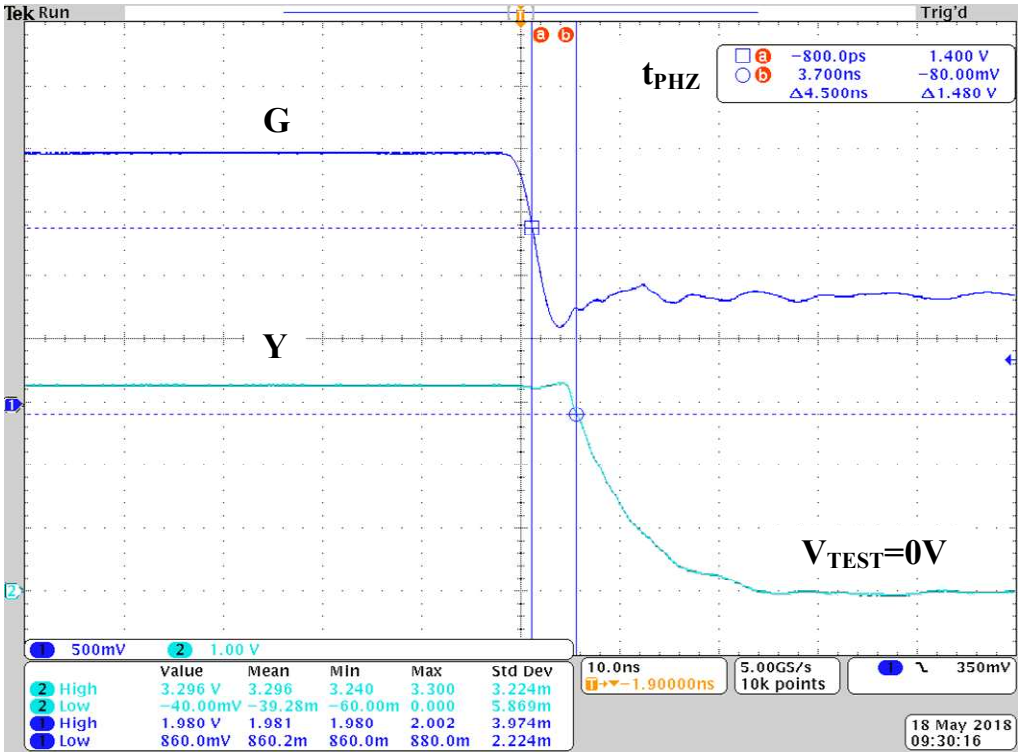




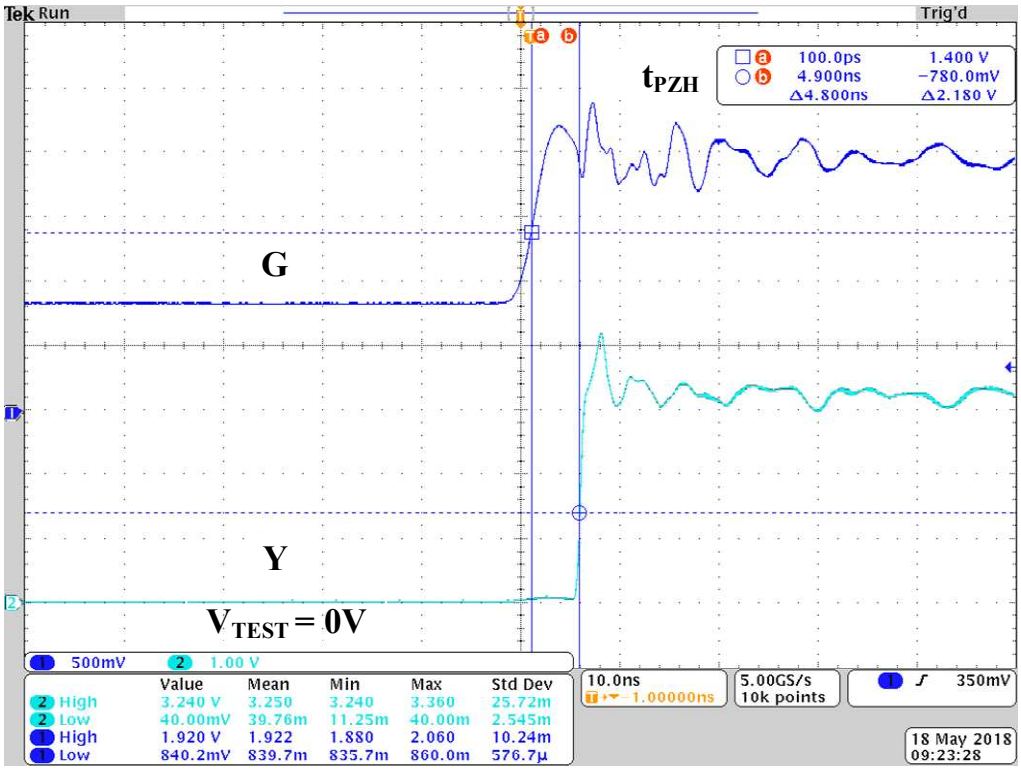
High-Z to H delay Test waveform (Vtest=0V)



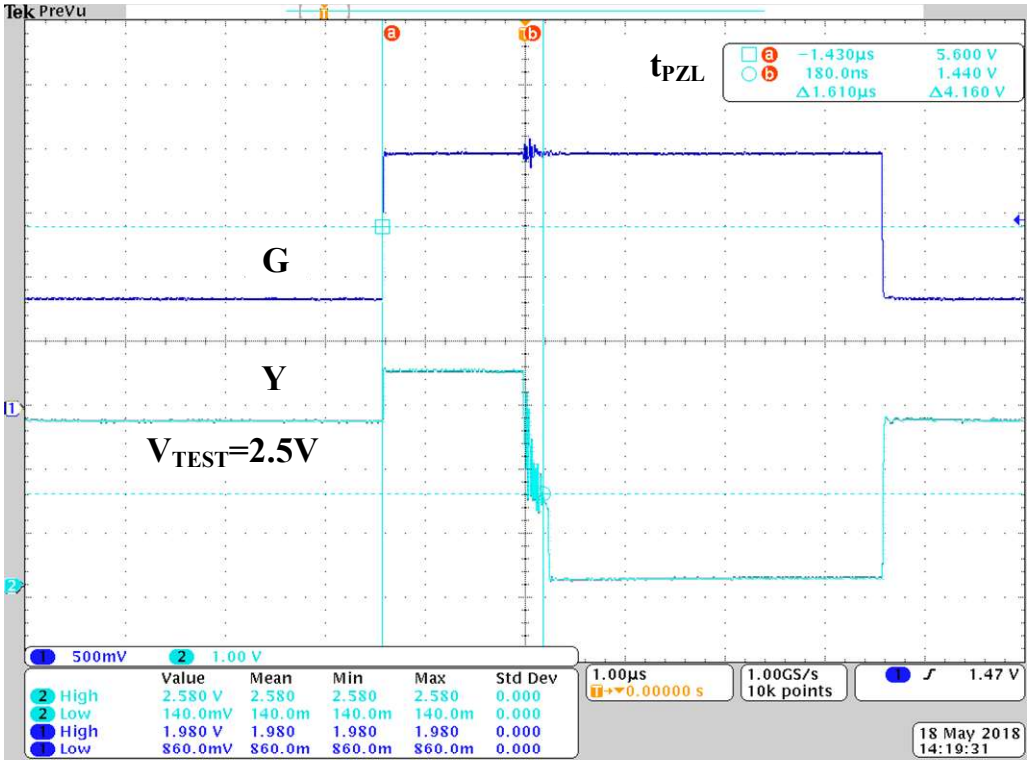
High-Z to L delay Test waveform (Vtest=2.5V)



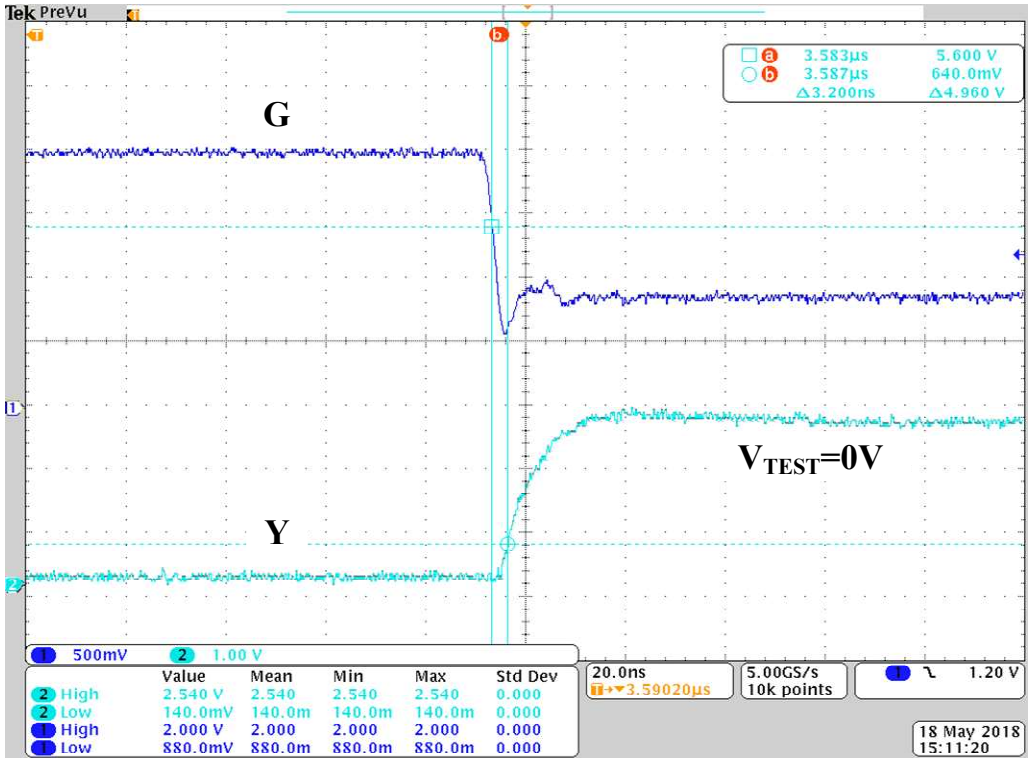
Test waveform for t_{PHZ}



Test waveform for t_{PZH}

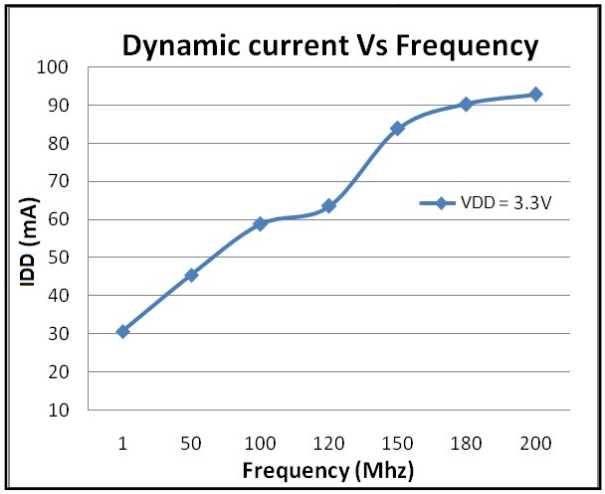


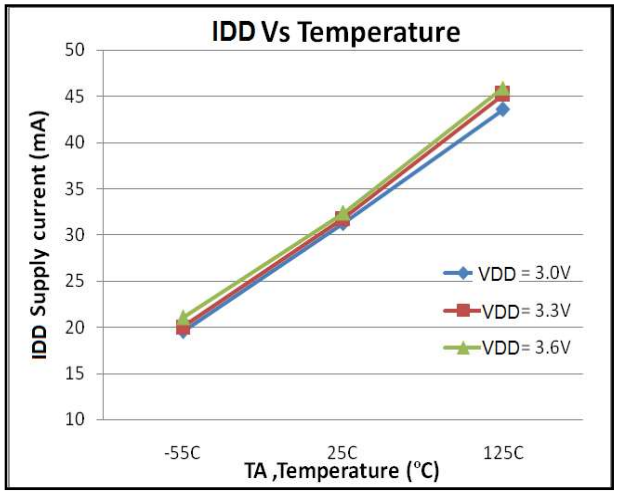
Test Waveform for t_{PZL}

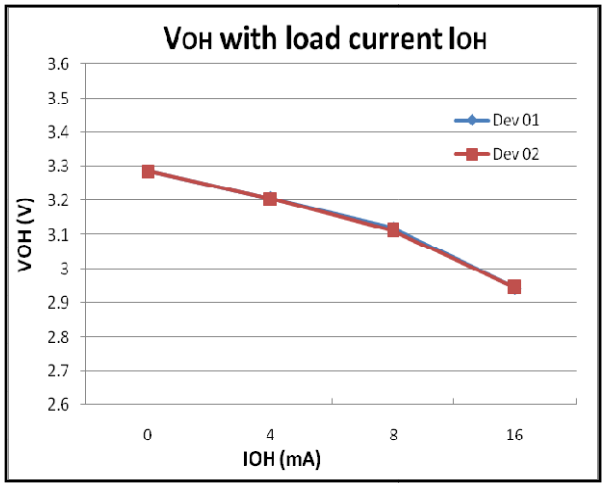


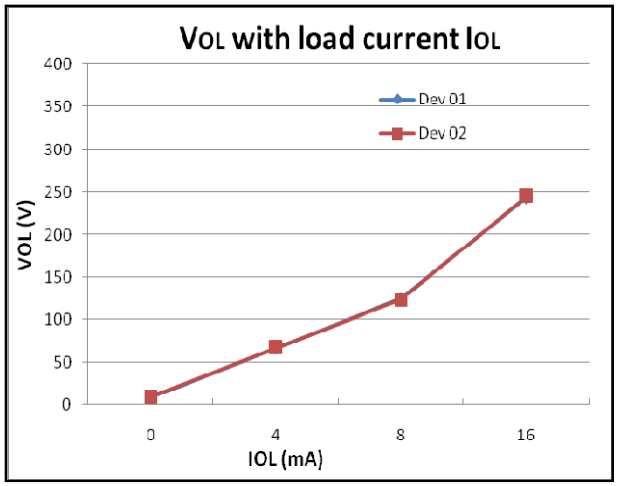
Test waveform for t_{PLZ}

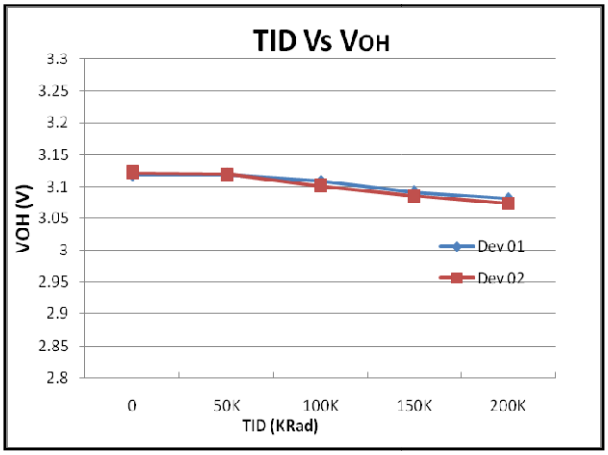
TYPICAL CHARACTERISTICS:

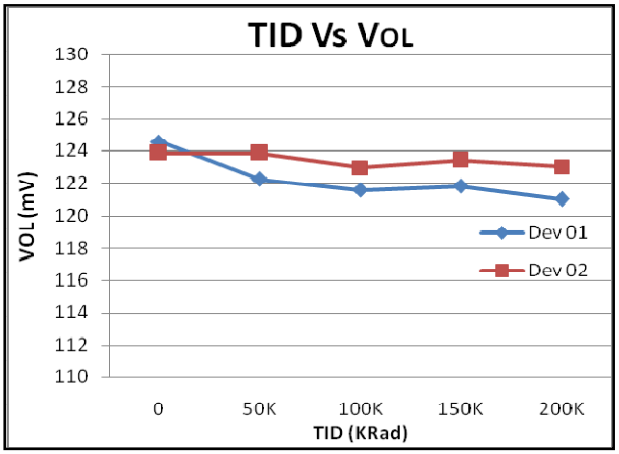








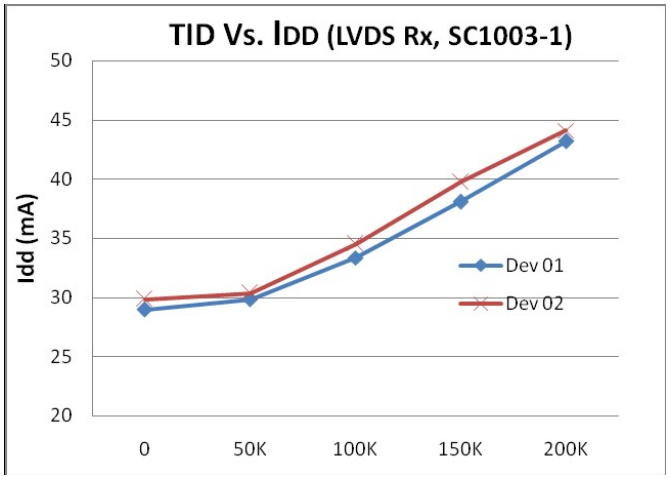




RADIATION CHARACTERISTICS:

❖ Total Ionization Dose (TID) Testing

- TID testing of QLVDS Receiver (SC1003-1) is performed for radiation level up to 200 KRad.
- No functional degradation and no significant change in device parameters such as IIL, IIH, VOL & VOH was observed up to 200KRad.
- Static supply current increases with radiation dose, shown in figure below.

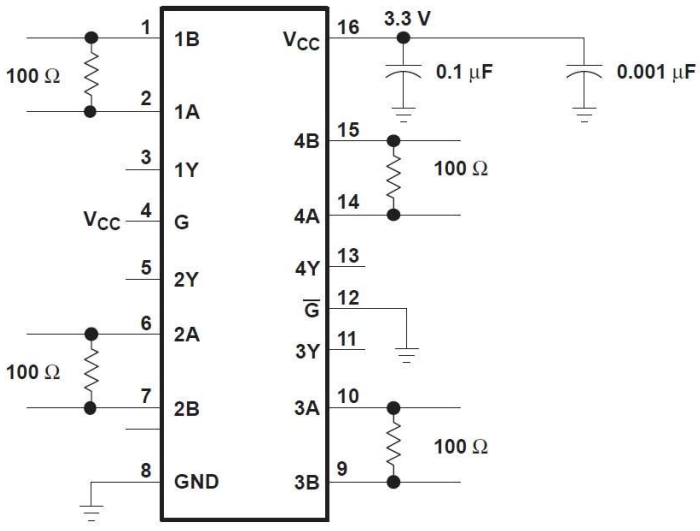


❖ Single Event Effect (SEE) Testing

SEE testing of QLVDS Receiver (SC1003-1) is performed at two different LET energy ion beams Ni+ (30 MeV-cm2/mg) and Ag+ (50 MeV-cm2/mg) for a Fluence of 10^6 ions/cm^2.

- No Single Event latch-up (SEL) was observed up to LET of 50 MeV-cm2/mg. Supply current (I_{DD}) remains within specification throughout testing.
- No Single Event transient (SET) was observed up to LET of 50 MeV-cm2/mg.

APPLICATION CIRCUIT:



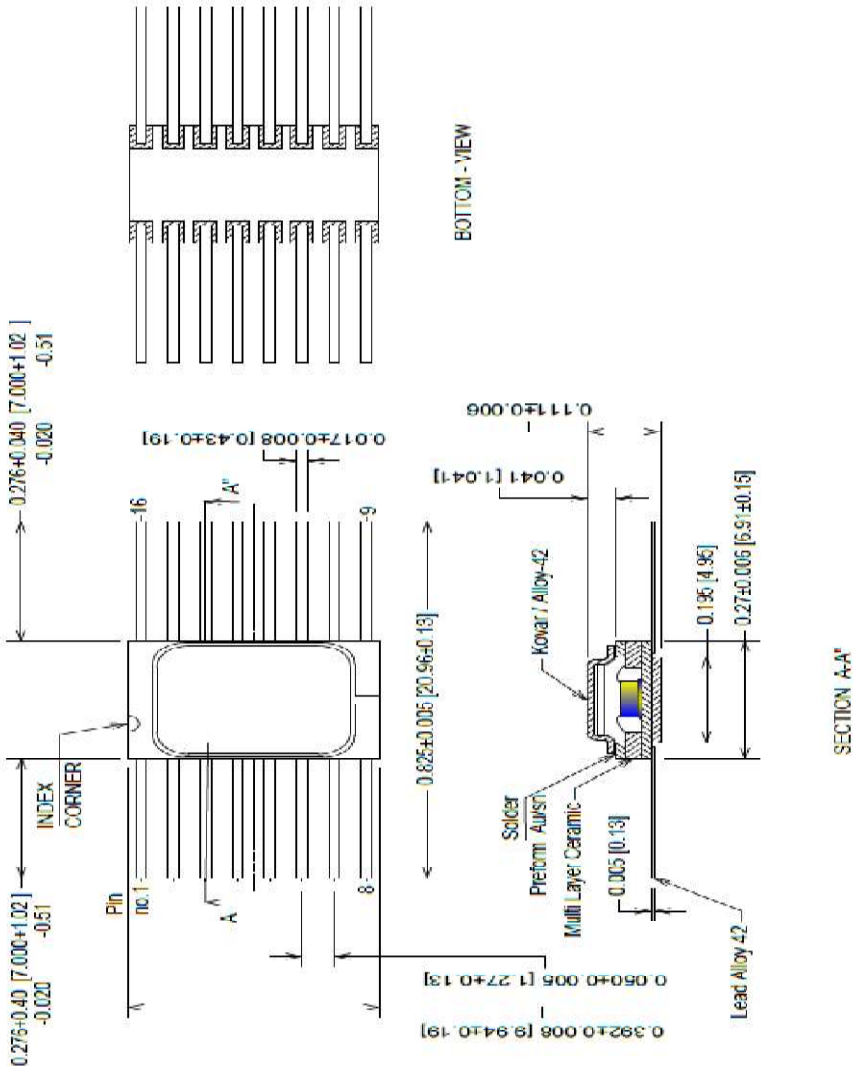
Typical Application circuit of QLVDS Receiver

REVISION HISTORY:

S. No.	Version	Date of release	Description
1	1.0	26th March 2019	New

PACKAGE DRAWING (CERAMIC-DUAL-FLATPACK):

NOTE: All linear dimensions are in inches (mm.)



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