SEMI-CONDUCTOR LABORATORY
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SPACE APPLICATIONS CENTRE
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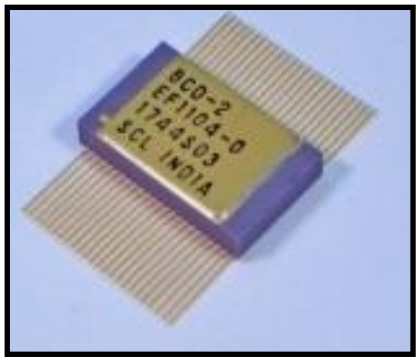


EF1104-0

DATA SHEET

4-CHANNEL BIPOLAR CLOCK DRIVER

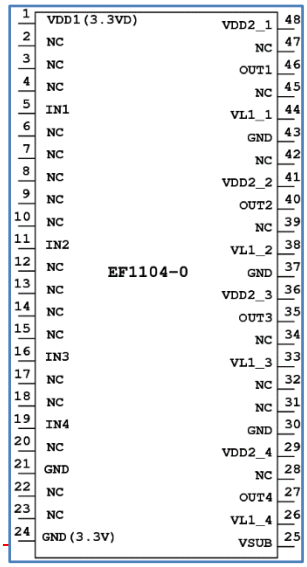
BCD-2

Version 1.0 August 2022

4-Channel Bipolar Clock Driver (EF1104-0)

FEATURES:

- 3.3V power supply for VDD1
- High voltage 0.35um AMS CMOS Process (H35B4D3)
- Four channels input
- Input-compatibility with TTL/LVCMOS/CMOS logic
- Input level shifters
- -5V ≤VL ≤5V
- 6V ≤ VH ≤ 15V
- Min. VH-VL ≥6V
- Low quiescent current
- Low power dissipation (<5W at 5MHz with output load of 850pf on each output)
- Wide output voltage range
- 15ns t_r/t_f at 850pF load
- <3ns rise and fall time mismatch
- <4.5ns prop delay mismatch
- Up to 15 MHz operating frequency Note-1
- Hermetic sealed 48 pin Lead Flat package (DIL)
- θ_{jc}: 2.53°C/Watt
- Full Mil-temp Range Operation TA -55°C to +125°C
- Radiation Hardness
  - **TID 300Krad(Si)**
  - **SEE Hardness**
  - **LET (SEL and SEU Immunity) 50 MeV-cm^2/mg**



PIN DIAGRAM

PRODUCT DESCRIPTION:

EF1104-0 is a four-channel high speed Bipolar Clock Driver ASIC, designed inHigh voltage 0.35um AMS CMOS Process (H35B4D3). It is capable of running at clock rates from DC to 15MHz and features 2A typical peak drive capability and a nominal on-resistance of just 3Ω. The device is packaged in 48 pin flat ceramic quad and has four independent channels. It can be switched between respective high (VH) or low (VL) voltages depending on the given input. The inputs are compatible with both 3.3V and 5V CMOS logic. All four high (VH) or low (VL) supply pins can be independently selected in the quad device EF1104-0. The EF1104-0 is ideal for bipolar/Unipolar operation and driving high capacitive loads, such as storage and vertical clocks in CCD/TDI CCDs applications. It is also well suited for level shifting and clock driving for negative low voltage applications.

The EF1104-0 is inverting bipolar clock driver with very fast rise and fall times, which are typically matched to within 3ns. The propagation delay is also matched between rising and falling edges to typically within 4.5ns and specified for operation over the full ambient temperature range of -55°C to +125°C.

Applications:

- CCD Drivers,
- Clock/line Drivers,
- Level-Shifters,
- TDI Detectors

DEVICE SUMMARY

Table-1: Device Summary

Reference	Package	Pins	Lead Finish	Description
EF1104-0	Ceramic Flat Pack	48	Gold	Flight Model

Note-1: The device can be operated up to 15MHz with reduced output load.

Note-2: Design Values.

Note-3: Characterization data on sample basis.

PLEASE NOTE THAT FREQUENCY AND LOAD SHALL BE SLECTED IN SUCH A WAY THAT POWER CONSUMPTION ($P_{total} = P_{load} + P_Q + P_{Q(Dyanamic)}$) IS <5W

4-Channel Bipolar Clock Driver (EF1104-0)

BLOCK LEVEL DIAGRAM

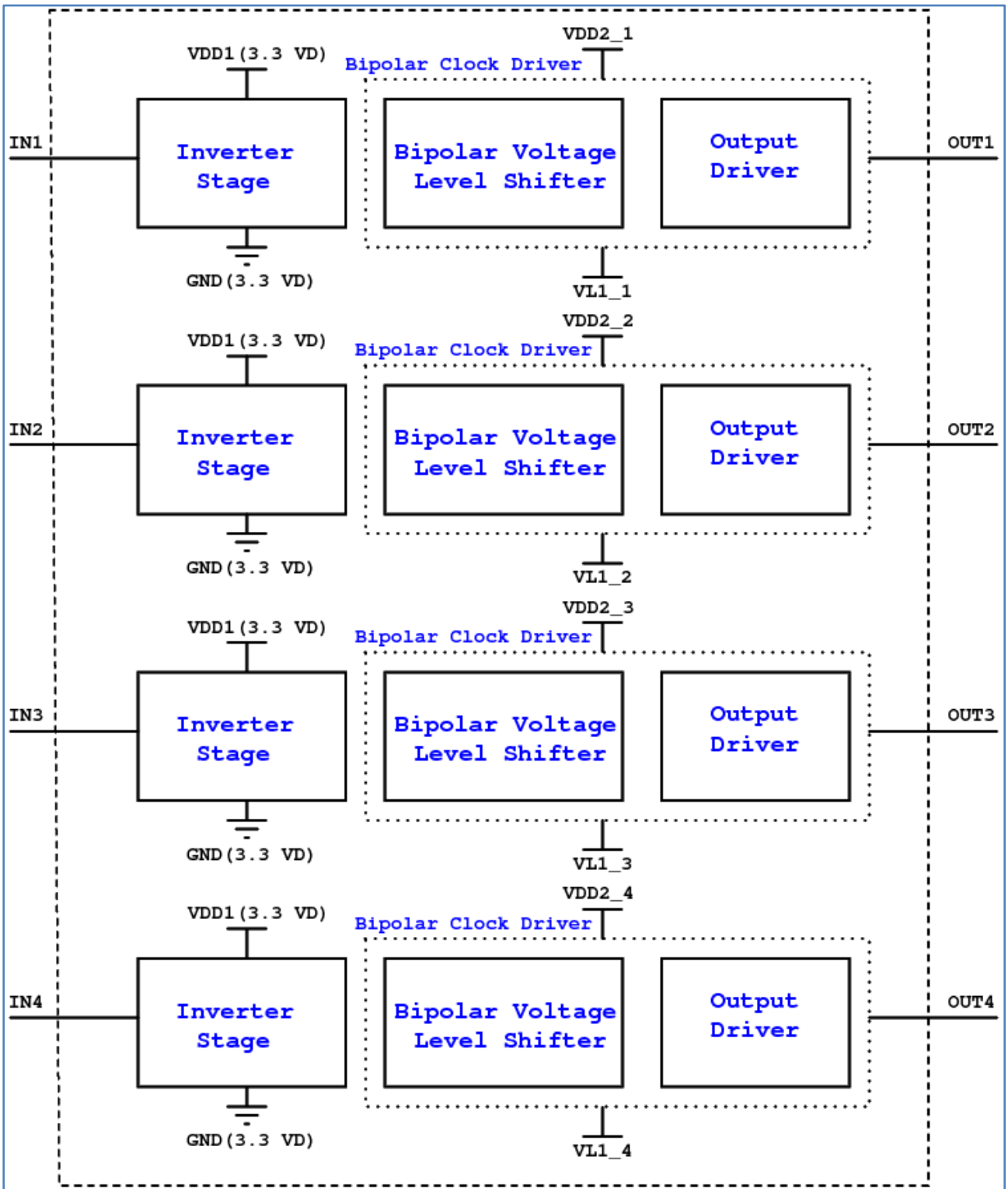


Figure-1: Block Level Diagram

4-Channel Bipolar Clock Driver (EF1104-0)

PIN CONFIGURATION:

Table-2: Pin Configuration

Pin No.	Pin Name	Pin Type	Pin Description
1	VDD1(3.3VD)	AP	Input Interface Buffer Supply (3.3V/5V*) to BCD.
2	NC	NC	NC
3	NC	NC	NC
4	NC	NC	NC
5	IN1	DI	BCD TTL/LVCMOS/5V* Level Input for channel 1
6	NC	NC	NC
7	NC	NC	NC
8	NC	NC	NC
9	NC	NC	NC
10	NC	NC	NC
11	IN2	DI	BCD TTL/LVCMOS/5V* Level Input for channel 2
12	NC	NC	NC
13	NC	NC	NC
14	NC	NC	NC
15	NC	NC	NC
16	IN3	DI	BCD TTL/LVCMOS/5V* Level Input for channel 3
17	NC	NC	NC
18	NC	NC	NC
19	IN4	DI	BCD TTL/LVCMOS/5V* Level Input for channel 4
20	NC	NC	NC
21	GND	AGND	Analog Ground
22	NC	NC	NC
23	NC	NC	NC
24	GND(3.3VD)	GND	Digital Ground
25	VSUB	AP	Connected to VL externally
26	VL1_4	AP	Driver Low Rail supply for channel 4
27	OUT4	AO	Driver Output for channel 4
28	NC	NC	NC
29	VDD2_4	AP	Driver High Rail supply for channel 4
30	GND	AGND	Analog Ground
31	NC	NC	NC
32	NC	NC	NC
33	VL1_3	AP	Driver Low Rail supply for channel 3
34	NC	NC	NC
35	OUT3	AO	Driver Output for channel 3
36	VDD2_3	AP	Driver High Rail supply for channel 3
37	GND	AGND	Analog Ground
38	VL1_2	AP	Driver Low Rail supply for channel 2
39	NC	NC	NC
40	OUT2	AO	Driver Output for channel 2
41	VDD2_2	AP	Driver High Rail supply for channel 2
42	NC	NC	NC
43	GND	AGND	Analog Ground
44	VL1_1	AP	Driver Low Rail supply for channel 1
45	NC	NC	NC
46	OUT1	AO	Driver Output for channel 1
47	NC	NC	NC
48	VDD2_1	AP	Driver High Rail supply for channel 1

- Pin Type DI = Digital Input, AO = Analog Output, AP = Analog Power, AGND = Analog Ground
- De-coupling capacitors of 10uF and 0.1uF in parallel are recommend on Analog Power pins w.r.t ground pin
- * For 5V interface

4-Channel Bipolar Clock Driver (EF1104-0)

RECOMMENDED OPERATING CONDITIONS:

Table-3: Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD1} to GND	Supply Voltage (VDD1)	3.0	3.3	5.0	V
V_{DD2} to GND	Supply Voltage (VDD2)	6.0	14	15.0	V
V_L to GND	VL Low Voltage	-5	0	5	V
V_{SUB} to GND*,**	VSUB Voltage	V_L	V_L	V_L	V
V_{IH}	Logic"1" Input Voltage	2.0	3.3	5	V
V_{IL}	Logic"0" Input Voltage	-0.2	0	0.8	V
T_A	Temperature range	-55	25	+125	ºC

***For V_L>0.5V, V_{SUB} must be connected to GND with 1kohm resistor. Refer Application Note-1.**

****All the channels of one device should be configured either in unipolar mode or bipolar mode. For VL≤ 0.5V, VSUB should be tied to VL (lowest/most negative) and for VL>0.5V, V_{SUB} must be connected to GND with 1kΩ resistor. Refer Application Note-1.**

ABSOLUTE MAXIMUM RATINGS:

Table-4: Absolute Maximum Rating

PARAMETER	VALUE	Units
Supply Voltage range **(V_{DD2} to V_{SUB})**	20	**V**
Supply Voltage range **(V_{DD1} to GND)**	6.0	**V**
Supply Voltage range **(V_L to V_{SUB})**	0*	**V**
T_{stg}, Storage temperature range	–65°C to 150°C	°C

***V_{SUB} should be shorted to V_L.**

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

4-Channel Bipolar Clock Driver (EF1104-0)

DC ELECTRICAL SPECIFICATIONS:

Test condition: V_{DD1} = 3.3V, V_{DD2} = 9V, V_L = V_{SUB} = -5V, GND = 0V, T_A = -55ºC to 125ºC, C_{LOAD}=850pF, Frequency=5MHz.

Table-5: DC Electrical Characteristics

Symbol	Parameter	Test Conditions	Pin	Min.	Typ.	Max.	Unit
INPUT							
V_{IH}	Logic"1" Input Voltage	V_{IH}=3.3V V_{IL}=0V	IN1, IN2, IN3, IN4,	2.0		5	
V_{IL}	Logic"0" Input Voltage				0	0.8	
I_{IH}	Logic "1" Input Current				0.1	10	uA
I_{IL}	Logic "0" Input Current				0.1	10	uA
C_{IN}	Input Capacitance				<5.7 Note2		pF
R_{IN}	Input Resistance				>5 Note2		MΩ
OUTPUT							
R_{OH}	ON Resistance VH to OUT		OUT1, OUT2, OUT3, OUT4		3 Note2		Ω
R_{OL}	ON Resistance VL to OUT				3 Note2		Ω
V_{OH}	Output Voltage High				9.1	9.2	V
V_{OL}	Output Voltage Low			-5.0	-4.79		V
POWER SUPPLY							
I_{DDS} (static)	I_{DDH} (Inputs at High)	3.3V at all Inputs	VDD1		0.32	5	mA
			VDD2		1.60	5	
			VL/VSUB	-20.0	-5.17		
	I_{DDL} (Inputs at Low)	0V at all Inputs	VDD1		0.32	5	mA
			VDD2		2.70	5	
			VL/VSUB	-20	-6.23		
I_{DD} (Dynamic)	I_{DD} Dynamic	0 to 3.3V square wave input with frequency of 5MHz, 50% duty cycle	VDD1		0.65	2	mA
			VDD2		305.08	350	
			VL/VSUB	-350	-309.61		

AC ELECTRICAL SPECIFICATIONS:

Test condition: V_{DD1} = 3.3V, V_{DD2} = 9V, V_L = V_{SUB} = -5V, GND = 0V, T_A = -55ºC to 125ºC, C_{LOAD}=850pF, Frequency=5MHz.

Table-6: AC Electrical Characteristics

Symbol	Parameter	Test Conditions	Typical	Units
t_R	Output rise time (10% to 90%)	0 to 3.3V square wave input with frequency of 5MHz , 50% duty cycle	14.75	ns
t_F	Output fall time (90% to 10%)		12.70	ns
$t_{RF\Delta}$	t_R, t_F mismatch		2.05	ns
t_{D+}	Turn-Off Delay Time		27.67	ns
t_{D-}	Turn-On Delay Time		26.25	ns
t_{DD}	t_{D-1} - t_{D-2} Mismatch		1.42	ns

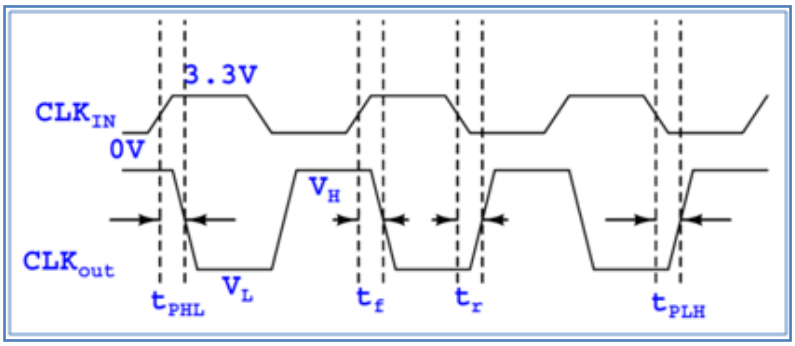


Figure-2: Timing Diagram

4-Channel Bipolar Clock Driver (EF1104-0)

Test condition: V_{DD1} = 3.3V, V_{DD2} = 15V, V_L = V_{SUB} = 0V, GND = 0V, T_A = -55ºC to 125ºC, C_{LOAD}=850pF, Frequency=5MHz. (Note-3)

Table-7: DC Electrical Characteristics

Symbol	Parameter	Test Conditions	Pin	Min.	Typ.	Max.	Unit
INPUT							
V_{IH}	Logic"1" Input Voltage	V_{IH}=3.3V V_{IL}=0V	IN1, IN2, IN3, IN4,	2.0		5	
V_{IL}	Logic"0" Input Voltage				0	0.8	
I_{IH}	Logic "1" Input Current				0.1	10	uA
I_{IL}	Logic "0" Input Current				0.1	10	uA
C_{IN}	Input Capacitance				<5.7 Note2		pF
R_{IN}	Input Resistance				>5 Note2		MΩ
OUTPUT							
R_{OH}	ON Resistance VH to OUT		OUT1, OUT2, OUT3, OUT4		3 Note2		Ω
R_{OL}	ON Resistance VL to OUT				3 Note2		Ω
V_{OH}	Output Voltage High				14.2	14.6	V
V_{OL}	Output Voltage Low				0.82	1.4	V
POWER SUPPLY							
I_{DDS} (static)	I_{DDH} (Inputs at High)	3.3V at all Inputs	VDD1		0.32	5	mA
			VDD2		2.85	5	
			VL/VSUB		6.50	20	
	I_{DDL} (Inputs at Low)	0V at all Inputs	VDD1		0.32	5	mA
			VDD2		2.86	5	
			VL/VSUB		6.59	20	
I_{DD} (Dynamic)	I_{DD} Dynamic	0 to 3.3V square wave input with frequency of 5MHz , 50% duty cycle	VDD1		0.65	2	mA
			VDD2		328.08	350	
			VL/VSUB	-350	-319.61		

Test condition: V_{DD1} = 3.3V, V_{DD2} = 15V, V_L = V_{SUB} = 0V, GND = 0V, T_A = -55ºC to 125ºC, C_{LOAD}=850pF, Frequency=5MHz. (Note-3)

Table-8: AC Electrical Characteristics

Symbol	Parameter	Test Conditions	Typical	Units
t_R	Output rise time (10% to 90%)	0 to 3.3V square wave input with frequency of 5MHz, 50% duty cycle	14.70	ns
t_F	Output fall time (90% to 10%)		15.66	ns
$t_{RF\Delta}$	t_R, t_F Mismatch		0.96	ns
t_{D+}	Turn-Off Delay Time		26.85	ns
t_{D-}	Turn-On Delay Time		31.05	ns
t_{DD}	t_{D-1} - t_{D-2} Mismatch		4.20	ns

4-Channel Bipolar Clock Driver (EF1104-0)

Test condition: V_{DD1} = 3.3V, V_{DD2} = 6V, V_L = V_{SUB} = 0V, GND = 0V, T_A = 25ºC, C_{LOAD}=850pF, Frequency=5MHz. (Note-3)

Table-9: DC Electrical Characteristics

Symbol	Parameter	Test Conditions	Pin	Min.	Typ.	Max.	Unit
INPUT							
V_{IH}	Logic"1" Input Voltage	V_{IH}=3.3V V_{IL}=0V	IN1, IN2, IN3, IN4,	2.0		5	
V_{IL}	Logic"0" Input Voltage				0	0.8	
I_{IH}	Logic "1" Input Current				0.1	10	uA
I_{IL}	Logic "0" Input Current				0.1	10	uA
C_{IN}	Input Capacitance				<5.7 Note2		pF
R_{IN}	Input Resistance				>5 Note2		MΩ
OUTPUT							
R_{OH}	ON Resistance VH to OUT		OUT1, OUT2, OUT3, OUT4		3 Note2		Ω
R_{OL}	ON Resistance VL to OUT				3 Note2		Ω
V_{OH}	Output Voltage High				5.7	5.8	V
V_{OL}	Output Voltage Low				0.6	0.6	V
POWER SUPPLY							
I_{DDS} (static)	I_{DDH} (Inputs at High)	3.3V at all Inputs	VDD1		0.32	5	mA
			VDD2		0.94	5	
			VL/VSUB		6.50	20	
	I_{DDL} (Inputs at Low)	0V at all Inputs	VDD1		0.32	5	mA
			VDD2		1.05	5	
			VL/VSUB		6.60	20	
I_{DD} (Dynamic)	I_{DD} Dynamic	0 to 3.3V square wave input with frequency of 5MHz , 50% duty cycle	VDD1		0.65	2	mA
			VDD2		115.18	350	
			VL/VSUB	-350	-105.61		

Test condition: V_{DD1} = 3.3V, V_{DD2} = 6V, V_L = V_{SUB} = 0V, GND = 0V, T_A = 25ºC, C_{LOAD}=850pF, Frequency=5MHz. (Note-3)

Table-10: AC Electrical Characteristics

Symbol	Parameter	Test Conditions	Typical	Units
t_R	Output rise time (10% to 90%)	0 to 3.3V square wave input with frequency of 5MHz , 50% duty cycle	11.26	ns
t_F	Output fall time (90% to 10%)		13.89	ns
$t_{RF\Delta}$	t_R, t_F Mismatch		2.63	ns
t_{D+}	Turn-Off Delay Time		36.85	ns
t_{D-}	Turn-On Delay Time		37.05	ns
t_{DD}	t_{D-1} - t_{D-2} Mismatch		0.20	ns

4-Channel Bipolar Clock Driver (EF1104-0)

Test condition: V_{DD1} = 3.3V, V_{DD2} = 9V to 12V, V_L = 3V to 6V, V_{SUB} = 0V, GND = 0V, Rs = 1 KΩ T_A = 25ºC, CLOAD=850pF, Frequency=5MHz. (Note-3)

Table-11: Supply Current Data with Different V_{DD2} and VL

Symbol	Parameter	Test Conditions	Typical Values			Unit
			VDD1	VDD2	VL	
I_{DDS} (static)	I_{DDH} (Inputs at High) 3.3V at all Inputs	**V_{DD2} = 9V, V_L = 3V**	0.175	0.05	48.933	mA
		V_{DD2} = 10V, V_L = 4V	0.2	0.05	65.386	
		V_{DD2} = 11V, V_L = 5V	0.25	0.05	80.366	
		V_{DD2} = 12V, V_L = 6V	0.25	0.05	93.599	
	I_{DDL} (Inputs at Low) 0V at all Inputs	**V_{DD2} = 9V, V_L = 3V**	0.2	0.05	48.983	mA
		V_{DD2} = 10V, V_L = 4V	0.2	0.05	65.377	
		V_{DD2} = 11V, V_L = 5V	0.2	0.05	80.261	
		V_{DD2} = 12V, V_L = 6V	0.175	0.17	93.436	
I_{DD} (Dynamic)	I_{DD} Dynamic 0 to 3.3V square wave input with frequency of 5MHz , 50% duty cycle	**V_{DD2} = 9V, V_L = 3V**	0.82	118.46	-69.50	mA
		V_{DD2} = 10V, V_L = 4V	0.84	119.06	-53.68	
		V_{DD2} = 11V, V_L = 5V	0.91	119.74	-39.41	
		V_{DD2} = 12V, V_L = 6V	0.91	120.45	-26.87	

Table-12: AC Electrical Characteristics with Different V_{DD2} and VL

Parameter	Test Conditions	Typical Values					
AC Parameters		**t_R (ns)**	**t_F (ns)**	**+Duty (%)**	**-Duty (%)**	**V_{OH} (V)**	**V_{OL} (V)**
0 to 3.3V square wave input with frequency of 5MHz , 50% duty cycle	V_{DD2} = 9V, V_L = 3V	19.37	17.93	47.24	52.74	8.8	2.7
	V_{DD2} = 10V, V_L = 4V	20.14	19.58	46.94	52.73	9.7	3.7
	V_{DD2} = 11V, V_L = 5V	20.66	19.06	47.35	52.63	10.7	4.9
	V_{DD2} = 12V, V_L = 6V	20.42	21.11	47.51	52.46	11.6	5.7

t_R: Output rise time (10% to 90%)

t_F: Output fall time (90% to 10%)

4-Channel Bipolar Clock Driver (EF1104-0)

PERFORMANCE PLOTS:

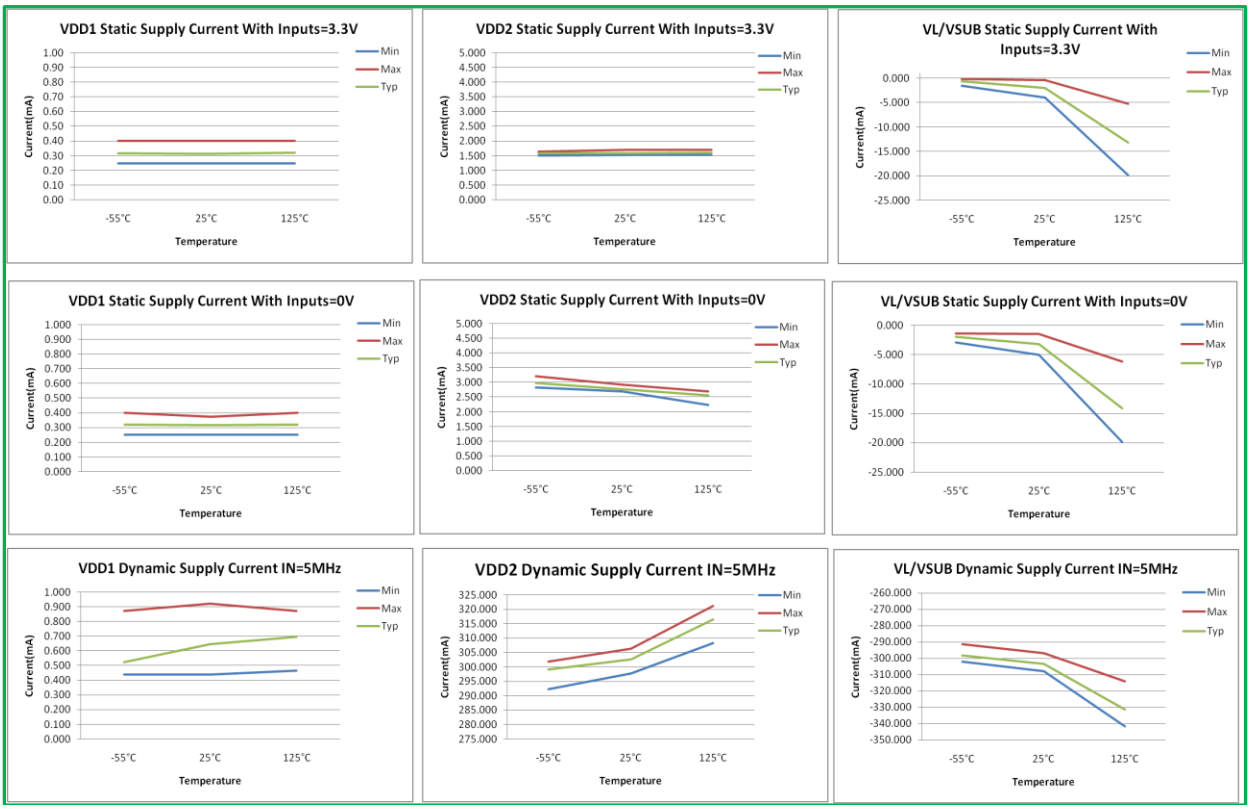


Figure-3: Power Supply Current Plots

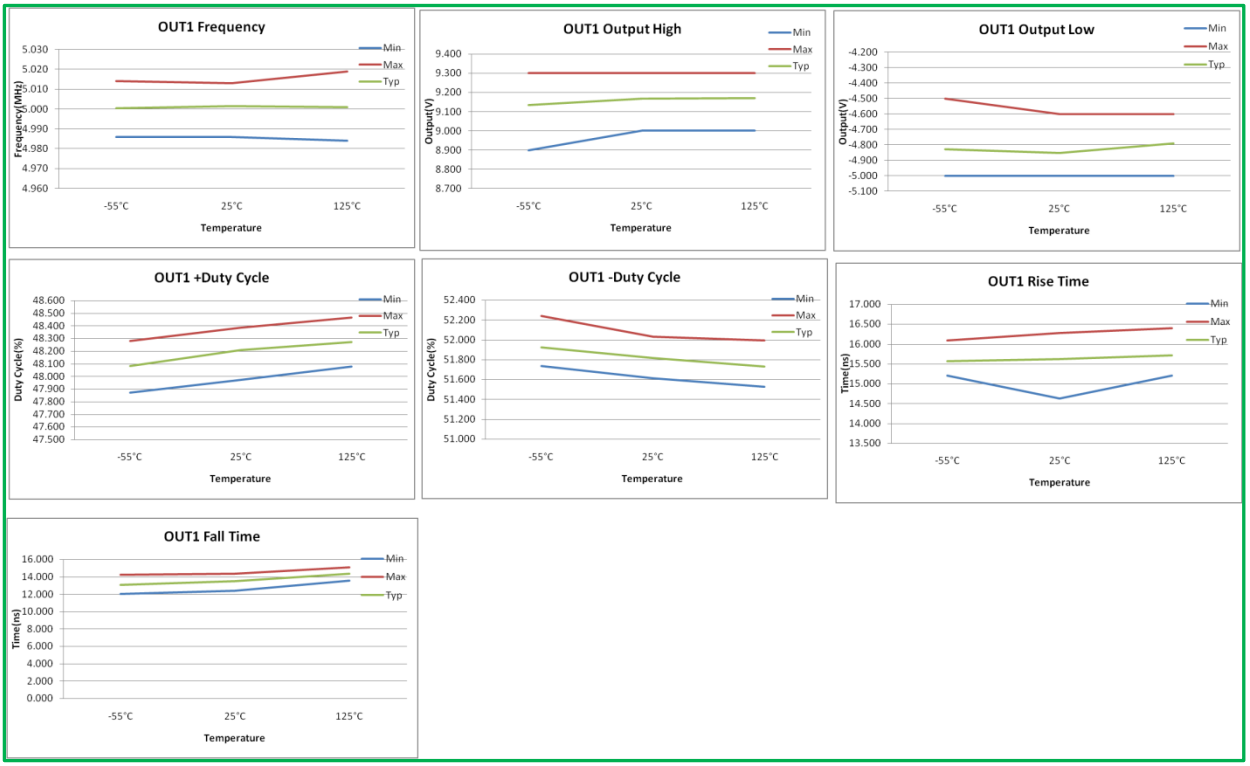


Figure-4: OUT1 AC Parameter Plots

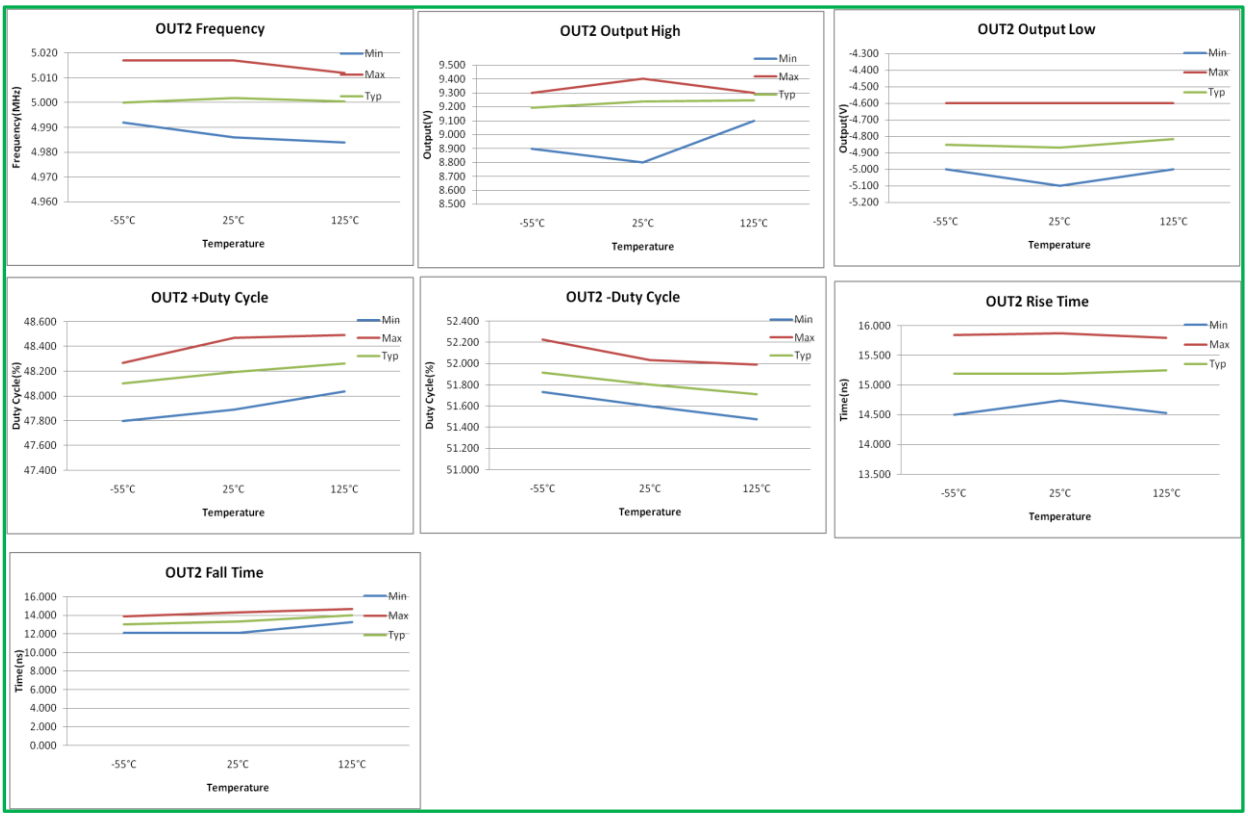


Figure-5: OUT2 AC Parameter Plots

4-Channel Bipolar Clock Driver (EF1104-0)

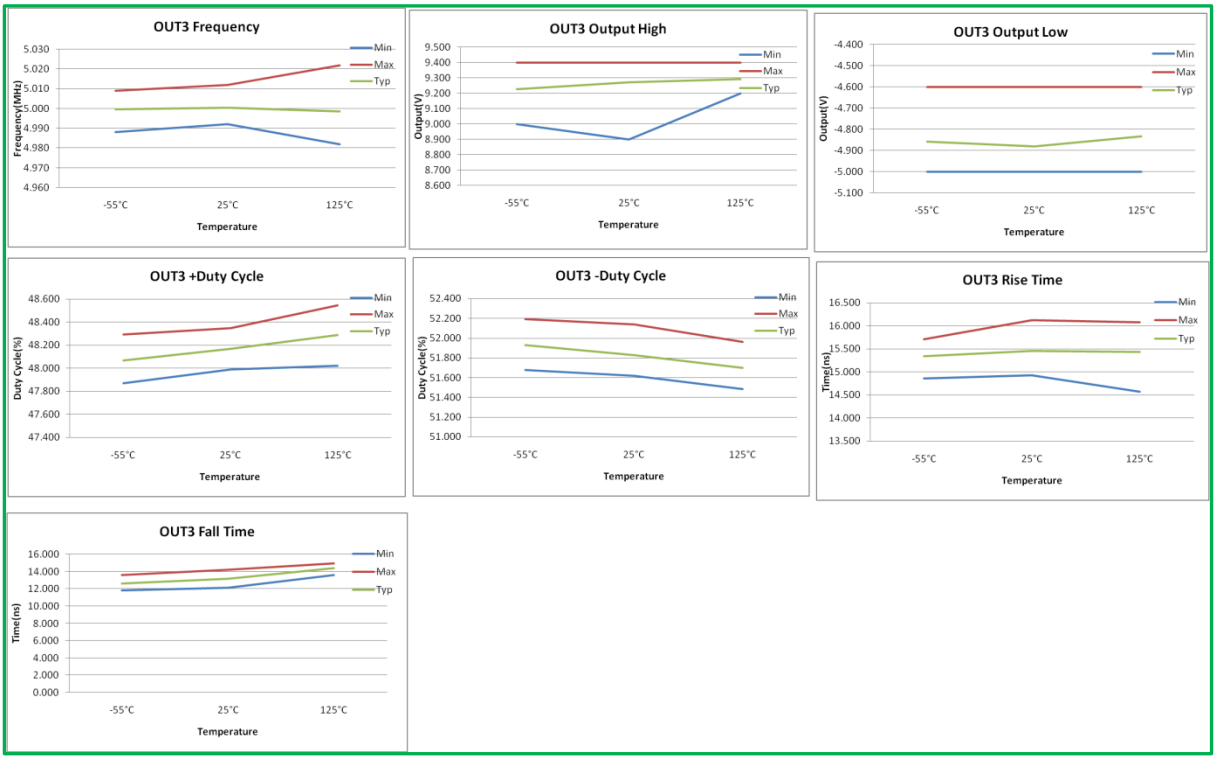


Figure-6: OUT3 AC Parameter Plots

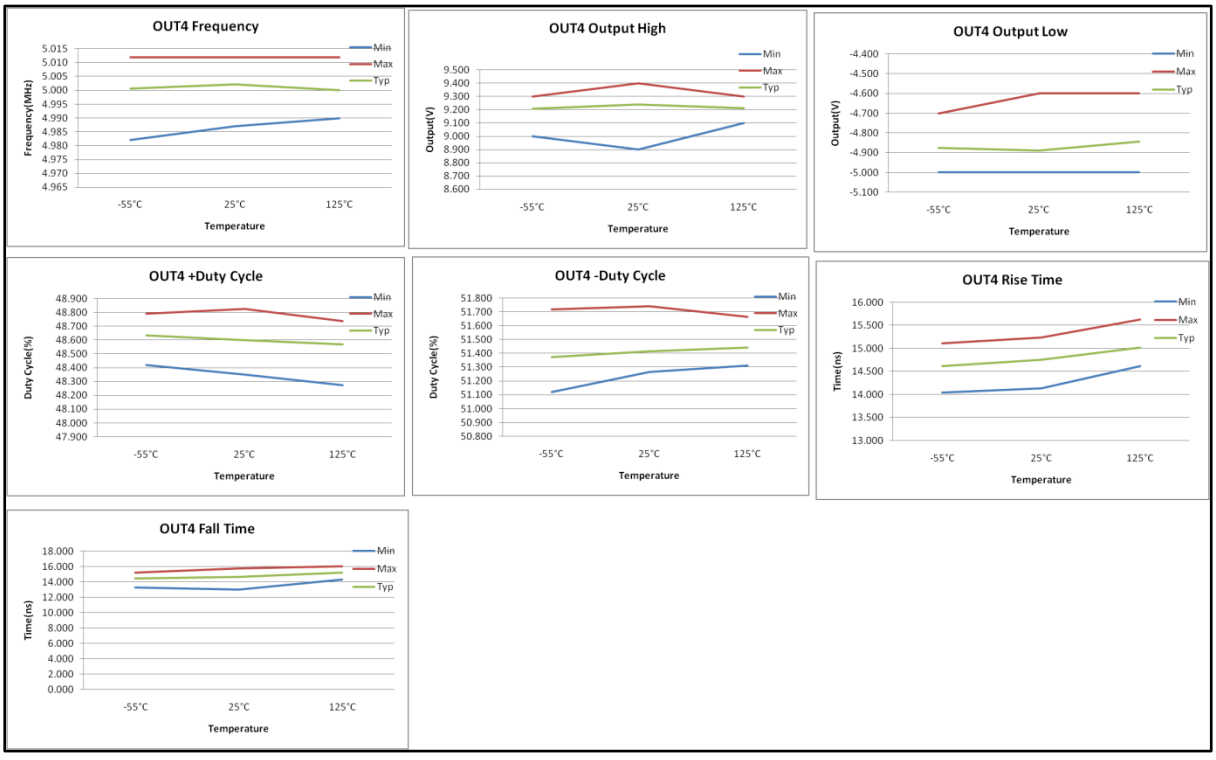


Figure-7: OUT4 AC Parameter Plots

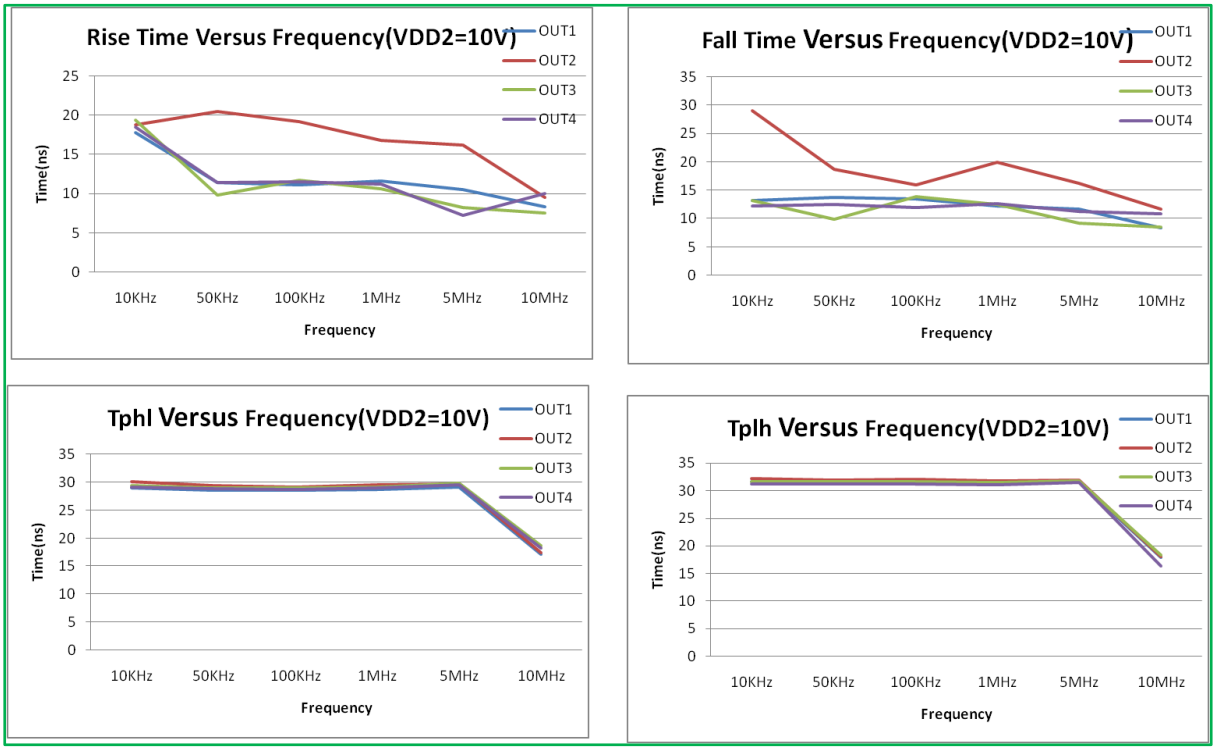


Figure-8: Rise Time/Fall Time/Delay Tphl/Delay Tplh versus Frequency at VDD2=10V
(Test conditions: V_{DD1} = 3.3V, V_{DD2} = 10V, V_L = V_{SUB} = 0V, GND = 0V, T_A = 25ºC
C_{LOAD}=850pF, Frequency=10KHz to 10MHz)

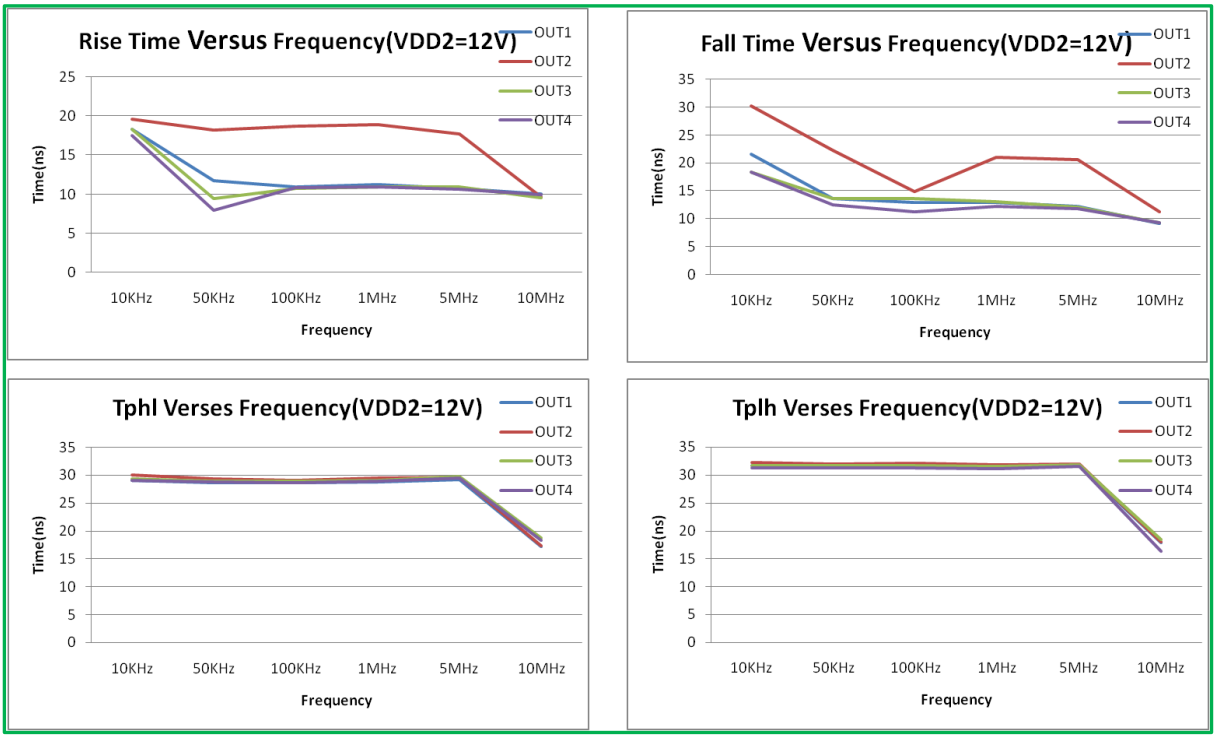


Figure-9: Rise Time/Fall Time/Tphl/Tplh versus Frequency at VDD2=12V
(Test conditions: V_{DD1} = 3.3V, V_{DD2} = 12V, V_L = V_{SUB} = 0V, GND = 0V, T_A = 25ºC
C_{LOAD}=850pF, Frequency=10 KHz to 10MHz)

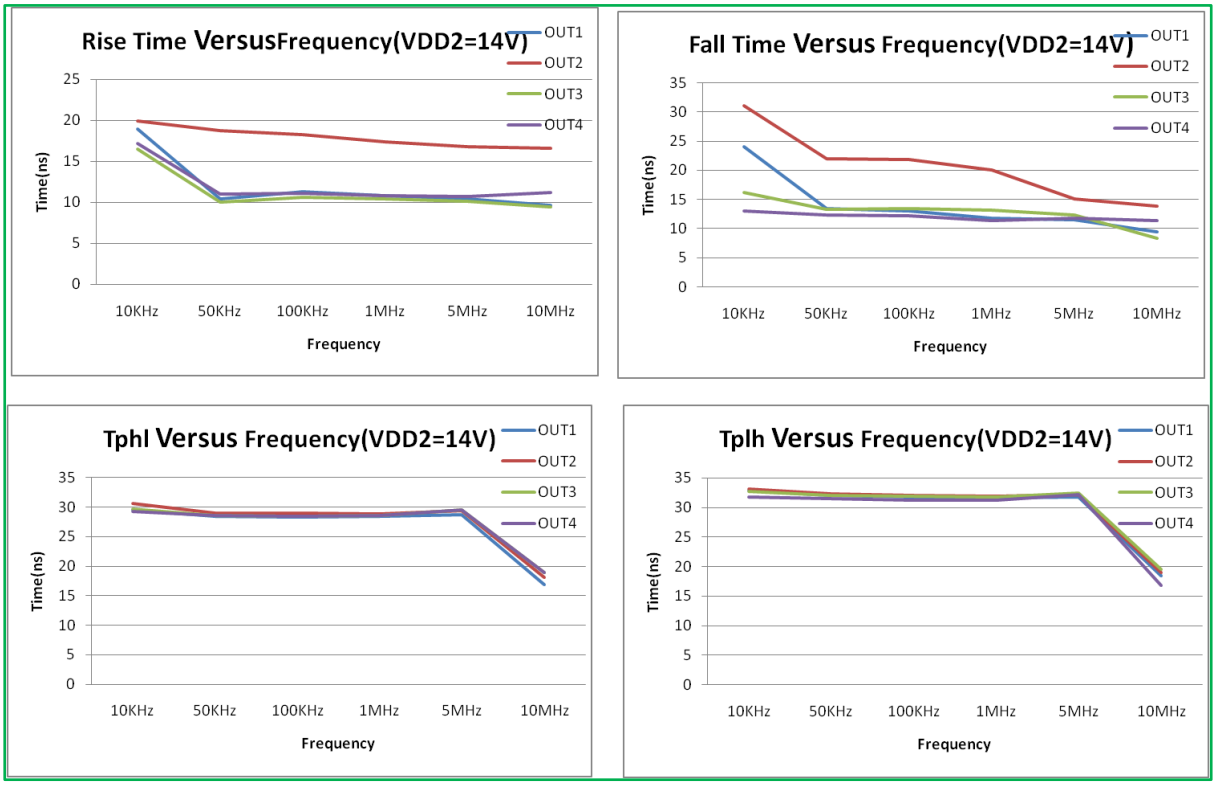


Figure-10: Rise Time/Fall Time/Tphl/Tplh versus Frequency at VDD2=14V
(Test conditions: V_{DD1} = 3.3V, V_{DD2} = 14V, V_L = V_{SUB} = 0V, GND = 0V, T_A = 25ºC
C_{LOAD}=850pF, Frequency=10KHz to 10MHz)

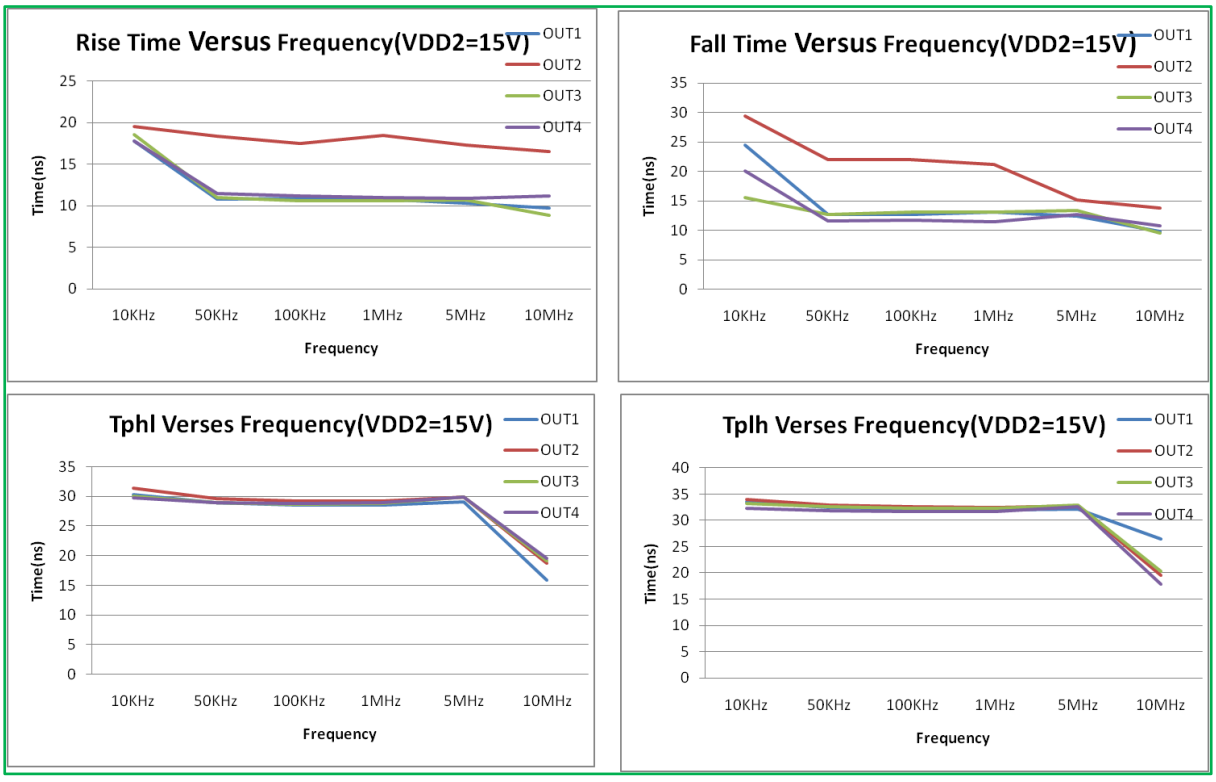


Figure-11: Rise Time/Fall Time/Tphl/Tplh versus Frequency at VDD2=15V
(Test conditions: V_{DD1} = 3.3V, V_{DD2} = 15V, V_L = V_{SUB} = 0V, GND = 0V, T_A = 25ºC
C_{LOAD}=850pF, Frequency=10KHz to 10MHz)

4-Channel Bipolar Clock Driver (EF1104-0)

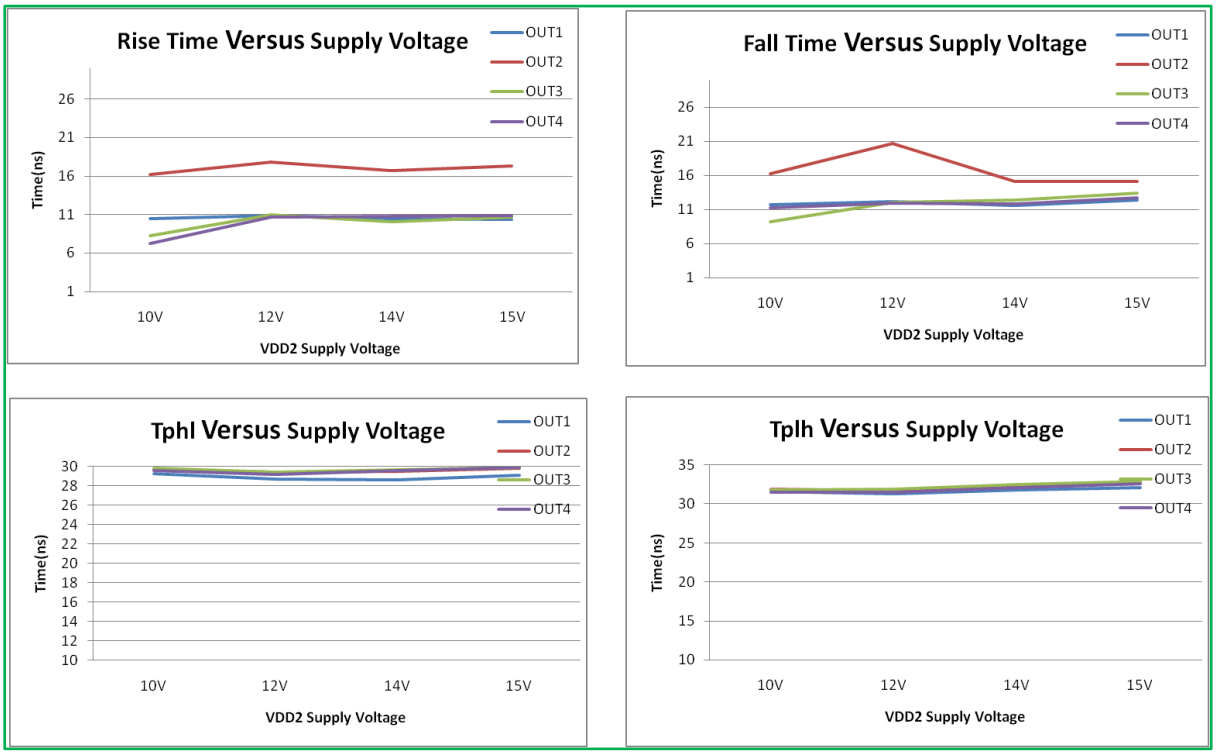


Figure-12: Rise Time/Fall Time/Tphl/Tplh versus Supply Voltage

(Test conditions: V_{DD1} = 3.3V, V_{DD2} = 10V to 15V, V_L = V_{SUB} = 0V, GND = 0V, T_A = 25ºC C_{LOAD}=850pF, Frequency=5MHz)

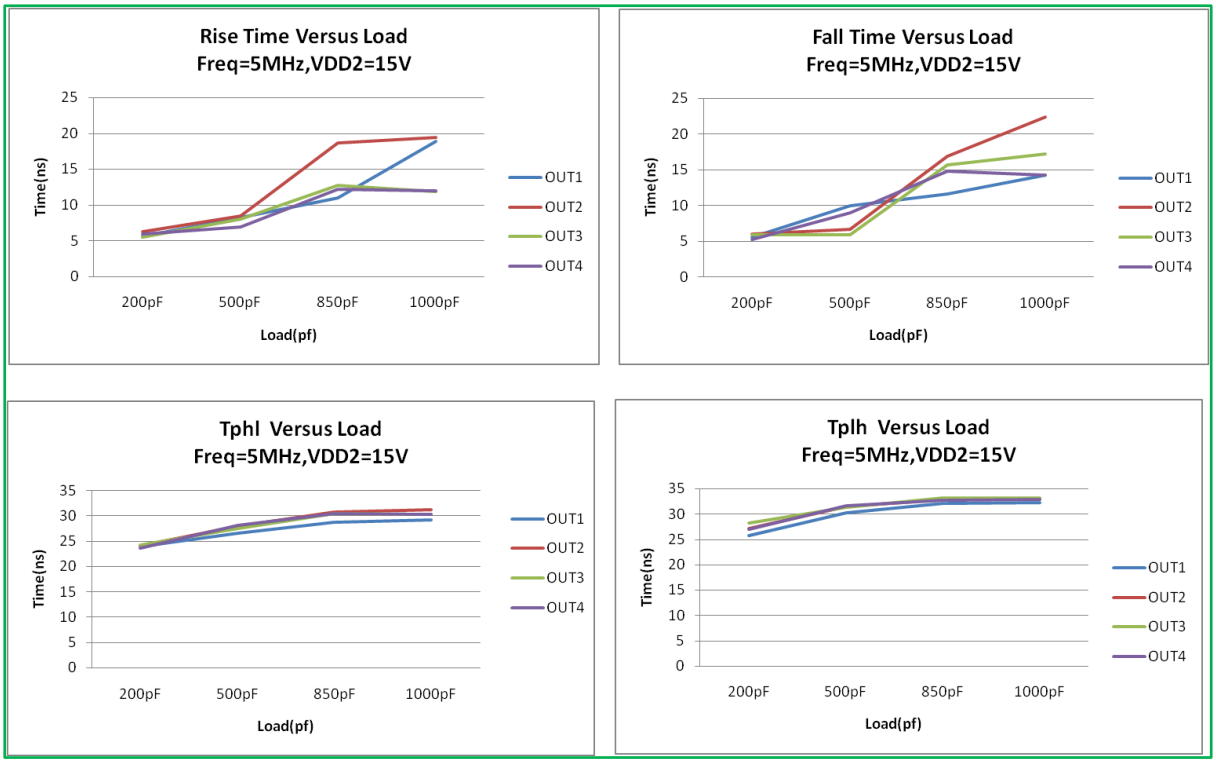


Figure-13: Rise Time/Fall Time/Tphl/Tplh versus Load

(Test conditions: V_{DD1} = 3.3V, V_{DD2} = 15V, V_L = V_{SUB} = 0V, GND = 0V, T_A = 25ºC C_{LOAD}=200pF to 1000pF, Frequency=5MHz)

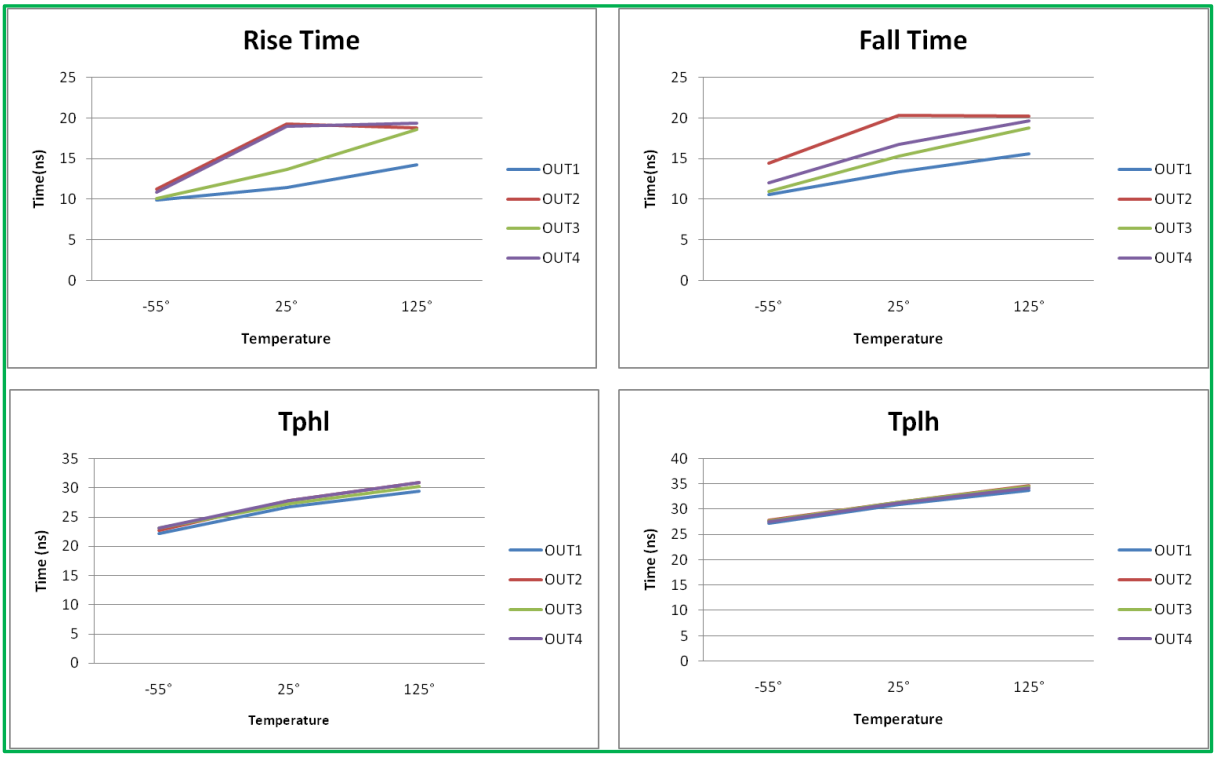


Figure-14: Rise Time/Fall Time/Tphl/Tplh versus Temperature
(Test conditions: V_{DD1} = 3.3V, V_{DD2} = 15V, V_L = V_{SUB} = 0V, GND = 0V, T_A = 25ºC
C_{LOAD}=850pF, Frequency=5MHz)

4-Channel Bipolar Clock Driver (EF1104-0)

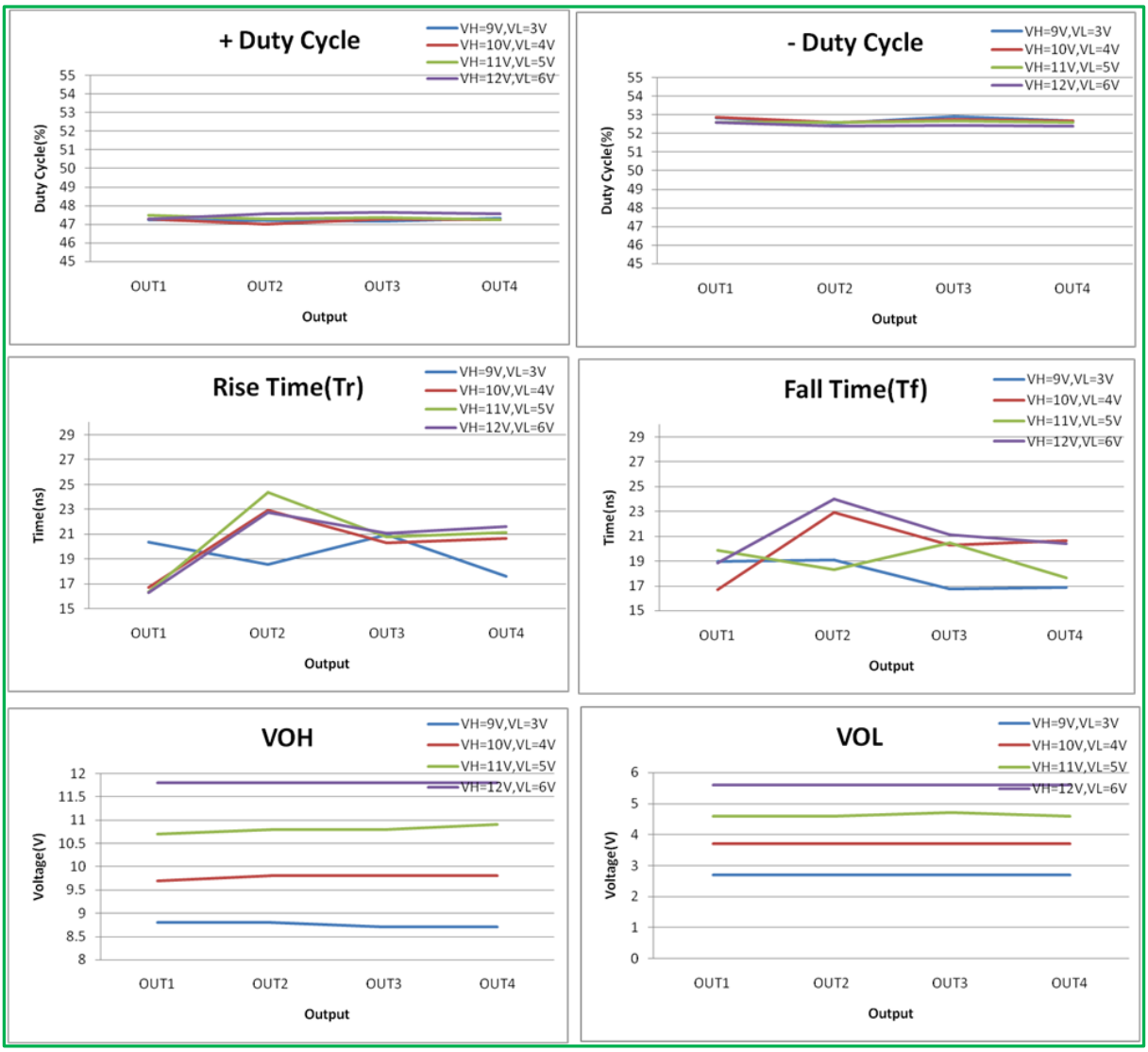


Figure-15: Device parameter for different positive VL voltages

(Test conditions: V_{DD1} = 3.3V, V_{DD2} = 9V to 12V, V_L = 3V to 6V, GND = 0V, VSUB = GND through 1kΩ resistor, T_A = 25ºC, C_{LOAD}=850pF, Frequency=5MHz)

4-Channel Bipolar Clock Driver (EF1104-0)

PACKAGE DRAWING (CERAMIC-LEAD-FLATPACK):

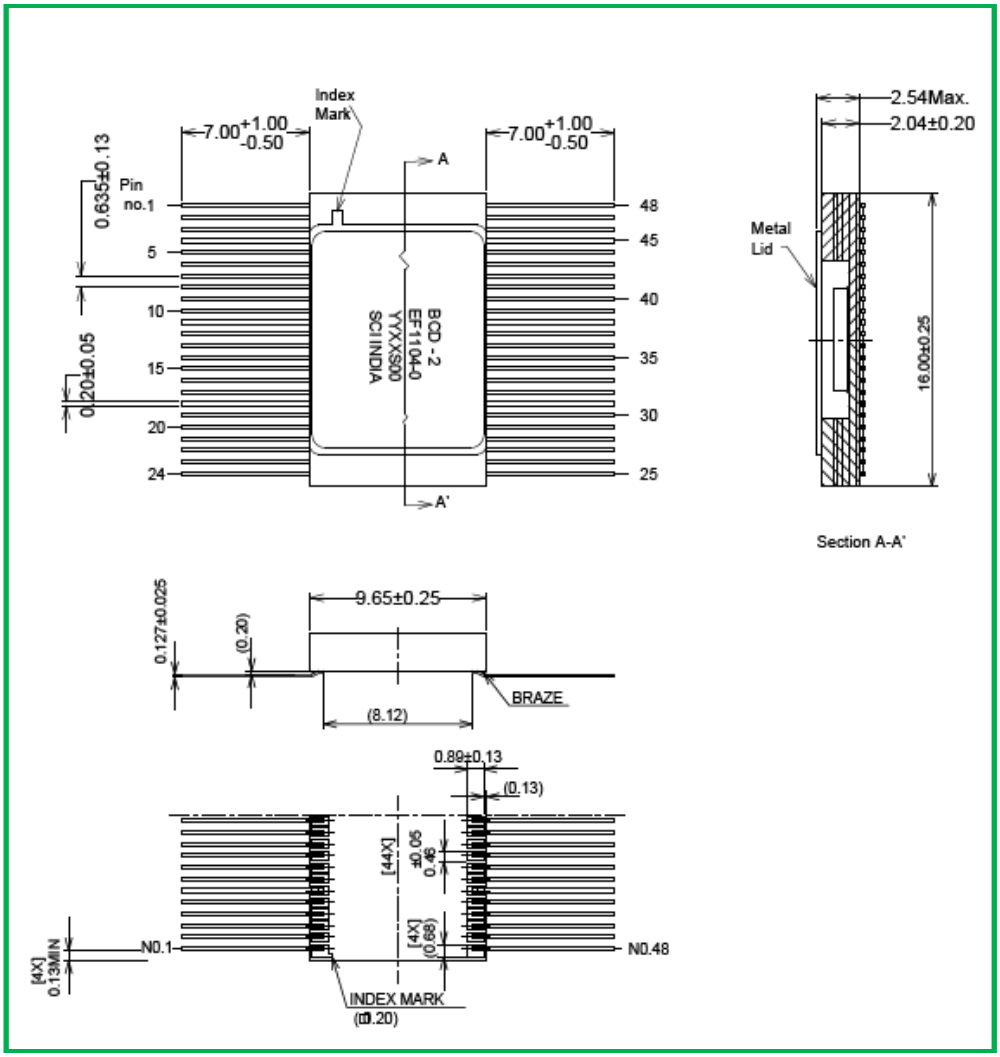


Figure-16: Package Device Drawing

NOTE: All linear dimensions are in inches (mm.)

4-Channel Bipolar Clock Driver (EF1104-0)

APPLICATION DIAGRAM:

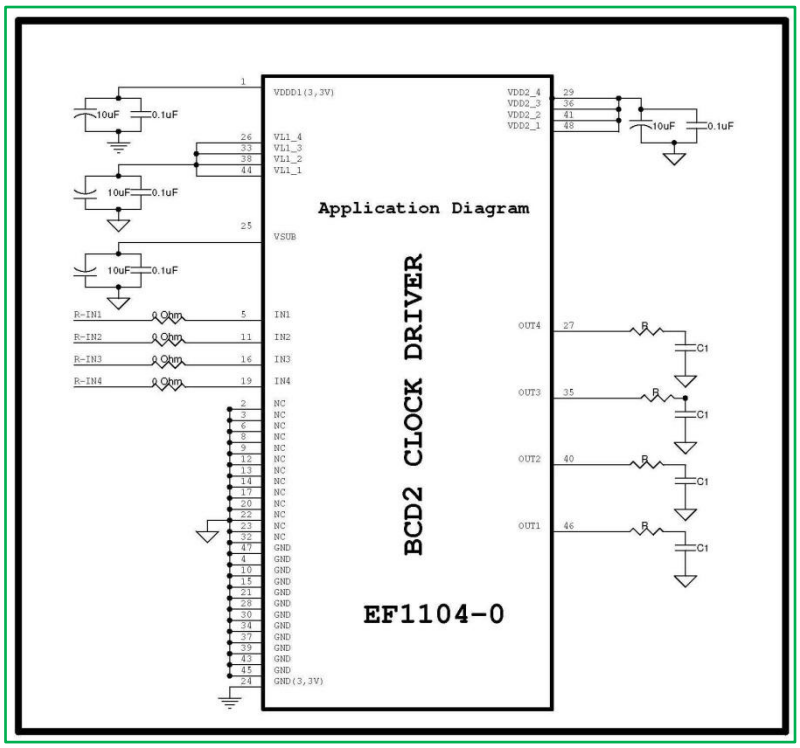


Figure-17: Typical Application Diagram

Note: R: in the rage of 10Ω to 50Ω depending upon frequency and Undershoot / Overshoot acceptable range.

POWER DISSIPATION CALCULATION

For reliable operation die temperature must be kept below Junction temperature (125°C). For a given application the power dissipation is calculated as:

$$P_D = (V_S * I_{DDS}) + \sum_{1}^{4} (C_{IN} * V_S^2 * f) + (C_{LOAD} * V^2_{OUT} * f)$$

P_D : Power Dissipation
V_S: Total power supply (from VH to VL)
V_{OUT}: Output Swing (VH - VL)
C_{LOAD} : Load capacitance
C_{IN}: Internal load capacitance
I_{DDS}: Quiescent supply current
f: Frequency

So $T_{JMAX} = T_{MAX} + \theta_{jc} * P_D$

T_{JMAX}: Maximum junction temperature (125°C)
T_{MAX}: Maximum ambient operating temperature
θ_{jc} :Thermal resistance, junction to ambient, of the application

4-Channel Bipolar Clock Driver (EF1104-0)

APPLICATION NOTE -1:

For reliable operation for VL> 0.5 volt requires minimum 1KΩ resistor to be mounted between V_{SUB} and Ground. The value of 1 KΩ ≤ Rs≤ 10 KΩ and may be optimized to minimize substrate current.

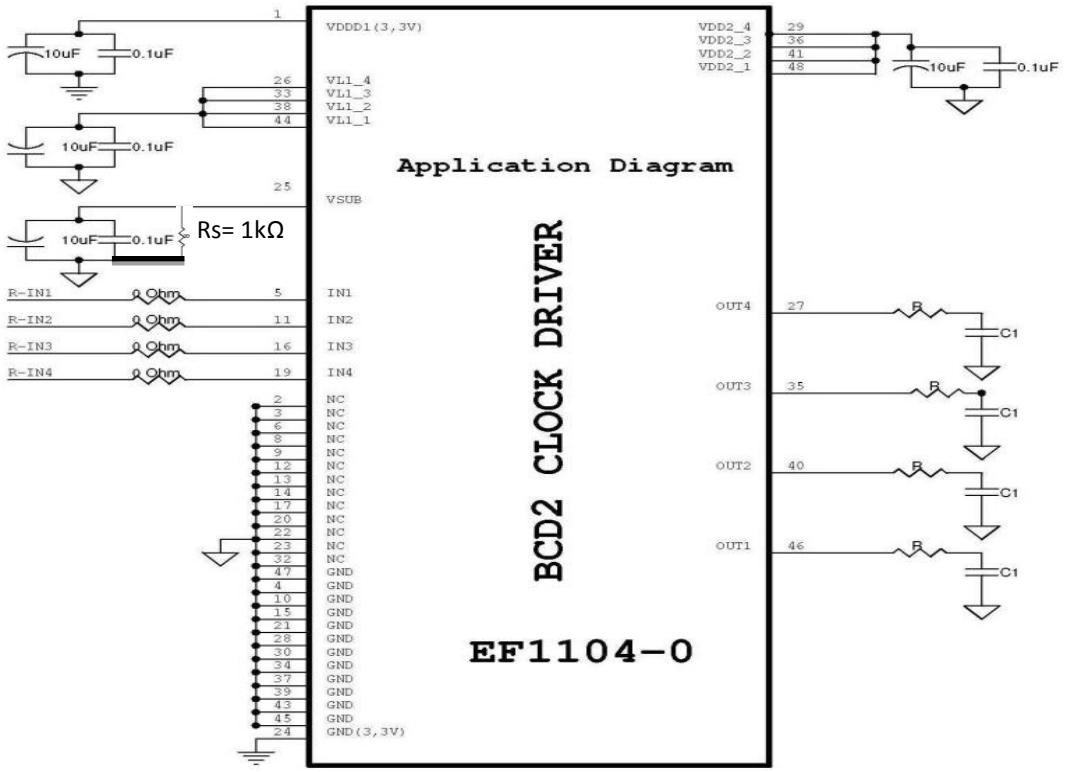
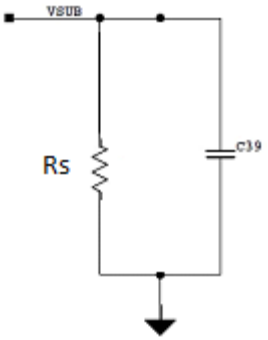


Figure-18: Application Diagram for VL > 0.5V



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