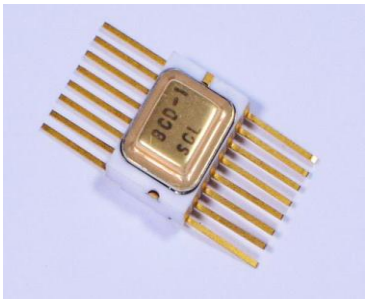
BCD-1 CLOCK DRIVER

EF1103-0

DATA SHEET



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FEATURES

- High voltage 0.35 um AMS CMOS Process (H35B4D3)
- Single channel input
- Input level shifters
- 5V ≥ VL ≥- 5V
- 9V ≤ VH ≤ 14V
- 20ns tr/tf at 850pF load
- 30 ns Tplh/Tphl delay
- 5 MHz operating frequency
- 3.3V power supply for VDD1
- Low power dissipation (0.7W at 5MHz with output load of 850pf)
- Hermetic sealed 16 pin Lead Flat package (SOP)
- Radiation Hardened (TID) up to 200Krad(Si)
- Single event effect (SEE) immune up to 50 MeV-cm2/mg
- Temperature range of -55°C to +125°C
- **θj_c: 7.12 °C/Watt**

PRODUCT DESCRIPTION

Designed on High voltage 0.35 um AMS CMOS Process (H35B4D3), The **EF1103-0** is a high-speed clock driver specifically designed and packaged in a hermetic sealed ceramic flat-16 lead (SOP) package for use in high speed CCD and time delay integration (TDI) detector clocks. The intended application of these devices is to drive high capacitive CCD loads of the order of ~850pF and fast rise / fall requirements

DEVICE SUMMARY:

Table-1: Device Summary

Reference	Package	pins	Lead Finish	Description
EF1103-0	Ceramic Flat pack	16	Gold	Flight Model

BLOCK LEVEL DIAGRAM:

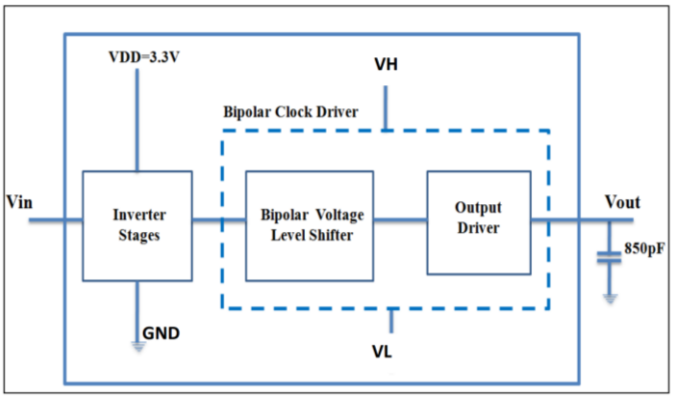

Figure-1: Block Level Diagram

DEVICE PIN DIAGRAM:

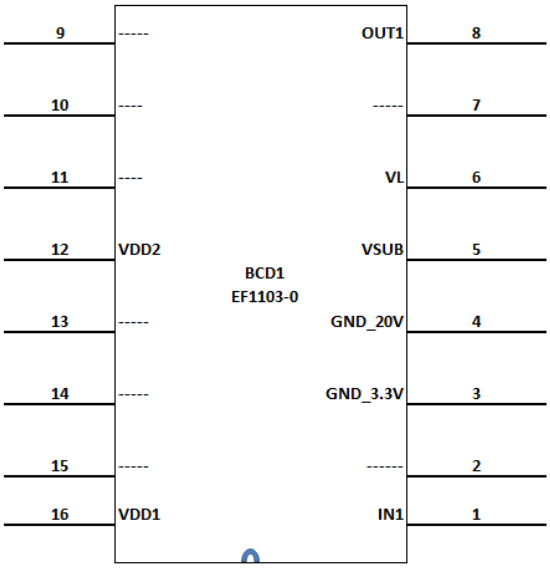

Figure-2: Device Pin Diagram

PIN CONFIGURATION:

Table-2: Pin Configuration

Pin No	Signal Name	Pin Type	Pin Description
1	IN1	DI	Input channel
2	---	NC	
3	GND (VDD1)	AGND	
4	GND (VDD2)	AGND	
5	VSUB	AP	Substrate supply
6	VL	AP	Driver Low Rail supply
7	---	*NC*	
8	*OUT1*	AO	Driver Output
9	---	*NC*	
10	---	NC	
11	---	NC	
12	VDD2	AP	Driver High Rail supply
13	----	*NC*	
14	----	*NC*	
15	----	*NC*	
16	VDD1	AP	Input Interface Buffer Supply (3.3V) to BCD

- Pin Type DI = Digital Input, AO = Analog Output, AP = Analog Power, AGND = Analog Ground
- De-coupling capacitors of 10uF and 0.1uF in parallel are recommend on Analog Power pins w.r.t ground pin

RECOMMENDED OPERATING CONDITIONS:

Table-3: Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD1} to GND	Supply Voltage (VDD1)	3.0	3.3	5.0	V
V_{DD2} to GND	Supply Voltage (VDD2)	5.0	9	14.0	V
V_L to GND	VL Low Voltage	-5	0	5	V
V_{SUB} to GND	VSUB Voltage	-5	-5	0	V
V_{IH}	High Level Input Voltage	2.0	3.3	5	V
V_{IL}	Low Level Input Voltage	0	0	0.8	V
T_A	Temperature range	-55	25	+125	ºC

ABSOLUTE MAXIMUM RATINGS (1):

Over operating free-air temperature range (unless otherwise noted),

Table-4: Absolute Maximum Rating

Parameter	Unit
Supply Voltage range **(V_{DD2} to V_{SUB})**	15 V
Supply Voltage range **(V_{DD1} to GND)**	6 V
Supply Voltage range **(V_L to V_{SUB})**	–0.3 V
T_{stg} , Storage temperature range	–65°C to 150°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DC ELECTRICAL SPECIFICATIONS:

Test condition: V_{DD1} = 3.3V, V_{DD2} = 9V, V_L = V_{SUB} = -5V, GND = 0V, T_A = -55ºC to 125ºC

Table-5: DC Electrical Characteristics

Symbol	Parameter	Test Conditions	Pin	Min.	Typ.	Max.	Unit
INPUT							
I_{IH}	Logic "1" Input Current	V_{IH}=9V	IN1		0.1	10	uA
I_{IL}	Logic "0" Input Current	V_{IL}=-5V			0.1	10	uA
OUTPUT							
V_{OH}	Output Voltage High		OUT1	8.5	9.1	9.5	V
V_{OL}	Output Voltage Low			–5.5	-4.8	-4.5	V
POWER SUPPLY							
I_{DD} (static)	I_{DDL} (Inputs at Low)	0V at all Inputs	VDD1		0.1	0.2	mA
			VDD2		0.1	0.2	
			VL	-10	-3.5		
			VSUB	-10	-3.2		
	I_{DDH} (Inputs at High)	3.3V at all Inputs	VDD1		0.1	0.2	mA
			VDD2		0.1	0.2	
			VL	-10	-3.6		
			VSUB	-10	-3.3		
I_{DD} (Dynamic)	I_{DD}, dynamic	0 to 3.3V square wave input with frequency of 5MHz , 50% duty cycle	VDD1		0.1	1	mA
			VDD2		82	125	
			VL	-125	-86		
			VSUB	-10	-6.5		

AC ELECTRICAL SPECIFICATIONS:

Test condition: V_{DD1} = 3.3V, V_{DD2} = 9V, V_L = V_{SUB} = -5V, GND = 0V, T_A = -55ºC to 125ºC

Table-6: AC Electrical Characteristics

Symbol	Parameter	Test Conditions	Typical	Units
$\mathbf{T_R}$	Output rise time (10% to 90%)	0 to 3.3V square wave input with frequency of 5MHz , 50% duty cycle, C_L=1000pF	19.5	ns
$\mathbf{T_F}$	Output fall time (90% to 10%)		20.1	ns
$\mathbf{t_{RF\Delta}}$	t_R, t_F Mismatch		0.6	ns
$\mathbf{t_{D+}}$	Turn-Off Delay Time		30.3	ns
$\mathbf{t_{D-}}$	Turn-On Delay Time		29.6	ns
$\mathbf{t_{DD}}$	t_{D-1} - t_{D-2} Mismatch		0.7	ns

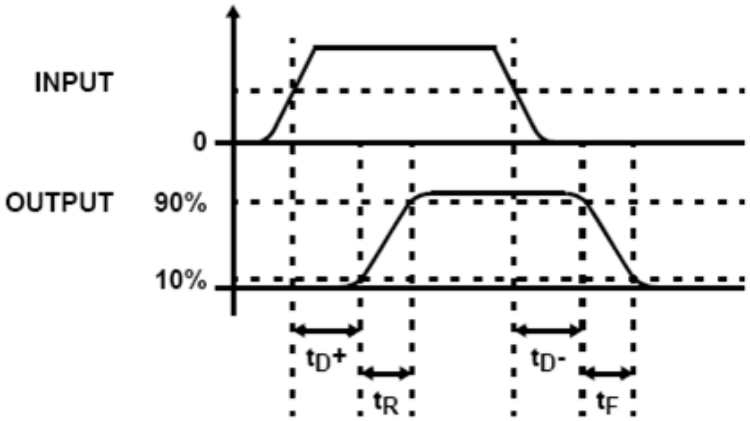

Figure-3: Timing Diagram

PERFORMANCE PLOTS:

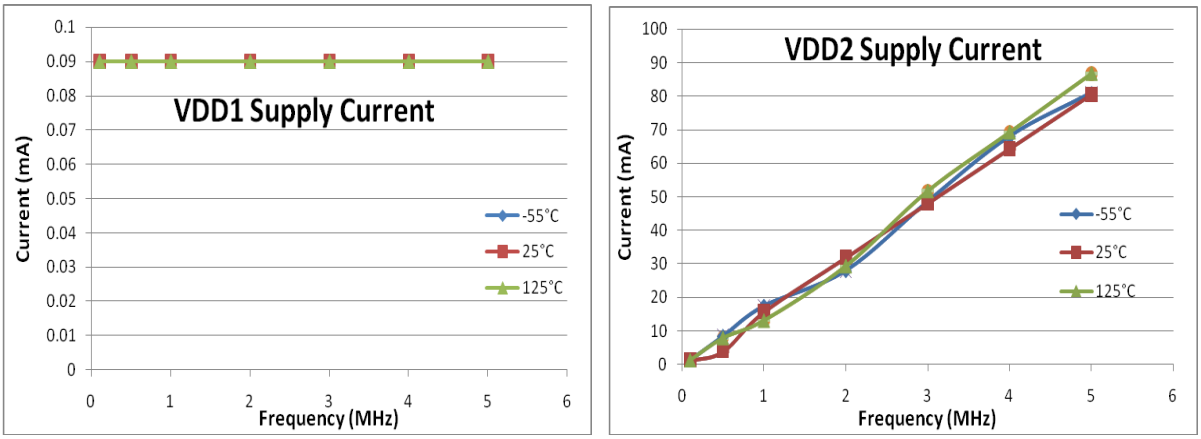

Figure-4: Dynamic VDD1 & VDD2 Power Supply Current

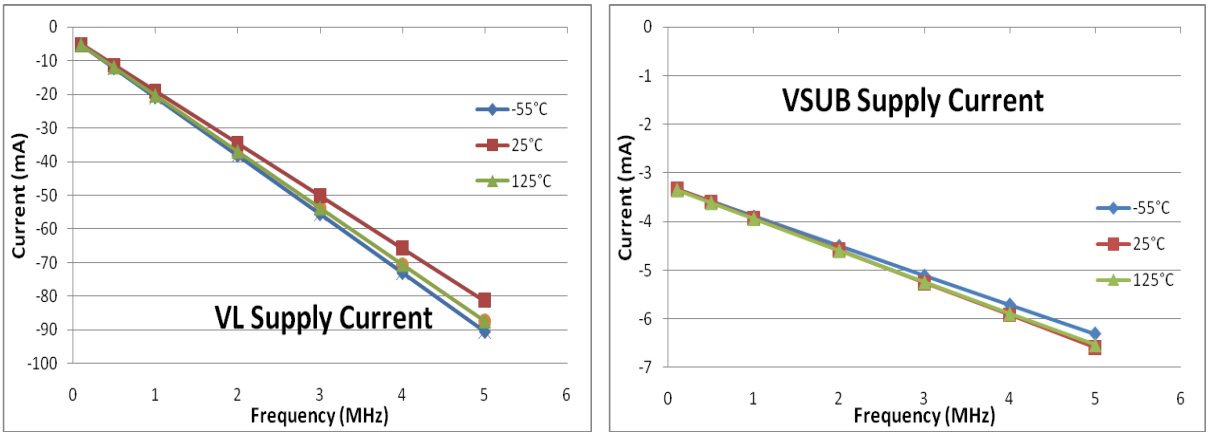

Figure-5: Dynamic VL & VSUB Power Supply Current

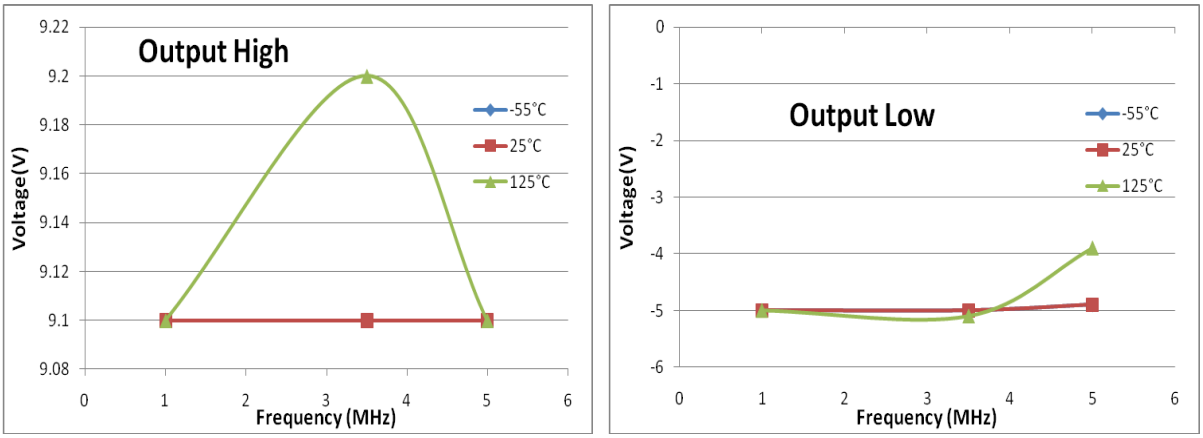

Figure-6: Output Voltage Levels

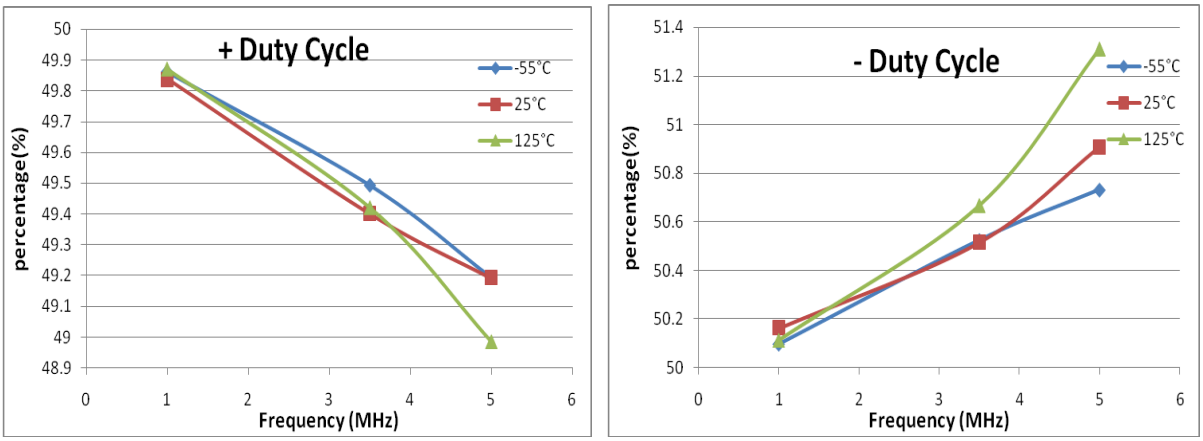

Figure-7: Output Duty Cycle

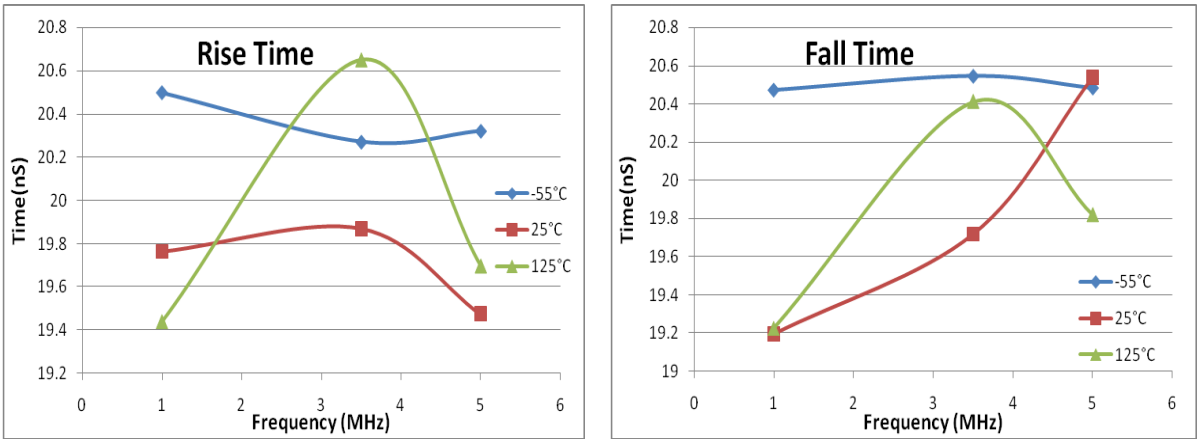

Figure-8: Output Rise/Fall Time

PACKAGE DRAWING (CERAMIC-LEAD-FLATPACK):

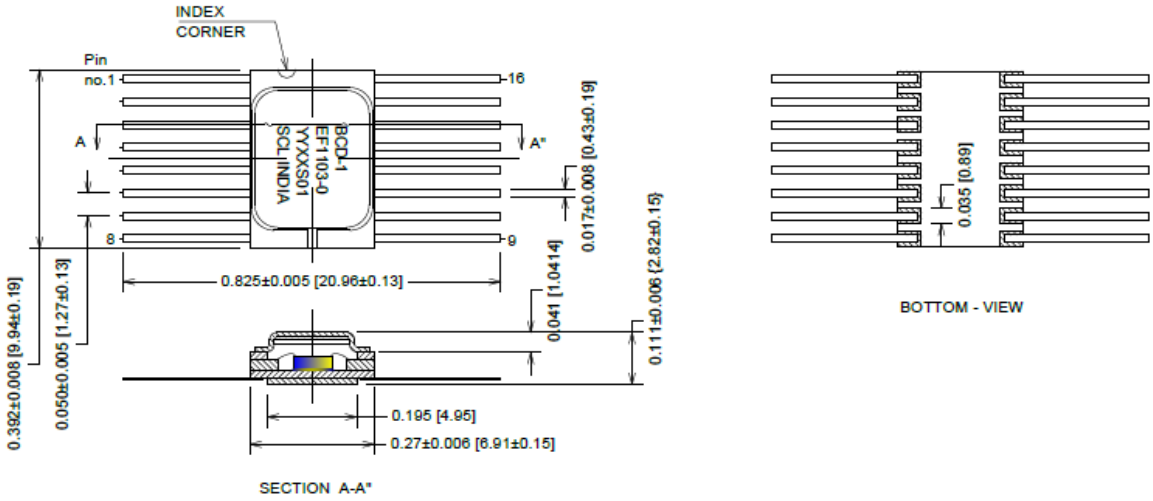

Figure-9: Package Device Drawing

NOTE: All linear dimensions are in inches (mm.)

APPLICATION DIAGRAM:

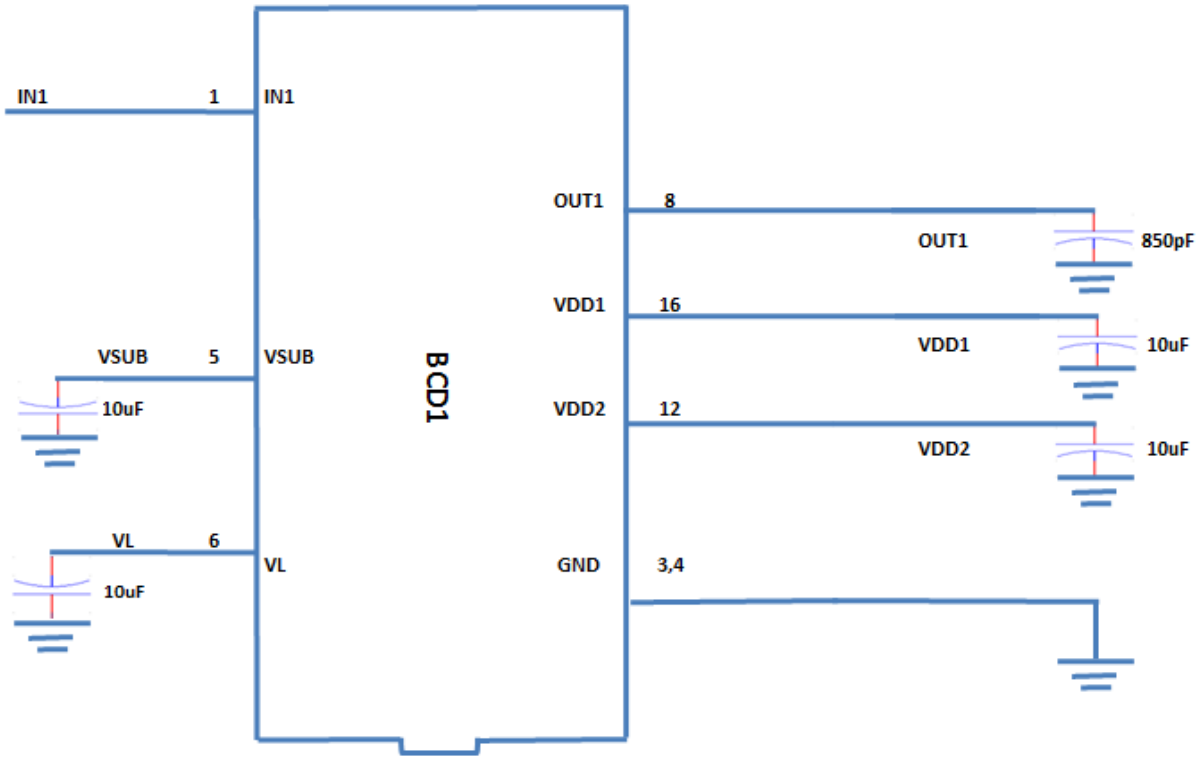

Figure-10: Application Diagram