# EF1008-0

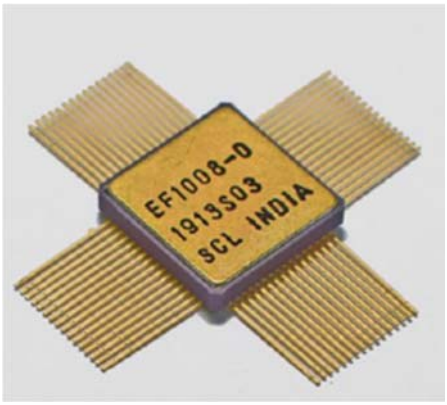
SCL-DEC 2019

PRELIMINARY DATASHEET

# Quad Core Charge to Voltage Amplifier (QCCVA)

## FEATURES:

- **Analog Supply Voltage is ±5V.**
- **Digital Supply is 3.3V.**
- **PGA: 1 to 32 in Binary Steps.**
- **Output DC level Adjustment: 0 V, 1.25 V, 1.65 V, 2.5 V.**
- **Operating Temperature: -55ºC to +125ºC.**
- **Low Power Dissipation.**
- **Packaged in 64 Pin CQFP package.**
- **AMS 0.18µ CMOS technology.**




## DESCRIPTION:

Charge Amplifier is a signal conditioner which conditions the signal from Vibration, Shock and Acoustic transducers. Quad Core programmable C-to-V Amplifier (EF1008-0) contains 4 cores of programmable C-to-V amplifier. Each of the cores can be programmed independently through input control signals. The user can select any of the gain and DC output value by applying the appropriate value at the control inputs.

Programmable C-to-V amplifier is targeted for vibration, acoustic and other measurements having charge as input. The device converts input charge to voltage. Charge to Voltage converter is followed by the Programmable Gain Amplifier (PGA) which provides 6 programmable gains from 1 to 32 binary steps. The DC level of the output is shifted upto four different values. The user can set the values of PGA and DC output level using input control signals. The operating temperature of the chip is -55ºC to +125ºC.

## BLOCKDIAGRAM:

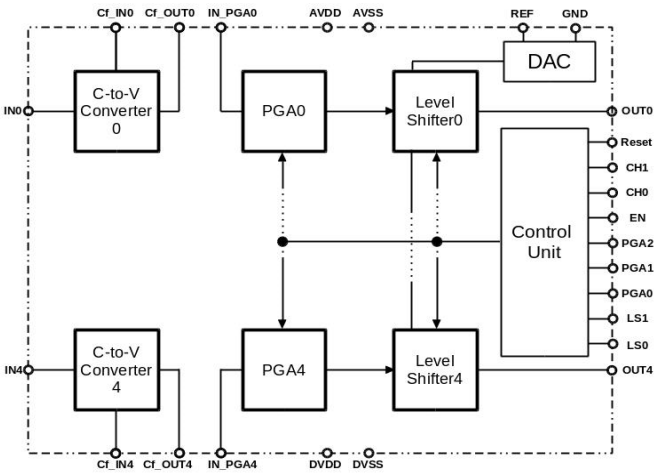



Figure1: Device block Diagram of EF1008-0

**PIN CONFIGURATION:**

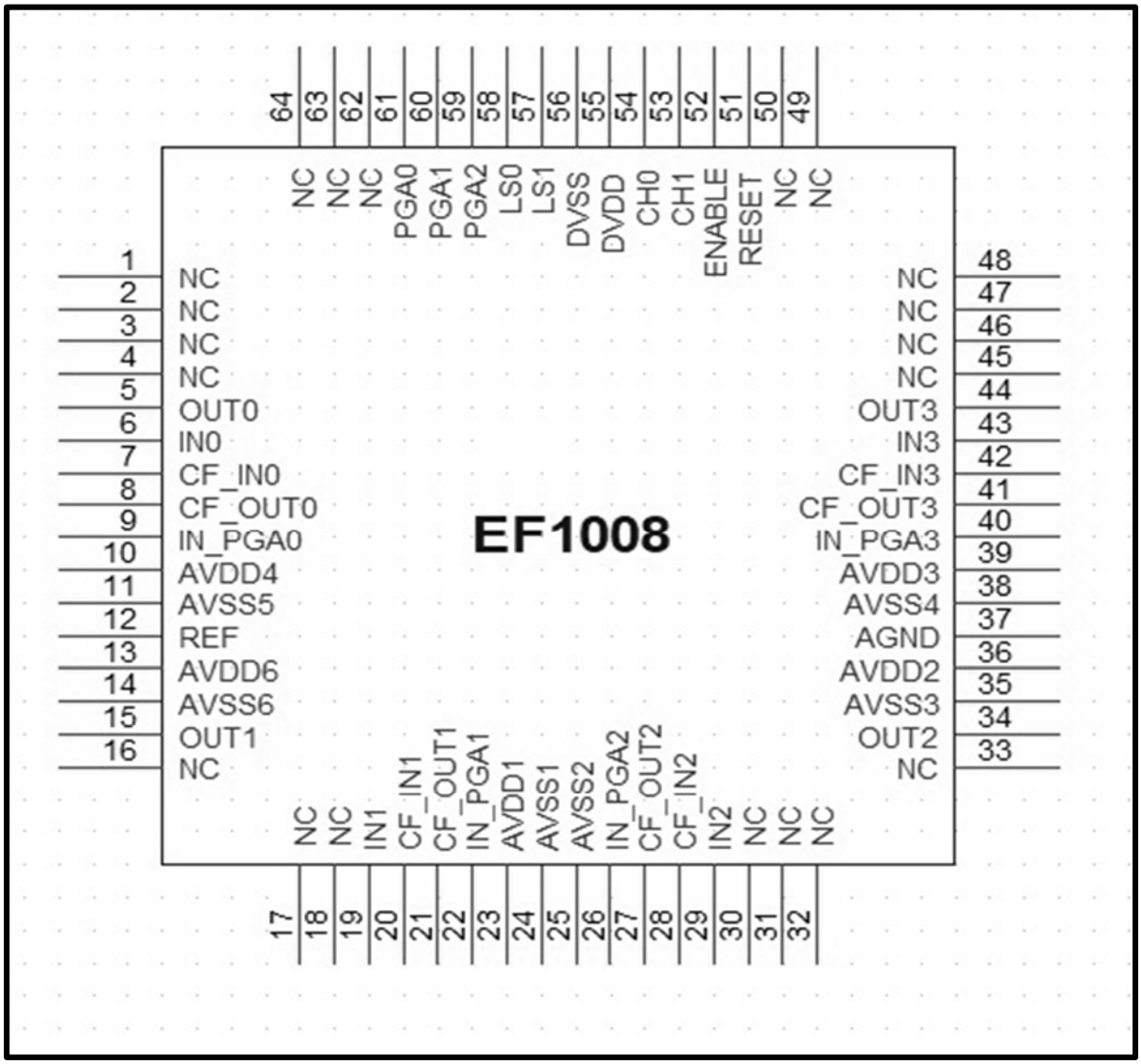



Figure2: Device Pin Diagram

**PIN DESCRIPTION:**

| Pin No | Name | Description |
|---|---|---|
| 1 | AGND | Analog Ground 0V. A current of $V_{REF}$/12K will flow into the pin |
| 2 | DVDD | Digital Supply (3.3V) |
| 3 | DGND | Digital Ground (0 V) |
| 4 | IN0 | Input Pin for Core0 |
| 5 | IN1 | Input Pin for Core1 |
| 6 | IN2 | Input Pin for Core2 |
| 7 | IN3 | Input Pin for Core3 |
| 8 | CF_IN0 | A capacitor of value 1nF to 10nF will be connected between CF_IN0 and CF_OUT0(Core 0) |
| 9 | CF_OUT0 | |
| 10 | CF_IN1 | A capacitor of value 1nF to 10nF will be connected between CF_IN0 and CF_OUT0(Core 1) |
| 11 | CF_OUT1 | |
| 12 | CF_IN2 | A capacitor of value 1nF to 10nF will be connected between CF_IN0 and CF_OUT0(Core 2) |
| 13 | CF_OUT2 | |
| 14 | CF_IN3 | A capacitor of value 1nF to 10nF will be connected between CF_IN0 and CF_OUT0(Core 3) |
| 15 | CF_OUT3 | |
| 16 | IN_PGA0 | CF_OUT0 will be connected to the IN_PGA0 through a decoupling capacitor |
| 17 | IN_PGA1 | CF_OUT1 will be connected to the IN_PGA1 through a decoupling capacitor |
| 18 | IN_PGA2 | CF_OUT2 will be connected to the IN_PGA2 through a decoupling capacitor |
| 19 | IN_PGA3 | CF_OUT0 will be connected to the IN_PGA3 through a decoupling capacitor |
| 20 | OUT0 | Output (max driving capability: 20pF Capacitor): Core0 |
| 21 | OUT1 | Output (max driving capability: 20pF Capacitor): Core1 |
| 22 | OUT2 | Output (max driving capability: 20pF Capacitor): Core2 |
| 23 | OUT3 | Output (max driving capability: 20pF Capacitor): Core3 |
| 24 | REF | Ref Voltage of value 2.5V. A current of $V_{REF}$/12K will flow from this pin |
| 25 | AVSS | Negative Supply (-5V) |
| 26 | AVDD | Positive supply (5V) |
| 27 | LS0 | Control Input for DC Level Shift of output (0 to 3.3V) |
| 28 | LS1 | Control Input for DC Level Shift of output (0 to 3.3V) |
| 29 | PGA0 | Control Input for PGA (0 to 3.3V) |
| 30 | PGA1 | Control Input for PGA (0 to 3.3V) |
| 31 | PGA2 | Control Input for PGA (0 to 3.3V) |
| 32 | RESET | Control Input for Resetting the chip (0 to 3.3V) |
| 33 | CH0 | Control Input for selection for core (0 to 3.3V) |
| 34 | CH1 | Control Input for selection for core (0 to 3.3V) |
| 35 | ENABLE | Control Input for switching of transparent and latch mode(0 to 3.3V) |

Table1: Pin Description of EF1008-0

***Note**: User should set $C_{IN}$= $C_F$= 1nF and $R_F$= 50 MΩ*

**PROGRAMMING EF1008:**

User can set any of the PGA gain and any output DC value by selecting any of the channels and by applying appropriate input control signals (PGA, LS & ENABLE). There are two modes of operation in EF1008. They are known as Transparent Mode and Latched Mode. Any of the modes can be selected by applying appropriate signal at the ENABLE pin.

**TRANSPARENT MODE:**

This mode will be selected when ENABLE = 0. In this mode, the device will directly respond to the change in the values of the control signals (PGA & LS).

**LATCHED MODE:**

This mode will be selected when ENABLE = 1.In this mode, the PGA and DC level values set at a particular channel will be latched.

- Set the appropriate value at the PGA2:PGA0 and LS1:LS0.
- Set ENABLE = 0, so that the device will be in the transparent mode.
- During transparent mode the PGA and DC output level of the selected core will be set. Set ENABLE = 0 to latch the set values of PGA and Output DC level.
- Now select another core and follow the above steps.

The Procedure for setting the different values of PGA and DC output level in various channels is given as follows:

- Select a particular core by applying appropriate value at CH1:CH0.

User has to refer to the following timing diagram for configuring the IC in Transparent Mode or Latched Mode.

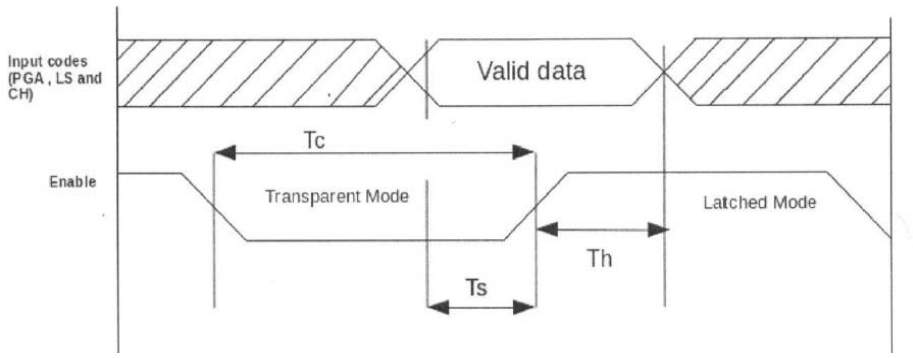



Figure3: The timing diagram for setting PGA and DC output level values

| SPEC | DESCRIPTION | MIN | UNIT |
|---|---|---|---|
| $T_c$ | Minimum Clock Cycle | 1 | us |
| $T_s$ | Data Setup Time | 100 | ns |
| $T_h$ | Data Hold Time | 100 | ns |

**Table 2 Timing Specification**

## DC ELECTRICAL CHARACTERISTICS:

All Specifications are at AVDD = 5 V, AVSS = -5V, DVDD =3.3V, $V_{REF}$= 2.5V, $C_{IN}$=$C_F$=1nF, $R_F$=50 MΩ and $T_A$=+25°C, unless otherwise specified.

| Parameter | Description | Test Conditions | EF1008-0 | | | |
|---|---|---|---|---|---|---|
| | | | Min. | Typ | Max. | Unit |
| Continuity Test | ESD Positive Diode | Force Current : 100uA | 0.3 | 0.45 | 0.9 | V |
| | ESD Negative Diode | Sink Current : -100uA | -0.9 | -0.37 | -0.3 | V |
| Leakage Current for digital Pins | $I_{IL}$ | Input Pin at 0 V | -1 | 0.002 | 1 | µA |
| | $I_{IH}$ | Input Pin at 3.3 V | -1 | 0.01 | 1 | µA |
| Leakage Current for analog Pins | $I_{IL}$ | Input Pin at 0 V | -1 | 0.002 | 1 | µA |
| | $I_{IH}$ : Pins INO-IN3, CF_IN0-CF IN3 | Input Pin at 3.3 V | -1 | 0.01 | 1 | µA |
| | $I_{IH}$ : Pins IN_PGA0-IN_PG3 | | - | 36 | 40 | mA |
| Static $I_{DD}$ | Static $I_{AVDD}$ | All Input Pins at 0V | | 35.5 | 50 | mA |
| | Static $I_{DVDD}$ | All Input Pins at 0V | | 10 | 1000 | µA |
| | Static $I_{AVSS}$ | All Input Pins at 0V | -50 | -35.6 | | mA |
| | Static $I_{AVDD}$ | All Input Pins at 3.3V | | 35.5 | 50 | mA |
| | Static $I_{DVDD}$ | All Input Pins at 3.3V | | 10 | 1000 | µA |
| | Static $I_{AVSS}$ | All Input Pins at 3.3V | -50 | -35.6 | | mA |

Table3: DC Electrical characteristics of EF1008-0

## AC ELECTRICAL CHARACTERISTICS:

All Specifications are at AVDD = 5V, AVSS = -5V, DVDD =3.3V, $V_{REF}$ = 2.5V, $C_{IN}$=$C_F$=1nF, $R_F$=50 MΩ, $V_{IN}$ = 0 to FSI $V_{RMS}$ in 10 steps .i.e. 0.17677V to 1.767 V. Step Size: 0.17677 V and $T_A$=+25°C, unless otherwise specified.

| Parameter | Description | Test Conditions | EF1008-0 | | | |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | Unit |
| **Calibration** | | | | | | |
| Gain (Scale Factor) | SF | $F_{in}$ = 110Hz , PGA=1 | | | 1.75 | % |
| | | $F_{in}$ = 1KHz , PGA=1 | | | | |
| | | $F_{in}$ = 10 KHz, PGA=1 | | | | |
| Non-Linearity | Best Fit Nonlinearity (NL) | $F_{in}$ = 110Hz, PGA=1 | | 0.05 | | % FSO |
| | | $F_{in}$ = 1KHz , PGA=1 | | 0.05 | | |
| | | $F_{in}$ = 10 KHz, PGA=1 | | 0.05 | | |
| **Frequency Response** | | | | | | |
| Frequency Response | $F_C$ Lower | Lower Cutoff frequency | 1 | 4 | 5 | Hz |
| | $F_C$ Upper | Upper Cutoff Frequency | 125 | 130 | 140 | KHz |
| | | Roll off | 0 | 3.96 | 5 | dB |
| | | Pass band Error | 0 | 1.55 | 3 | % |

Table4: AC Electrical Characteristics of EF1008-0

## FREQUENCY RESPONSE

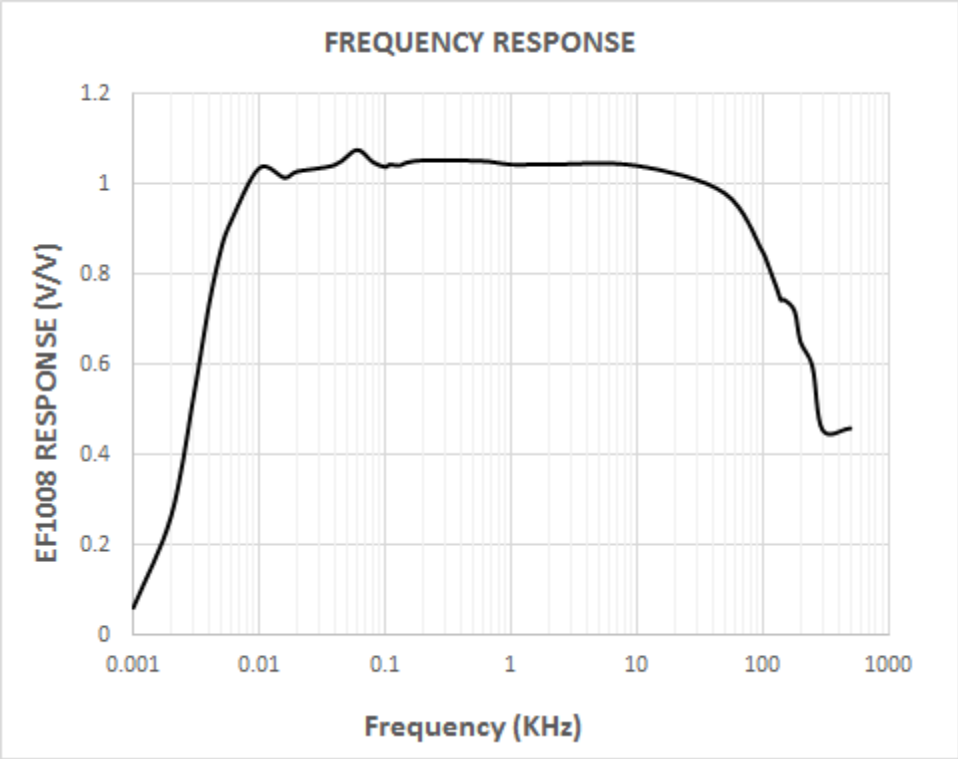



Figure4: Frequency Response

## RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| AVDD | Supply voltage AVDD | 4.5 | 5 | 5.5 | V |
| AVSS | Supply voltage AVSS | -5.5 | -5 | -4.5 | V |
| $V_{IH}$ | High level input voltage | 2.4 | - | - | V |
| $V_{IL}$ | Low level input voltage | - | - | 0.8 | V |
| $T_A$ | Ambient temperature range | -55 | - | +125 | ºC |

Table5: Recommended Operating Conditions

## OVERVIEW

### Charge to voltage converter

Charge amplifiers are usually constructed using an operational amplifier or other high gain semiconductor circuit with a negative feedback capacitor. The input current is offset by a negative feedback current flowing in the capacitor, which is generated by an increase in output voltage of the amplifier. The output voltage is therefore dependent on the value of input current it has to offset and the inverse of the value of the feedback capacitor. When the capacitance is connected to the inverting input of an Op-amp, this charge flows into the feedback capacitor. The resultant change in charge on feedback capacitor generates on output voltage.

$V_O = Q/C_F$ [Eq-1]

Therefore, gain of the circuit depends on the value of the feedback capacitor $C_F$. The resistor $R_F$ is required to provide the DC path for an Op amp. $R_F$ is inserted in parallel with $C_F$ which limits the DC gain of the circuit to a finite value.

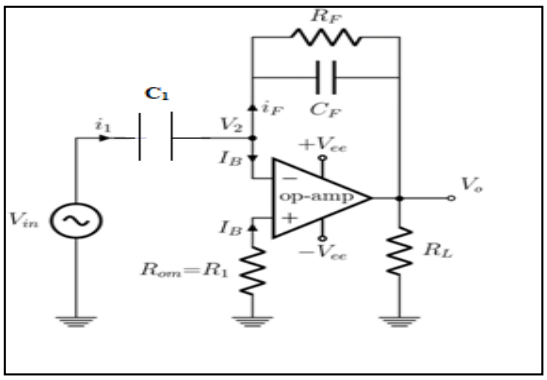



Figure5: Block Diagram of Charge Amplifier

There are four C-2-V Converter blocks in EF1008. This is the primary block which converts charge into voltage with gain of 1/Cf. A feedback Capacitor $C_F$ has to be connected externally between CF_IN and CF_OUT pins of the device. Value of the $C_F$ can vary between 1nf and 10nf.

Core Selection Control Settings:

| Sr. No | CH1: CH0 | Selected Core |
|---|---|---|
| 1 | 00 | Core 0 |
| 2 | 01 | Core 1 |
| 3 | 10 | Core 2 |
| 4 | 11 | Core 3 |

Table 6.Core Selection Control Settings

There are separate PGAs blocks for each C-2-V block in EF1008.The output of the charge to voltage converter goes into PGA through decoupling capacitor. This decoupling capacitor should be connected between CF_OUT and IN_PGA pins. Decoupling Capacitor prevents the transfer of charge from one circuit to another. PGA has 6 different gains from 1 to 32 in binary steps. These gains can be programmed by PGAs logic inputs (PGA2, PGA1 and PGA0). 3.3V corresponds to logic HIGH and 0V corresponds to logic LOW for these inputs.

PGA Control Settings:

| Sr. No | PGA2: PGA0 | Gain |
|---|---|---|
| 1 | 000 | 1 |
| 2 | 001 | 2 |
| 3 | 010 | 4 |
| 4 | 011 | 8 |
| 5 | 100 | 16 |
| 6 | 101 | 32 |

Table7: PGA Control Settings

### Level Shifter

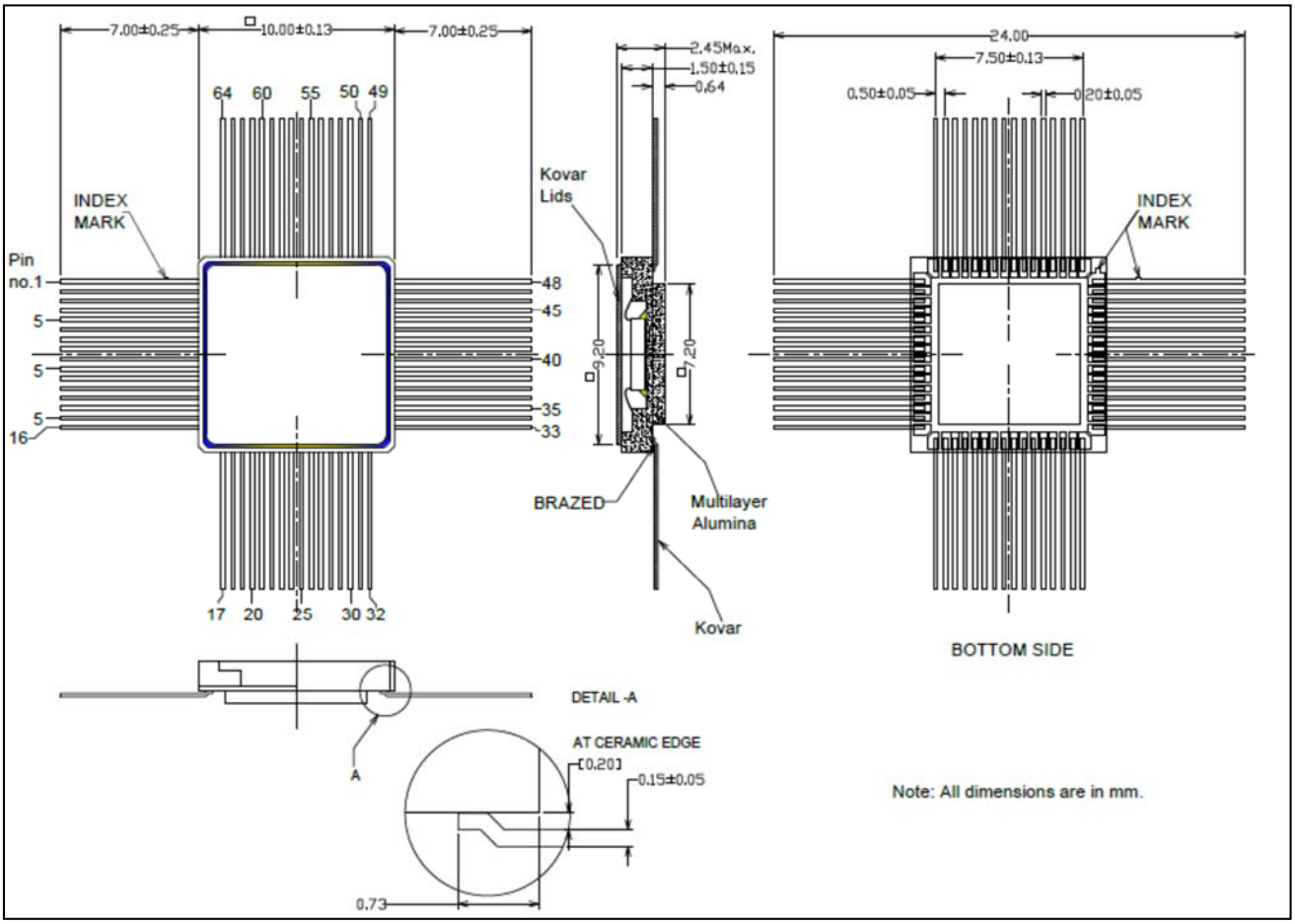
A level shifter (also called logic-level shifter or voltage level translator) is a circuit used to translate signals from one logic level or voltage domain to another, allowing compatibility

between ICs with different voltage requirements, such as TTL and CMOS. Level shifters are used to bridge domains between processors, logic, sensors, and other circuits. Level shifters are used to resolve the voltage incompatibility between various parts of a system.In EF1008 the output of PGA directly goes to level shifter block. Level shifter block provides an option to shift the DC voltage level of the output. There are four different DC levels and these levels can be selected by two input selection lines LS1 and LS0. 3.3V corresponds to logic HIGH and 0V Corresponds to logic LOW for these inputs.

| Sr. No | LS1: LS0 | Output DC level (V) |
|---|---|---|
| 1 | 00 | 0 |
| 2 | 01 | 1.25 |
| 3 | 10 | 1.65 |
| 4 | 11 | 2.5 |

Table8: Level Shifter Control Settings

**PACKAGE DRAWING (64 Pin CQFP):**

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