Research Areas in

VLSI Design, CMOS Process Technology & MEMS Design & Process Technology

(for Preparing Project Proposals by Universities/Institutes)

Respond Programme
Semi-Conductor Laboratory
S.A.S. Nagar

June 2018

Semi-Conductor Laboratory (SCL) offers following areas to academia to participate and contribute in conducting Research & Development (R&D) activities related to Micro-electronics with larger interest related to Space Science/ Technology/ Application

A	**VLSI Design**
A 1	**Charge pump PLL frequency synthesizer design** Description: Design of low phase noise differential CMOS VCO Differential change pump with CMFB (Common Mode Feed Back) Basic specs: 5MHz to 65MHz PLL output frequency required: input frequency × 28
A 2	**Design of instrumentation amplifier** The brief specifications are: Low noise:0.3µV p-p at 0.1 Hz to 10 Hz Low nonlinearity 0.003%(G = -1) High CMRR (Common Mode Rejection Ratio): 120dB (G=1000) Low offset voltage: 50µV Low offset voltage drift: 0.5µV/OC GBW(Gain Band Width) product: 25 MHz
A 3	**Design of a current feedback amplifier** The brief specifications are: High speed: 1650 MHz (G = +1) Low voltage offset: 0.7 mV Low input bias current: 7µA High O/p drive : 100 mA
A 4	**Design of low Noise amplifier** The brief specifications are; To operate from 1.8V power supply To give flat gain from 3 to 5 GHz To deliver 21 dB power gain with only -15dB variation Average noise figure to be 5.4 dB Input and output reflection coefficients to be -13.3 and -19.5 dB
A 5	**Design of 12 bit, 200/250 MHz, low power(<200mW) Pipeline ADC, 3.3V supply,0.18um SCL technology**
A 6	**Design of SAR ADC 14/16 bit, 10/20 Mbps, low power(<300mW), 3.3V supply,0.18um SCL technology**

A 7	**Design of DAC 12/14 bit, 1Gbps, power(<450mW), 3.3V supply,0.18um SCL technology**
A 8	**Design of Programmable Gain Amplifier PSRR>94dB, CMRR>80dB, Gain range 0.1 to 100, Gain Error :0.1%,Gain Drift :5ppm/^{o}C**
A 9	**Design of High Slew Rate amplifier(1200V/µsec),UGB >200MHz,Input offset<100µV,**
A 10	**Design of Low offset (75µVMax) and low drift 1.3µV/^{o}C OPAMP**
A 11	**Design of PLL with VCO, 25MHz -3000MHz,Ultra low phase noise -110dBc/Hz, very low RMS jitter<180fs**
A 12	**Design of adjustable high performance Rad hard negative voltage regulator, Input supply ranges from - 3 V to - 12 V,3 A low dropout voltage**
A 13	**Design of Controller area network (CAN) serial communication physical layer in accordance with the ISO 11898 standard, capability between the differential CAN bus and a CAN controller, with signaling rates up to 1 Mbps.**
A 14	**Design of ultra-low-noise, high-precision voltage reference (1.2V)5ppm/℃ Drift**
A 15	**Design of Radiation Hardened Single port SRAM – different cuts**
A 16	**Design of Radiation Hardened Dual port SRAM – different cuts**
A 17	**Design of DSP Processor (180nm)**
A 18	**Development of Memory Compiler (Radhard) for SP and DP SRAM – to generate all views like .db., .lib, .v, .sdf etc**
A 19	**Design of Memory controller and other microprocessor peripherals**
A 20	**Design of USB 3.0 OR HIGHER**
A 21	**PDSOI analog cell library considering Floating Body (FB) and Self-Heating (SH) effects:** PDSOI technology offers smaller device capacitances when compared with its equivalent bulk CMOS counterpart. In addition, it is also much more resistant to radiation effects when compared to its bulk counterpart. However, circuit design using a PDSOI technology is challenging due to Forward Body Bias (FBB) induced by the Floating Body (FB) effects, hysteresis, body Bipolar Junction Transistor (BJT) and Self-Heating (SH) effects. In analog circuits the FB and SH effects would be very important due to their continuously flowing bias currents and their consequent temporal increase. The performance of analog circuits varies temporally due to the FB induced FBB and SH

	effects since the trans -conductance, output resistance and junction capacitances would change with time. Modelling of the body's hole density (the dynamic equilibrium value) as a function of bias current and layout style and body's hole density to be linked to the small signal model parameters of a PDSOI devices and circuits is required. In this work, we aim to design FB-PDSOI analog standard cells targeted to retain/attain a specified performance within a given time duration. The deliverables of the project would be: TCAD PMOSFET and NMOSFET devices for SCL bulk process calibrated with SCL's process recipe and I-V/C-V measurements. The process recipe would be followed in detail in process simulations and the devices obtained would be calibrated with I-V and C-V measured data. The devices would later be realized using first a TCAD structure editor, and later HSPICE LUT based Verilog-A model for faster simulations. These structure editors and Verilog-A model devices would be used to realize their PDSOI versions. Models relating gm, ro, Ibias and source/drain-body junction capacitance with a FB-PDSOI MOSFET's terminal bias voltages and time for fingered and common centroid analog layout styles and Analog standard cell library consisting of FB-PDSOI analog cells (e.g. OPAMPs and comparators) with several power consumption levels and a specified performance. The library would be at layout (GDS II) and schematic levels.
B	**CMOS Process Technology**
B 1	**Development of 1.8/5V I/O Pads** Development of 1.8/5V I/O circuits (Analog and Digital Pad Circuits with ESD) in 180 nm CMOS process is required. This work to be done as process integration for 5V-MOSFETs in the baseline process has been completed.
B 2	**Development of accurate frequency dependent SPICE models for both active transistors and passive elements** The minimum-channel length MOSFETs SCL process (180nm CMOS technology) has Unity Current Gain frequency, Ft ~55 GHz. The existing device models supported by the technology are however valid up to baseband frequencies (one tenth of Ft of transistors) only. Development of accurate frequency dependent SPICE models for both active transistors and passive elements (Inductors & capacitors) in gigahertz range is required for RF-circuit designs capability in the existing process
B 3	**Modelling of HV (10, 20, 40, 50/60V) devices (n and PMOS)**
B 4	**Development of I/O pads with ESD and Latch up protection for HV Process**
B 5	**Modelling of Bipolar Devices and development of I/O pads**
B 6	**Modelling of Devices in SOI-CMOS Process**

B 7	**Enablement of PDK for HV, Biploar and SOI CMOS Process**
B 8	**Studies on epitaxial growth and characterization of lattice matched InAlN/GaN Heterostructures on silicon for high power applications** GaN-based wide band gap semiconductors are suitable for light emitting diodes, solar cells and ultraviolet photodiodes applications. They are also of use for wireless network base stations and satellite communication systems etc. where GaN-based devices can multiply the efficiency of amplifiers. However, improvements in GaN-based High Electron Mobility Transistors (HEMTs) are limited by the fundamental parameters of established AlGaN / GaN heterostructures. The objective is to explore new heterostructures using InAlN/GaN alloys and enhance the potential power density of HEMTs. InAlN alloys are attractive due to their wide bandgap (0.6 to 6.2 eV) and lattice matching capability with GaN. Extremely high electron gas density coupled with polarisation fields in the heterojunction offers power densities of 30W/mm at 2 to 12 GHz. Focus should be on optimizing the growth of InAlN/GaN HEMT layers on Si using metalorganic vapour deposition (MOCVD) techniques to demonstrate high performance HEMT devices.
B 9	**To develop High Electron Mobility Transistor Structures for High Power RF Devices using Gallium Nitride based wide bandgap Semiconductors on Silicon:** Epitaxial growth Metal Organic CVD (MOCVD) of novel GaN-based hetero structures on silicon as low cost solution for high speed and high power RF devices. Novel stress mitigation techniques to grow crack-free layers. Advanced electrical (Hall, I-V, C-V) surface (AFM), structural (XRD, TEM) and optical (Photoluminescence, Raman) characterizations to assess the quality of layer structures. Submicron HEMT device fabrication and DC and RF characterization
B 10	**Development of Gallium Nitride-based Ultraviolet (UV) photodetectors on Silicon:** Conventional silicon-based UV detectors have some major intrinsic limitations such as aging due to exposure to radiation of much higher energy than the Si bandgap, reduced quantum efficiency in the deep-UV range, significant loss of effective area due to the need to use filters and cooling if low dark current is required. On the other hand, Group III Nitrides offer advantages over Si for UV detection. It is proposed to develop GaN-based ultraviolet (UV) detectors on Si with high performance. GaN and AlGaN layer structures of appropriate composition are required to be grown on Si substrates using MOCVD. Structural, electrical and optical characterizations need to be carried out to optimize the quality, composition and thickness of the layers suitable for photodetector applications. The (Al)GaN MSM (metal-semiconductor-metal) UV detectors (<280 nm) need to be designed and fabricated. The fabricated GaN/Si UV detectors will be aimed to exhibit high performance such as low dark current and high responsivity. Further studies may include addressing the dark current issues using insulating layers such as ZrO2

	and HfO2.
B 11	**Development of process technology for Germanium–via heterogeneous integration with silicon:** It is required to develop a growth method of Ge on Si integration using Chemical Vapour Deposition (CVD) with the aim to achieve reasonable quality for electronic and photonic applications. Once the Ge/Si hetrostructure with the desired properties is obtained, it is required that their electrical and optical properties need to be studied by fabricating active devices. The proposed development work should cover materials study, growth/fabrication, and device characterization.
B 12	**Development of Dry Etch Technology for Aluminium Free InGaP/GaAs/InGaAs epitaxial films for Laser Diodes**: Aluminium Free InGaP/GaAs/InGaAs laser diodes are receiving a great deal of attention because of their superior performance and reliability in comparison to more conventional AlGaAs/GaAs/InGaAs laser diodes. Interest in these devices is driven by their compatibility with the epitaxy-on-electronics (EoE) monolithic optoelectronic integration technology. In particular, high quality aluminium-free laser diodes can be grown at temperature below 475℃, which are compatible with EoE technology whereas laser diodes with aluminium in or near their active regions cannot be grown at such low temperatures. An important challenge with aluminium-free hetrostructures is dry etching vertical end mirror facets and angled deflector structures because of the very different chemical makeup of the layers. In particular, the wider bandgap InGaAsP layers contain significant amounts of In and P, and relatively little or no As, whereas the narrow gap GaAs and InGaAs layers contain roughly 50% As no P, and relatively little or no In. Conventional chlorine based and methane based dry etch techniques do not work well with the Aluminium free hetrostructures. Literature suggest that ion bean assisted chlorine etching of InGaP is very slow at room temperature; at elevated temperature where InGaP etch satisfactorily, GaAs layer are etched without ion beam and several lateral etching occurs, i.e the etch is not directional and anisotropic. The solution to this problem lies in changing the etchant from chlorine to bromine because the vapour pressures of the relevant bromides are much more similar than are those of corresponding chlorides. Consequently, it is possible to find etch conditions for which the etch rates of InGAP and GaAs are sufficiently similar that vertical mirror facets can be successfully etched. Therefore, it is proposed to develop an etch chemistry for the aforesaid application.
B 13	**Si-on-GaAs: Monolithic Hetrogenous Integration of Si-CMOS with GaAs Optoelectronic Devices using EoE technology:** As electronic technology becomes faster and denser, electrical interconnects (wires) have begun to limit the performance of the systems that depends on them. In order to alleviate this problem, optical interconnects are being considered as an alternative. Some of the benefits of optical interconnects include higher speeds of operation with low drive requirements and minimal power dissipation, reduced size weight and cost, freedom from electromagnetic interference, crosstalk and ease of

	layout and routing. In order to implement optical interconnects, optoelectronic integrated circuits (OEICs) which integrate both electrical devices (transistors) with optical devices (optical detectors and emitters) must be created using electronic integrated circuits. However, due to intrinsic structure of silicon, this material is not capable of emitting light efficiently. Compound semiconductors such as GaAs on the other hand can be used to make LEDs and Lasers. Efforts are on without much success to develop technology that would support the monolithic integration of these two types of semiconductors. Therefore, it is proposed to develop a new technology which can combine silicon and GaAs substrates by wafer bonding or Epitaxy on Elec tonics (EoE).
B 14	**Modeling of buried channel MOSFET:** The existing CCD process development at SCL is based on buried channel technology to cater the need of high Charge Transfer Efficiency with high SNR. The output stage of CCD comprises of multiple stage source follower amplifier connected with sense node to produce voltage equivalent of collected charge with greater sensitivity. To design CCD output amplifier, modeling of n-buried channel MOSFET is required using SPICE.
C	**MEMS Design & Process Technology**
C 1	**Micro Fluidics:** Simulations to capture following behaviours • Movement of ionic fluid (EMI-BF4) in a micro-capillary under the influence of electric field. • Formation of Taylor's Cone at the capillary tip under the influence of electric field. • Spray formation & droplet movement under the influence of electric field.
C 2	**Design & development of MEMS based THz devices for space applications.**
C 3	**Design & development of SiC based pressure sensors for harsh environment applications.**
C 4	**Design & development of MEMS flow sensor for low flow rate measurements**
C 5	**Design and Development of Nano Sensors for space applications**